FUJITSU

MOS 1024-BIT NON-VOLATILE RANDOM ACCESS MEMORY

MBM2212-20
MBM2212-25

December 1987
Edition 3.0

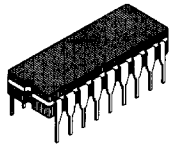
1024-BIT NON-VOLATILE STATIC RANDOM ACCESS MEMORY

The Fujitsu MBM 2212 is a 1024-bit non-volatile static random access memory (NVRAM) combined 1024 bit static random access memory (SRAM) and electrically erasable programmable read only memory (EEPROM) on one-chip. It is designed for applications such as system potentiometer or electrical switch to memorize the system condition etc.

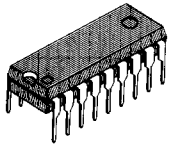
The MBM 2212 is organized as 256 words by 4 bit. Each one word is constituted with a pair of SRAM and EEPROM cell. The read and write operations are performed on the SRAM cell. The data transfer between SRAM and EEPROM is performed using two control pins. The store mode (transfering SRAM data to EEPROM) is executed with one shot pulse applied to $\overline{ST}$ pin in 10ms. The recall mode (transfering EEPROM data to SRAM) is executed with one shot pulse applied to $\overline{RC}$ pin in 1.2μs. Both store and recall operations are completed all bits at one time.

The MBM 2212 is fabricated using N-MOS silicon gate technology with floating gate cells. Single +5V supply and TTL input/output level operations greatly facilitate microprocessor applications.

- 256 words x 4 bit organization, fully decoded
- 10ms self-timed auto store
- 10 years data retention for each store
- Unlimited endurance for recall
- TTL compatible inputs/outputs
- Tri-state output
- Write protection on power-on/off and surge pulse
- Low power consumption;
  Active: 330mW max.
  Standby: 165mW max.
- Fast access time;
  200ns max. (MBM 2212-20)
  250ns max. (MBM 2212-25)
- Standard 18 pin CERAMIC DIP package: Suffix-Z
- Standard 18 pin PLASTIC DIP package: Suffix-P
- Pin compatible with Xicor X2212

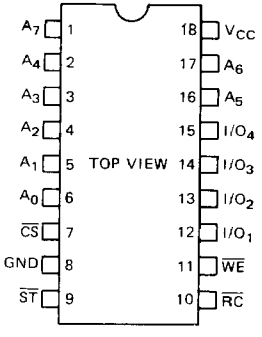


CERAMIC PACKAGE
(CERDIP)
DIP-18C-C01



PLASTIC PACKAGE
(PLASTIC)
DIP-18P-M02

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Supply Voltage with Respect to GND	V_{CC}	-1.0 to +7.0	V
All Input/Output Voltage with Respect to GND	V_{IN}, V_{OUT}	-1.0 to +7.0	V
Output Current with Respect to GND	I_{OUT}	+5.0	mA
Temperature under Bias	T_{BIAS}	-10 to +85	°C
Storage Temperature	T_{STG}	-65 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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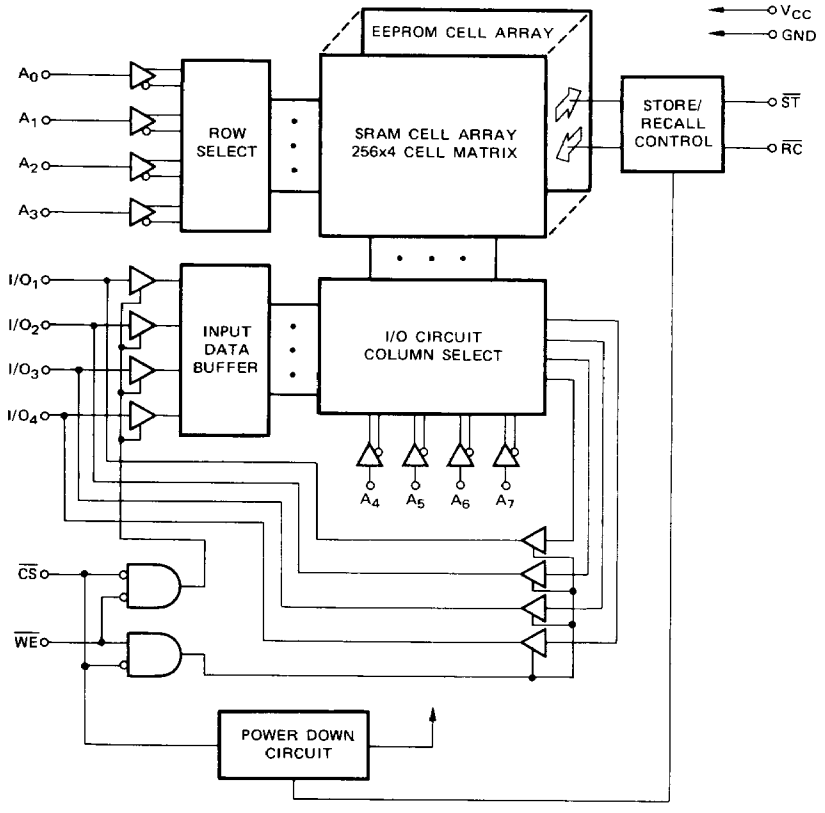
Fig. 1 – MBM 2212 BLOCK DIAGRAM



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CAPACITANCE (T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance (V_{IN} = 0V)	C_{IN}			6	pF
I/O Capacitance ($V_{I/O}$ = 0V)	$C_{I/O}$			8	pF

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	$\overline{RC}$	$\overline{ST}$	I/O	V_{CC}	GND	POWER
Standby	V_{IH}	X	V_{IH}	V_{IH}	High-Z	5V	GND	Standby
Read	V_{IL}	V_{IH}	V_{IH}	V_{IH}	D_{OUT}	5V	GND	Active
Write	V_{IL}	V_{IL}	V_{IH}	V_{IH}	D_{IN}	5V	GND	Active
Recall	X	V_{IH}	V_{IL}	V_{IH}	High-Z	5V	GND	Standby
	V_{IH}	X						
Store	X	V_{IH}	V_{IH}	V_{IL}	High-Z	5V	GND	Active
	V_{IH}	X						

Note: X Can be either V_{IL} or V_{IH}

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltae	V_{CC}	4.5	5.0	5.5	V
Input High Level	V_{IH}	2.0		V_{CC}+0.5	V
Input Low Level	V_{IL}	-1.0*		0.8	V
Operating Temperature	T_A	0		70	°C

Note: * For less than 50ns undershoot, but -0.5V for DC.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Condition	Symbol	Min	Max	Unit
Input Leakage Current	V_{IN} = GND to 5.5V	$\|I_{LI}\|$		10	μA
I/O Leakage Current	$\overline{CS}$ = V_{IH}, $V_{I/O}$ = GND to 5.5V	$\|I_{LO}\|$		10	μA
V_{CC} Standby Current	$\overline{CS}$ = V_{IH}, V_{CC} = 4.5V to 5.5V, $I_{I/O}$ = 0mA*1	I_{SB}		30	mA
V_{CC} Active Current	$\overline{CS}$ = V_{IL}, V_{CC} = 5.5V, $I_{I/O}$ = 0mA*2	I_{CC}		60	mA
Output Low Level	I_{OL} = 4.2mA	V_{OL}		0.4	V
Output High Level	I_{OH} = -2.0mA	V_{OH}	2.4		V
Store Inhibit V_{CC} Voltage		V_{IHBT}		2.7	V

Note: *1 Supply current increases to I_{CC} while store mode regardless of $\overline{CS}$ level.
*2 Supply current reduces to I_{SB} while recall mode regardless of $\overline{CS}$ level.

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AC CHARACTERISTICS

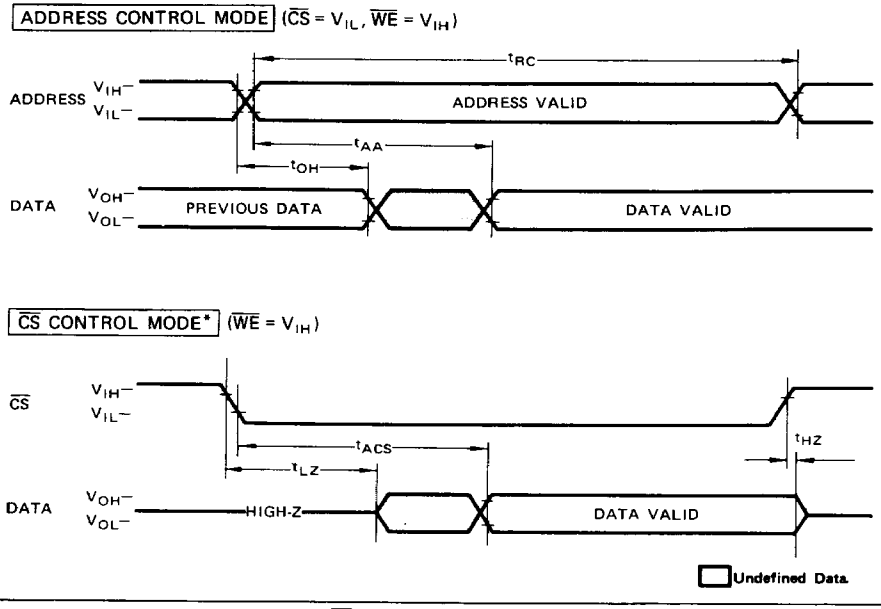
(Recommended operating conditions unless otherwise noted.)

READ MODE ($\overline{WE}$ = $\overline{ST}$ = $\overline{RC}$ = V_{IH})

Parameter	Symbol	MBM 2212-20		MBM 2212-25		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	200		250		ns
Address Access Time	t_{AA}		200		250	ns
Chip Select Access Time	t_{ACS}		200		250	ns
Output Hold after Address Change	t_{OH}	50		50		ns
Chip Select to Output Active*	t_{LZ}	10		10		ns
Chip Select to Output Disable*	t_{HZ}		100		100	ns

Note: * Transition is measured at point of ±500mV from steady state voltage.

READ CYCLE TIMING DIAGRAM ($\overline{WE}$ = V_{IH} for Read Cycle)



Note: *Address valid prior to or coincident with $\overline{CS}$ transition low.

WRITE MODE ($\overline{ST}$ = $\overline{RC}$ = V_{IH})

Parameter	Symbol	MBM 2212-20/25		Unit
		Min	Max	
Write Cycle Time	t_{WC}	300		ns
Chip Select to End of Write ($\overline{WE}$ = V_{IL})	t_{CW}	150		ns
Address Setup Time	t_{AS}	50		ns
Write Pulse Width ($\overline{CS}$ = V_{IL})	t_{WP}	150		ns
Write Recovery Time*1	t_{WR}	25		ns
Data Valid to End of Write	t_{DW}	100		ns
Data Hold Time	t_{DH}	0		ns
Write Enable to Output High-Z*2	t_{WZ}		100	ns
Output Active from End of Write*3	t_{OW}	10		ns

Note: *1 t_{WR} is defined from the end point of write.
*2 Transition is measured at point of ±500mV from steady state voltage.
*3 If $\overline{CS}$ goes high coincident with $\overline{WE}$ high transition, DATA OUT remains in a high impedance state.

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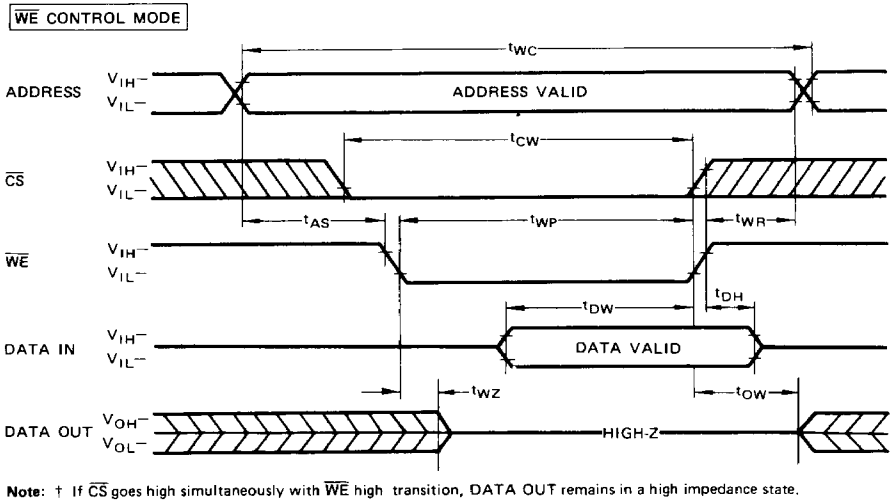
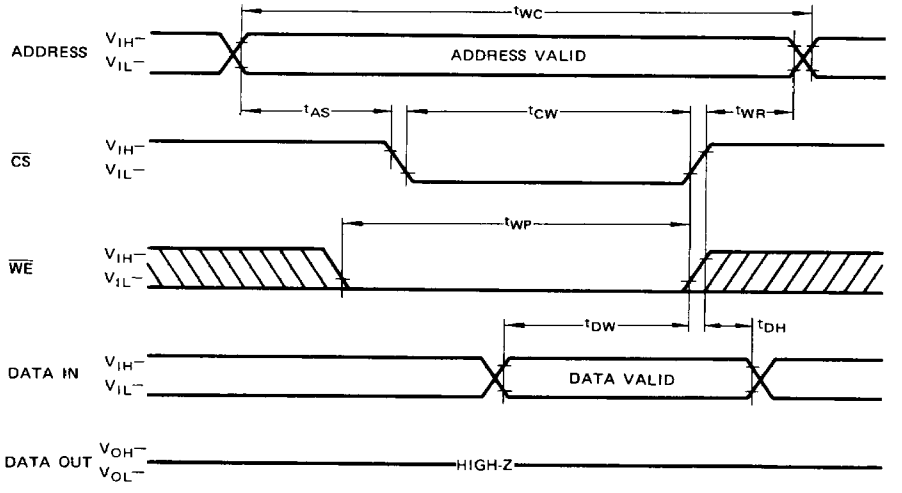
WRITE CYCLE TIMING DIAGRAM



Note: † If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high transition, DATA OUT remains in a high impedance state.

WRITE CYCLE TIMING DIAGRAM

$\overline{CS}$ CONTROL MODE



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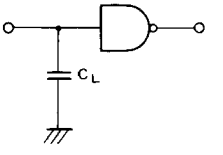
AC TEST CONDITIONS (including EEPROM mode)

Input Pulse Levels:	0.6V to 2.4V
Input Rise/Fall Times:	≦ 10 ns
Input Reference Levels:	0.8V, 2.2V
Output Reference Levels:	0.8V, 2.2V
Output Load:	1 TTL gate and C_L = 100pF



EEPROM READ/WRITE INFORMATION

The MBM 2212 can not read or write EEPROM data externally and it must be transferred from/to SRAM cell array corresponding to each EEPROM bit. $\overline{RC}$ and $\overline{ST}$ pins are assigned to execute these operation easily.

RECALL MODE

The recall mode is initiated when negative pulse (⊓⊔) is applied to $\overline{RC}$ pin while either $\overline{CS}$ = V_{IH} or $\overline{WE}$ = V_{IH} and is completed within 1.2μs. The supply current is reduced to standby current automatically.
Please notice that the SRAM data is replaced by the EEPROM data after the execution of this operation.

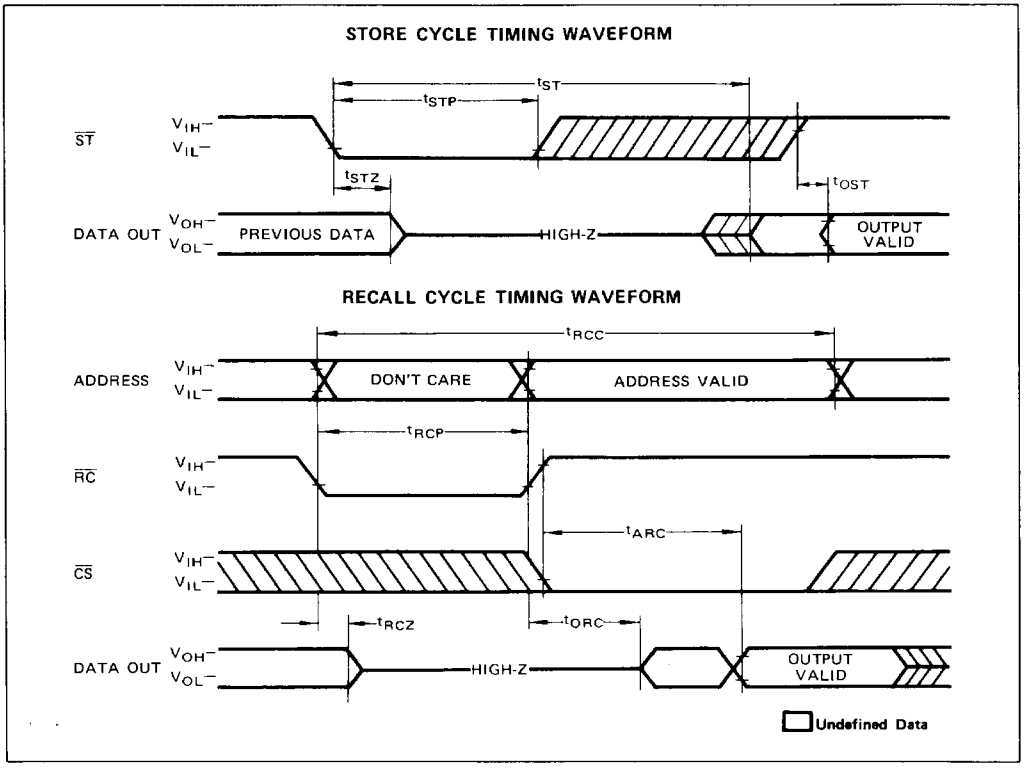
STORE MODE

The store mode is initiated when negative pulse (⊓⊔) is applied to $\overline{ST}$ pin while either $\overline{CS}$ = V_{IH} or $\overline{WE}$ = V_{IH} and is completed automatically be the on-chip timer. During this operation mode, all input and output pins are inhibited. The original SRAM data remains after the store mode.

The MBM 2212 has two protection circuits to prevent a erroneous store mode. Noise filter circuit for duration of less than 20ns negative pulse on $\overline{ST}$ pin is on the chip.
Auto-standby circuit prevents the store data on the EEPROM cell array from the destruction when V_{CC} is less than +3V.

When V_{CC} power is ON or OFF, the V_{IH} input level must be applied to $\overline{ST}$ pin before or while V_{CC} is greater than +3V.

These operation modes as store mode, recall mode and SRAM write mode have the same logical priority. Normally the first set logical condition determines the following operation mode among $\overline{ST}$, $\overline{RC}$ and $\overline{WE}$ pins.



EEPROM READ/WRITE INFORMATION (cont'd)

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

RECALL MODE ($\overline{WE}$ = $\overline{ST}$ = V_{IH})

Parameter	Symbol	MBM 2212-20/25		Unit
		Min	Max	
Recall Cycle Time	t_{RCC}	1200		ns
Recall Pulse Width	t_{RCP}	450		ns
$\overline{RC}$ to Output Disable*	t_{RCZ}		150	ns
$\overline{RC}$ to Output Active*	t_{ORC}	10		ns
$\overline{RC}$ to Output Valid	t_{ARC}		750	ns

Note: * Transition is measured at point of ±500mV from steady state voltage.

STORE MODE ($\overline{WE}$ = $\overline{RC}$ = V_{IH})

Parameter	Symbol	MBM2212-20		MBM2212-25		Unit
		Min	Max	Min	Max	
Store Cycle Time	t_{ST}		10		20	ms
Store Pulse Width*1	t_{STP}	100		100		ns
Store to Output Disable*2	t_{STZ}		500		500	ns
Output Valid from End of Store	t_{OST}		200		250	ns

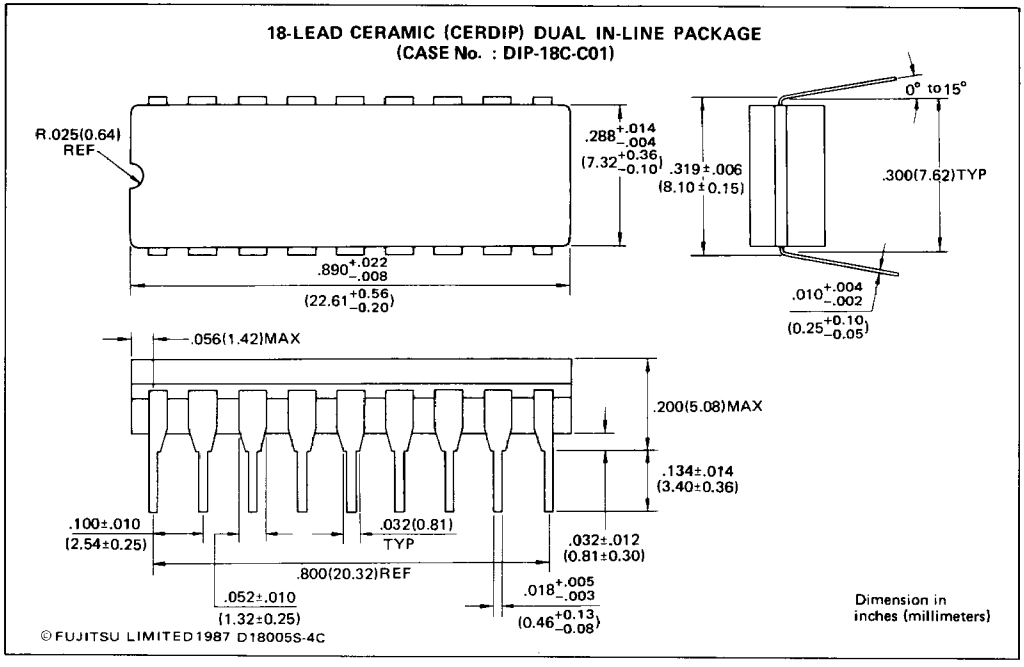
Note: *1 It is protected to enter into the store mode by less than 20ns pulse width.
*2 Transition is measured at point of ±500mV from steady state voltage.

ENDURANCE

Number of Store Cycles	Number of Data Changes per Bit	Unit
100,000	10,000	times

PACKAGE DIMENSIONS

Standard 18-pin Ceramic DIP (Suffix: -Z)



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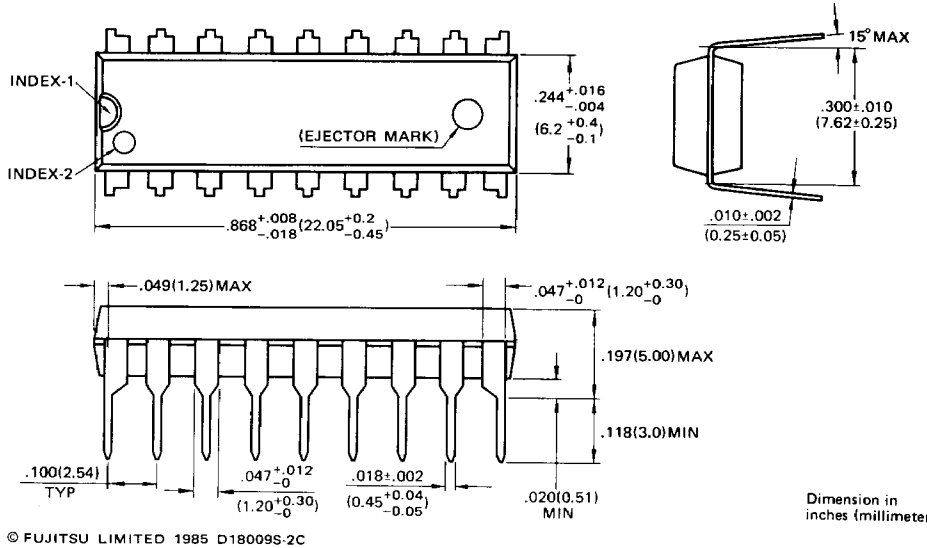
PACKAGE DIMENSIONS

Standard 18-pin Plastic DIP (Suffix: -P)

18-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-18P-M02)



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