

MC14009AL
MC14009CL
MC14009CP
MC14010AL
MC14010CL
MC14010CP

HEX BUFFERS

The MC14009 hex inverter/buffer and MC14010 noninverting hex buffer are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS devices find primary use where low power dissipation and/or high noise immunity is desired. Both devices can be used as current "sink" or "source" drivers, as CMOS-to-CMOS or CMOS-to-bipolar (TTL or DTL) logic level converters, or as multiplexers (1-to-6). The MC14009 also provides the invert function.

- Quiescent Power Dissipation = 50 nW/package typical
- High Current Sinking Capability
8.0 mA minimum @ $V_{OL} = 0.5\text{ V}$ and $V_{DD} = 10\text{ V}$
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14009/10 AL)
3.0 Vdc to 16 Vdc (MC14009/10CL/CP)
- Wide CMOS-to-Bipolar Conversion Range –
From MCMOS operating with specified supply voltage range to TTL or DTL operating with +3.0 V to +6.0 V supply. Conversion with logic output levels $> 6.0\text{ V}$ is permitted if $V_{CC} \leq V_{DD}$.
- Pin for Pin Replacement for CD4009A – MC14009
CD4010A – MC14010

McMOS

(LOW-POWER COMPLEMENTARY MOS)

HEX BUFFERS

Inverting – MC14009AL/CL/CP
 Noninverting – MC14010AL/CL/CP



L SUFFIX
CERAMIC PACKAGE
CASE 620



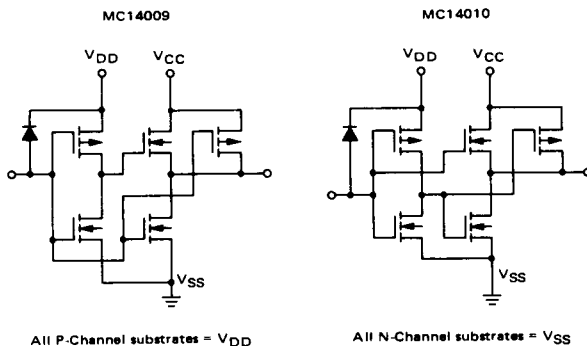
P SUFFIX
PLASTIC PACKAGE
CASE 648

MAXIMUM RATINGS (Voltages referenced to V_{SS} , Pin 8)

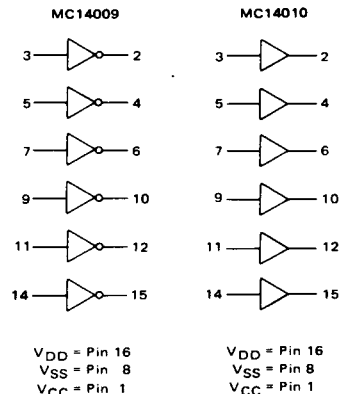
Rating	Symbol	Value	Unit
DC Supply Voltage ($V_{CC} \leq V_{DD}$) –AL Version CL,CP Version	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin*	I	10	mAdc
Operating Temperature Range –AL Version CL,CP Version	T_A	-55 to +125 -40 to +85	$^{\circ}\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^{\circ}\text{C}$

*Buffered Outputs may supply higher current.

CIRCUIT SCHEMATIC
 (1/6 OF CIRCUIT SHOWN)



LOGIC DIAGRAMS



See Mechanical Data Section for package dimensions.

MC14009, MC14010 (continued)

ELECTRICAL CHARACTERISTICS

Characteristic	Figure	Symbol	V _{DD} Vdc	V _{CC} Vdc	MC14009/10AL						MC14009/10CL/CP						Unit		
					-55°C		+25°C		+125°C		-40°C		+25°C		+85°C				
					Min	Max	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max		Min	Max
Output Voltage	1,2,3	V _{out}	5.0 10 15	5.0 10 15	"0" Level						"1" Level						Vdc		
MC14009 (V _{in} = 5.0 Vdc) (V _{in} = 10 Vdc) (V _{in} = 15 Vdc)					0.01	0	0.01	0.05	0.01	0	0.01	0	0.01	0	0.01	0.05			
MC14010 (V _{in} = 0 Vdc) (V _{in} = 0 Vdc) (V _{in} = 0 Vdc)					0.01	0	0.01	0.05	0.01	0	0.01	0	0.01	0	0.01	0.05			
MC14009 (V _{in} = 0 Vdc) (V _{in} = 0 Vdc) (V _{in} = 0 Vdc)					4.99	4.99	5.0	4.95	4.99	4.99	5.0	4.95	4.99	5.0	4.95	4.99			
MC14010 (V _{in} = 5.0 Vdc) (V _{in} = 10 Vdc) (V _{in} = 15 Vdc)					4.99	4.99	5.0	4.95	4.99	4.99	5.0	4.95	4.99	5.0	4.95	4.99			
MC14009 (V _{in} = 0 Vdc) (V _{in} = 0 Vdc) (V _{in} = 0 Vdc)					9.99	9.99	10	9.95	9.99	9.99	10	9.95	9.99	10	9.95	9.99			
Noise Immunity*		-	V _{NL}	5.0 10 15	5.0 10 15	MC14009						MC14010						Vdc	
(V _{out} ≥ 3.5 Vdc) (V _{out} ≥ 7.0 Vdc) (V _{out} ≥ 10.5 Vdc)						1.0	1.0	2.0	0.9	1.0	1.0	2.0	0.9	1.0	1.0	2.0			0.9
(V _{out} ≤ 1.5 Vdc) (V _{out} ≤ 3.0 Vdc) (V _{out} ≤ 4.5 Vdc)						1.4	1.5	2.25	1.5	1.4	1.5	2.25	1.5	1.4	1.5	2.25			1.5
(V _{out} ≤ 1.5 Vdc) (V _{out} ≤ 3.0 Vdc) (V _{out} ≤ 4.5 Vdc)			1.5	1.5	2.25	1.4	1.5	1.5	2.25	1.4	1.5	1.5	2.25	1.4					
(V _{out} ≥ 3.5 Vdc) (V _{out} ≥ 7.0 Vdc) (V _{out} ≥ 10.5 Vdc)			2.9	3.0	4.5	2.9	3.0	2.9	4.5	3.0	2.9	3.0	4.5	3.0					
(V _{out} ≤ 1.5 Vdc) (V _{out} ≤ 3.0 Vdc) (V _{out} ≤ 4.5 Vdc)			3.0	3.0	4.5	2.9	3.0	2.9	4.5	3.0	2.9	3.0	4.5	3.0					
Output Drive Current	5		I _{OH}	5.0 10 15	5.0 10 15	Source						Sink							mAdc
(V _{OH} = 2.5 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)						-1.85	-1.25	-1.75	-0.9	-1.5	-1.25	-1.75	-1.0	-1.75	-1.75	-1.0	-4.48		
(V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)						3.75	3.0	4.0	2.1	3.6	3.0	4.0	2.4	3.6	3.0	4.0	2.4		
(V _{OH} = 2.5 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)			0.9	0.6	0.8	0.4	0.7	0.6	0.8	0.5	0.7	0.6	0.8	0.5					
(V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)			8.0	8.0	10	5.6	9.6	8.0	10	6.4	9.6	8.0	10	6.4					
(V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)			35	35	35	35	35	35	35	35	35	35	35	35					
Input Current	-	I _{in}	-	-	-	-	-	-	-	-	-	-	-	pAdc					
Input Capacitance (V _{in} = 0)	MC14009	C _{in}	-	-	-	10	-	-	-	-	10	-	-	pF					
	MC14010	C _{in}	-	-	-	5.0	-	-	-	-	5.0	-	-	pF					
Quiescent Dissipation	7	P _D	5.0 10 15	-	1.5	0.06	1.5	100	15	0.1	300	50	0.15	15	210	μW			
						0.15					50		0.85	700					
Turn-On Delay Time** (C _L = 15 pF)	4	t _{PHL}	5.0 10 15	5.0 10 15	MC14009						MC14010						ns		
(I _{PHL} = (0.16 ns/pF) C _L + 12 ns)					-	15	55	-	-	-	15	70	-	-	-	15		70	
(I _{PHL} = (0.10 ns/pF) C _L + 8.0 ns)					-	9.0	30	-	-	-	9.0	40	-	-	-	9.0		40	
(I _{PHL} = (0.08 ns/pF) C _L + 6.0 ns)					-	7.0	-	-	-	-	7.0	-	-	-	-	7.0		-	
(I _{PHL} = (0.05 ns/pF) C _L + 7.0 ns)					-	5.0	25	-	-	-	5.0	35	-	-	-	5.0		35	
(I _{PHL} = (0.03 ns/pF) C _L + 5.0 ns)					-	5.0	5.0	-	-	-	5.0	5.0	-	-	-	5.0		5.0	
(I _{PHL} = (0.38 ns/pF) C _L + 19 ns)					-	25	55	-	-	-	25	70	-	-	-	25		70	
(I _{PHL} = (0.08 ns/pF) C _L + 19 ns)					-	20	30	-	-	-	20	40	-	-	-	20		40	
(I _{PHL} = (0.06 ns/pF) C _L + 14 ns)					-	15	-	-	-	-	15	-	-	-	-	15		-	
(I _{PHL} = (0.08 ns/pF) C _L + 14 ns)					-	15	25	-	-	-	15	35	-	-	-	15		35	
(I _{PHL} = (0.08 ns/pF) C _L + 9.0 ns)					-	10	-	-	-	-	10	-	-	-	-	10		-	
Turn-Off Delay Time** (C _L = 15 pF)					4	t _{PLH}	5.0 10 15	5.0 10 15	MC14009/10						MC14010				
(I _{PLH} = (1.0 ns/pF) C _L + 35 ns)	50	80	-	-					-	50	100	-	-	-	50	100			
(I _{PLH} = (0.40 ns/pF) C _L + 19 ns)	25	55	-	-					-	25	70	-	-	-	25	70			
(I _{PLH} = (0.34 ns/pF) C _L + 15 ns)	20	45	-	-					-	20	55	-	-	-	20	55			
(I _{PLH} = (0.36 ns/pF) C _L + 20 ns)	25	30	-	-					-	25	40	-	-	-	25	40			
(I _{PLH} = (0.16 ns/pF) C _L + 18 ns)	20	-	-	-					-	20	-	-	-	-	20	-			
Output Rise Time** (C _L = 15 pF)	4	t _r	5.0 10 15	5.0 10 15	MC14009						MC14010						ns		
(t _r = (2.4 ns/pF) C _L + 44 ns)					-	80	125	-	-	-	80	160	-	-	-	80		160	
(t _r = (1.0 ns/pF) C _L + 20 ns)					-	35	100	-	-	-	35	120	-	-	-	35		120	
(t _r = (0.62 ns/pF) C _L + 20 ns)					-	30	-	-	-	-	30	-	-	-	-	30		-	
(t _r = (1.6 ns/pF) C _L + 56 ns)					-	80	125	-	-	-	80	160	-	-	-	80		160	
(t _r = (0.76 ns/pF) C _L + 39 ns)					-	50	100	-	-	-	50	120	-	-	-	50		120	
(t _r = (0.6 ns/pF) C _L + 21 ns)					-	30	-	-	-	-	30	-	-	-	-	30		-	
(t _r = (0.22 ns/pF) C _L + 9.0 ns)					-	13	45	-	-	-	13	60	-	-	-	13		60	
(t _r = (0.10 ns/pF) C _L + 7.0 ns)					-	9.0	40	-	-	-	9.0	50	-	-	-	9.0		50	
(t _r = (0.07 ns/pF) C _L + 6.0 ns)					-	7.0	-	-	-	-	7.0	-	-	-	-	7.0		-	
(t _r = (0.20 ns/pF) C _L + 22 ns)					-	25	45	-	-	-	25	60	-	-	-	25		60	
(t _r = (0.07 ns/pF) C _L + 15 ns)					-	16	40	-	-	-	16	50	-	-	-	16		50	
(t _r = (0.07 ns/pF) C _L + 9.0 ns)	-	10	-	-	-	-	10	-	-	-	-	10	-						

*DC Noise Margin (V_{NH}, V_{NL}) is defined as the maximum voltage change, from an ideal "1" or "0" input level, before producing an output state change.

**The formula given is for the typical characteristics only.

FIGURE 1 – CURRENT AND VOLTAGE TRANSFER CHARACTERISTICS TEST CIRCUIT

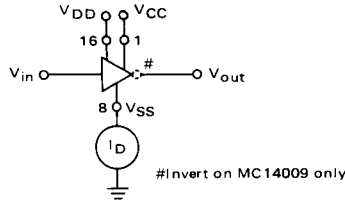


FIGURE 2 – TYPICAL VOLTAGE AND CURRENT TRANSFER CHARACTERISTICS versus TEMPERATURE

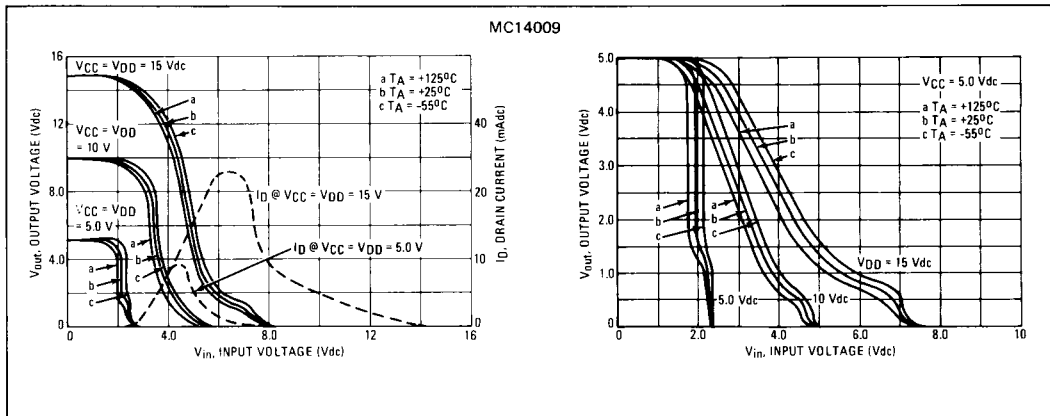


FIGURE 3 – TYPICAL VOLTAGE TRANSFER CHARACTERISTICS versus TEMPERATURE

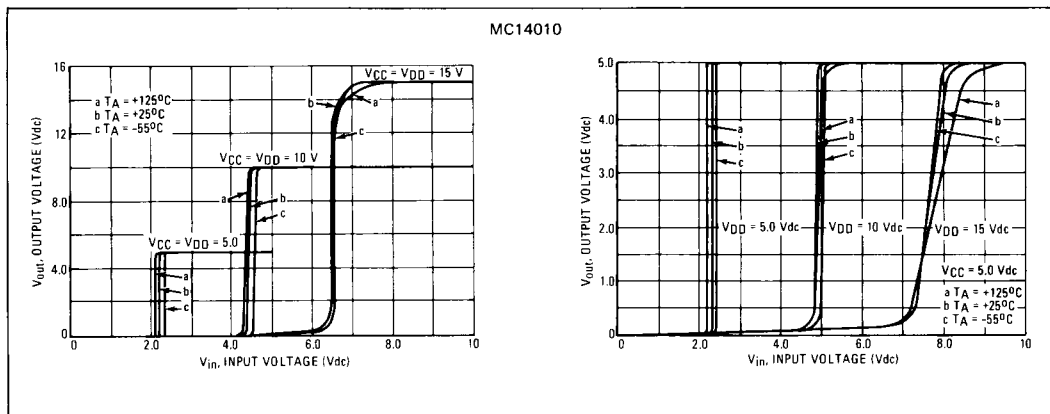


FIGURE 4 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

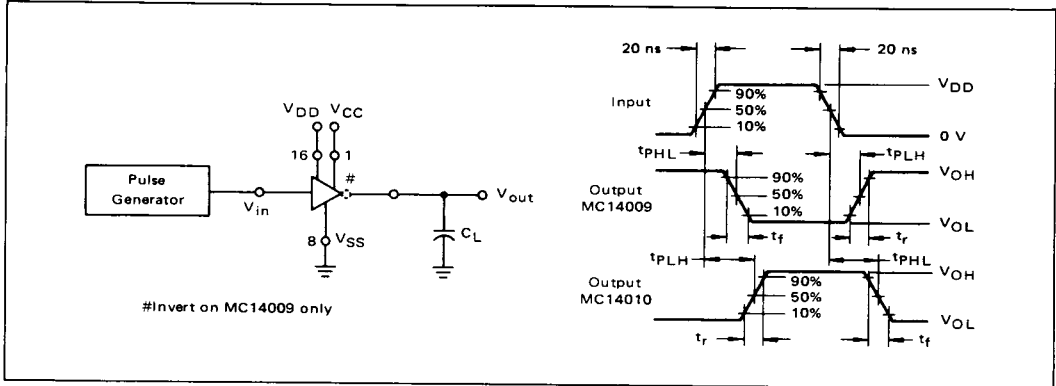


FIGURE 5 – TYPICAL OUTPUT SOURCE CHARACTERISTICS

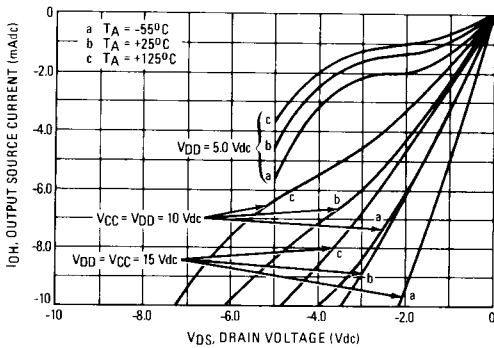
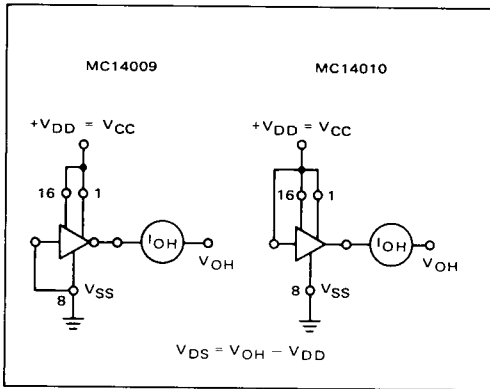


FIGURE 6 – TYPICAL OUTPUT SINK CHARACTERISTICS

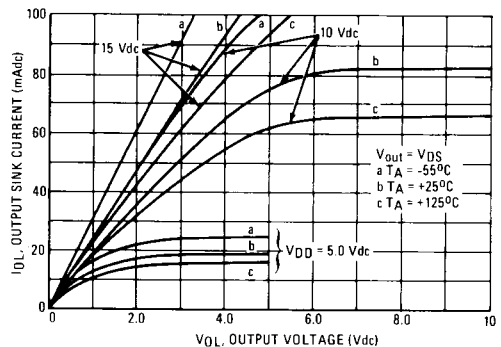
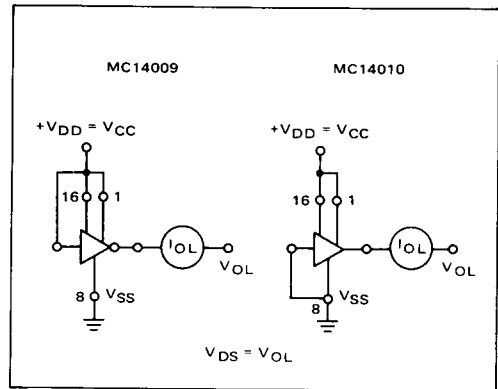
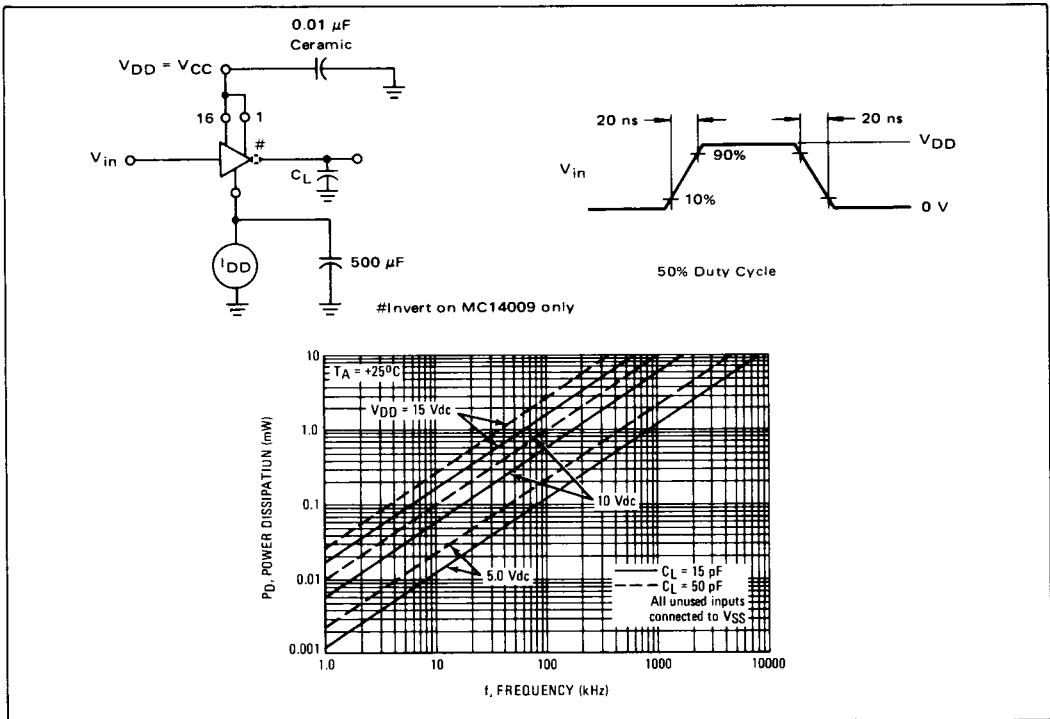


FIGURE 7 – TYPICAL DYNAMIC POWER DISSIPATION CHARACTERISTICS



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).