# OKI Semiconductor

# MSM6295

## 4-CHANNEL MIXING ADPCM VOICE SYNTEHSIS LSI

### GENERAL DESCRIPTION

The Oki MSM6295 is a 4-channel mixing ADPCM voice synthesis LSI which is fabricated using Oki's low power CMOS silicon gate technology.

The MSM6295 can access an external ROM, where speech or sound effects data is stored. The maximum external ROM size is 256K bytes.

The MSM6295 has a 4-channel synthesis stage which allows the simultaneous playback of four different channels. It is used to have a voice with BGM (Back Ground Music) effect, instrumental sound, echo etc.

### FEATURES

- Oki straight ADPCM algorithm
- Number of bits/sample: 4
- 18 address lines for external ROM
- 8-bit control bus for mode setting
- External memory capacity 2Mbit
- Interface with common CPU and MPU
- Clock frequency: 1 MHz to 5 MHz
- Sampling frequency:
  6.5 kHz and 8 kHz
  (@1.056 MHz clock)
  25.6 kHz and 32 kHz
  (@4.224 MHz clock)
- Number of words: 127 maximum
- Vocalization time: 60 sec maximum
  (@8 kHz, straight)
- Built-in DA converter: 12-bit
- DA output format: A-class
- Voice level attenuation: 0dB ~ –24dB
  on each channel (9 steps)
  –3dB/step
- Low power CMOS process
- 5 V single power supply
- 44-pin plastic QFP (QFP44-P-910-V1K)
  (QFP44-P-910-K)
- 42-pin plastic DIP (DIP42-P-600)

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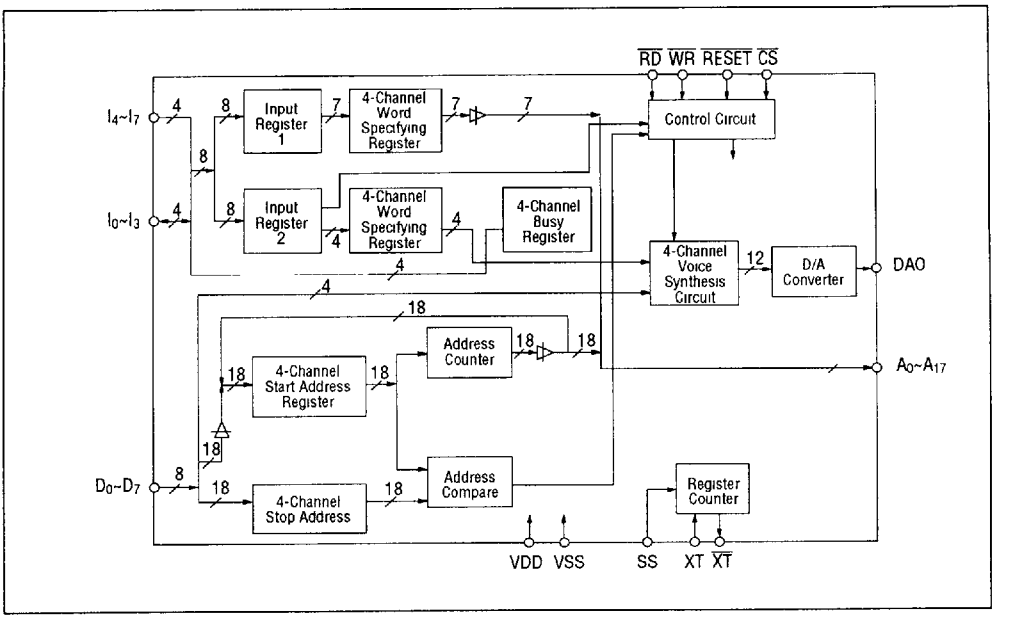
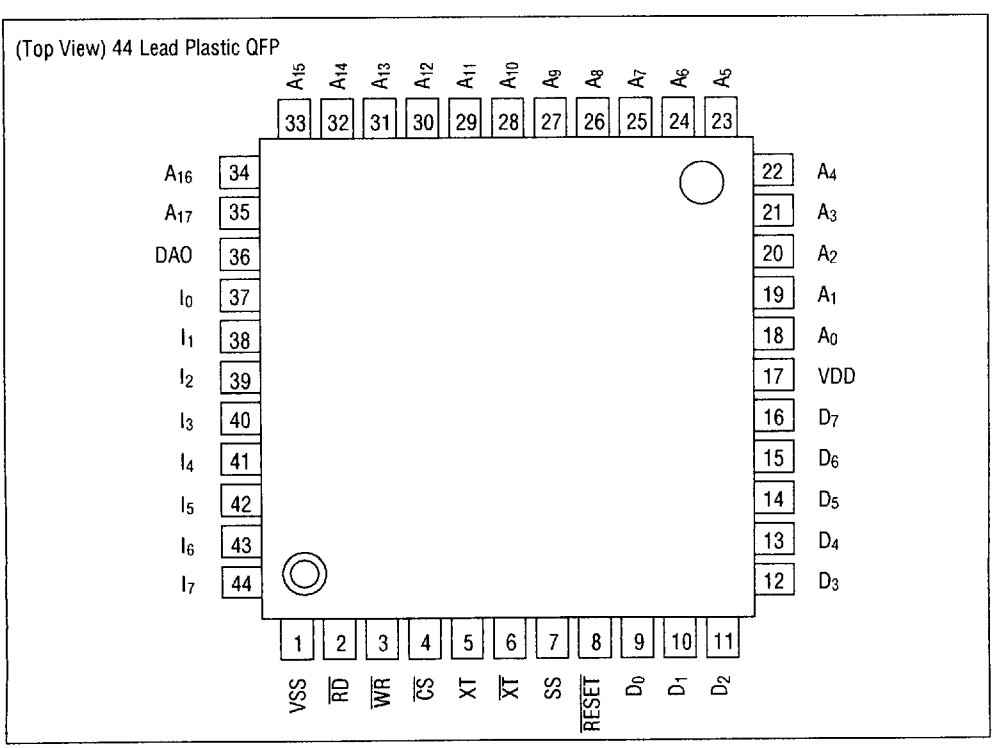
## BLOCK DIAGRAM




## PIN CONFIGURATION





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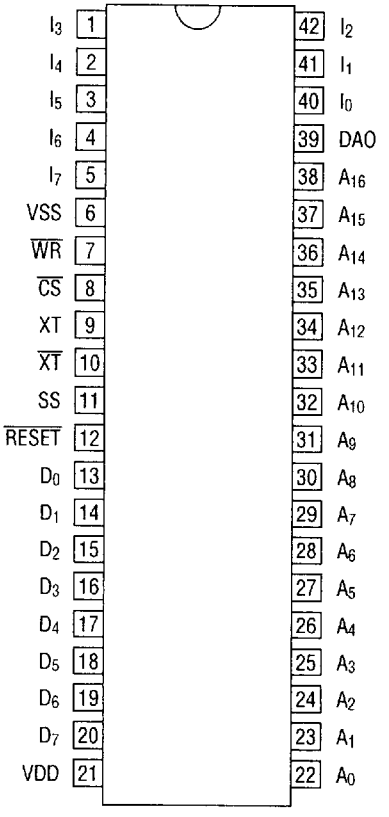
(Top View) 42 Lead Plastic DIP



## ELECTRICAL CHARACTERISTICS

### • Absolute Maximum Ratings

| Parameter | Symbol | Conditions | Value | Unit |
|---|---|---|---|---|
| Power supply voltage | VDD | Ta = 25°C | −0.3 ~ +7.0 | V |
| Input voltage | $V_{IN}$ | Ta = 25°C | −0.3 ~ VDD +0.3 | V |
| Storage temperature | $T_{stg}$ | — | −55 ~ +150 | °C |

### • Recommended Operating Conditions

| Parameter | Symbol | Conditions | Value | Unit |
|---|---|---|---|---|
| Power supply voltage | VDD | VSS = 0V | 4.5 ~ +5.5 | V |
| Operating temperature | $T_{op}$ | VSS = 0V | −40 ~ +85 | °C |
| Oscillation frequency | $f_{OSC}$ | VSS = 0V | 1 ~ 5 | MHz |

### • DC Characteristics

(VDD = 4.5~5 5V, VSS = 0V, Ta = −40 ~ +85°C)

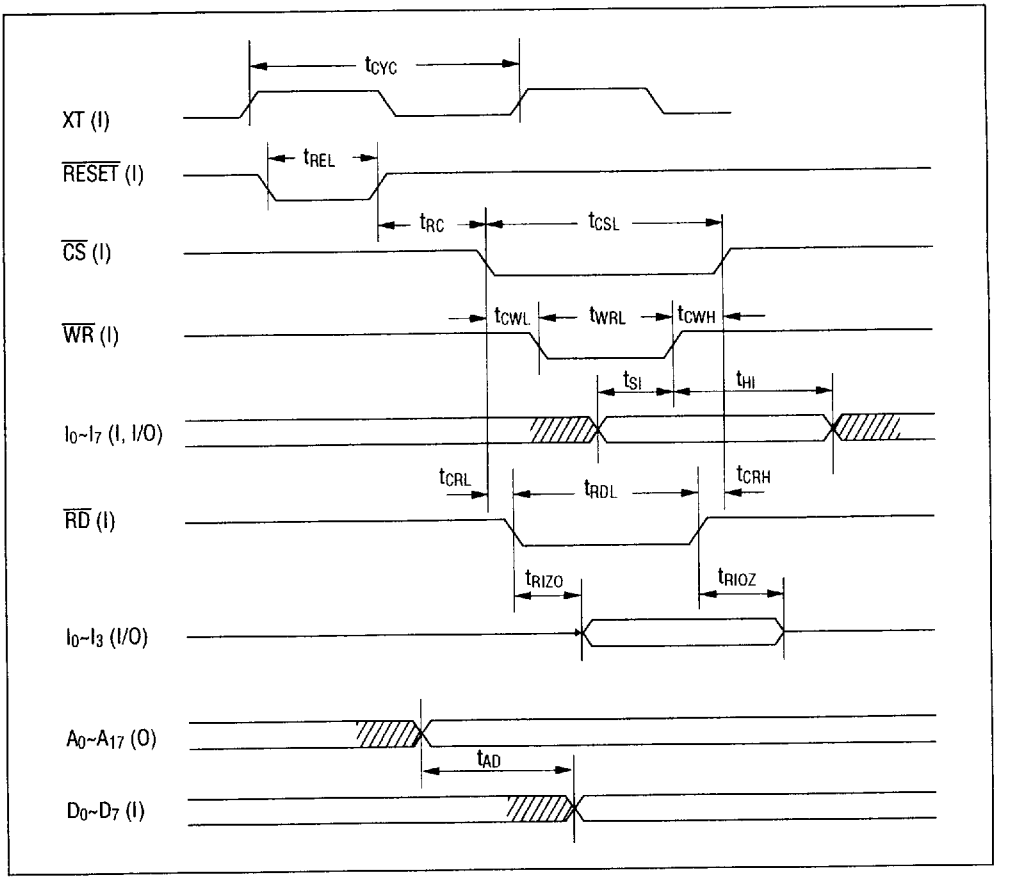
| Parameter | Symbol | Conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| "L" input current | $I_{IL}$ | $V_{IL}$ = VSS | −10 | — | — | µA |
| "H" input current | $I_{IH}$ | $V_{IH}$ = VDD | — | — | 10 | |
| "L" input voltage | $V_{IL}$ | — | — | — | 0.8 | V |
| "H" input voltage | $V_{IH}$ | — | 2.4 | — | — | |
| "L" output voltage | $V_{OL}$ | $I_{OL}$ = 0.8 mA | — | — | 0.45 | V |
| "H" output voltage | $V_{OH}$ | $I_{OH}$ = −40 µA | 3.7 | — | — | |
| Output leakage current | $I_{LO}$ | VSS ≦ $V_{OUT}$ ≦ VDD | −10 | — | 10 | µA |
| Operating current | $I_{DD}$ | $f_{OSC}$ = 5.0MHz | — | 5 | 10 | mA |
| DA output relative error | $\|V_{DAE}\|$ | No load | — | — | 20 | mV |
| DA output impedance | $R_{DAOUT}$ | — | — | 15 | — | kΩ |

## • AC Characteristics

(VDD = 4.5~5.5V, VSS = 0V, Ta = –40 ~ +85°C)

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Clock cycle | $t_{CYC}$ | 200 | – | – | ns |
| Clock duty cycle | $f_{DUTY}$ | 40 | 50 | 60 | % |
| $\overline{RESET}$ pulse width | $t_{REL}$ | 100 | – | – | ns |
| $\overline{CS}$ pulse width | $t_{CSL}$ | 250 | – | – | ns |
| $\overline{WR}$ pulse width | $t_{WRL}$ | 200 | – | – | ns |
| $\overline{RD}$ pulse width | $t_{RDL}$ | 300 | – | – | ns |
| $\overline{RESET}$ fall to $\overline{CS}$ fall | $t_{RC}$ | 250 | – | – | ns |
| $\overline{CS}$ fall to $\overline{WR}$ fall | $t_{CWL}$ | 50 | – | – | ns |
| $\overline{WR}$ raise to $\overline{CS}$ raise | $t_{CWH}$ | 0 | – | – | ns |
| Data set up time of $I_0$-$I_7$ in respect to $\overline{WR}$ raise | $t_{SI}$ | 80 | – | – | ns |
| Data hold time of $I_0$-$I_7$ in respect to $\overline{WR}$ raise | $t_{HI}$ | 80 | – | – | ns |
| $\overline{RD}$ fall to stable output of $I_0$-$I_3$ | $t_{RIZO}$ | – | – | 120 | ns |
| $\overline{RD}$ raise to flow status output of $I_0$-$I_3$ | $t_{RIOZ}$ | 0 | – | 120 | ns |
| $\overline{CS}$ fall to $\overline{RD}$ fall | $t_{CRL}$ | 20 | – | – | ns |
| $\overline{RD}$ raise to $\overline{CS}$ raise | $t_{CRH}$ | 0 | – | – | ns |
| Address stable ($A_0$-$A_{17}$) to data input of $D_0$-$D_7$ | $t_{AD}$ | – | – | $5 \cdot t_{CYC}+90$ | ns |

## • Timing Chart



## PIN DESCRIPTION

| Pin Name | Pin No. | I/O | Function |
|---|---|---|---|
| $I_0$ | 37 | I/O | Instruction bus and condition outputs |
| $I_1$ | 38 | I/O | These pins are inputs for phrase specification Maximum number |
| $I_2$ | 39 | I/O | of phrases is 127 $I_0$~$I_3$ pins are also outputs of the operating |
| $I_3$ | 40 | I/O | state, busy state, for channels 1~4 and are further used to select the |
| $I_4$ | 41 | I | channel attenuation rate. |
| $I_5$ | 42 | I | |
| $I_6$ | 43 | I | |
| $I_7$ | 44 | I | |
| $\overline{WR}$ | 3 | I | Write enable input<br>Data is written on the data bus of $I_0$~$I_7$ The data is written when $\overline{WR}$ goes low |
| $\overline{RD}$ | 2 | I | Read enable input<br>The output busy state of channels 1~4 on the data bus of $I_0$~$I_3$ Can be read using this input. A high level indicates busy |
| $\overline{CS}$ | 4 | I | Chip select input<br>Input "L" level either when $\overline{WR}$ signal is input or when $\overline{RD}$ signal is input |
| $\overline{RESET}$ | 8 | I | Reset input<br>Reset condition is available by inputting "L" level<br>All functions are suspended during reset |
| $A_0$ | 18 | I | Address outputs |
| 〃 | 〃 | 〃 | These pins are to address the external ROM in which voice data |
| $A_{17}$ | 35 | I | is stored. |
| $D_0$ | 9 | I | Voice data inputs |
| 〃 | 〃 | 〃 | |
| $D_7$ | 16 | I | |
| SS | 7 | I | Sampling frequency select input<br>When oscillation frequency is 1.056 MHz or 4 224 MHz, the following choices are available by inputting "H" level or "L" level to SS. |

| | SS = "H" | SS = "L" |
|---|---|---|
| Oscillation frequency 1.056 MHz | 8 kHz | 6 5 kHz |
| Oscillation frequency 4.224 MHz | 32 kHz | 25 6 kHz |

| | | | |
|---|---|---|---|
| DAO | 36 | O | Voice synthesis output<br>Voice synthesized analog signal is output from this pin |
| XT | 5 | I | Crystal oscillator pin |
| $\overline{XT}$ | 6 | O | Crystal oscillator pin |
| VDD | 17 | – | Power supply pin |
| VSS | 1 | – | Ground |

## FUNCTION EXPLANATION

### 1. Phrase Selection

Phrases are specified and read into the 2 byte data which consists of $I_0$~$I_7$ data bus.

The phrase selection data is latched when $\overline{WR}$ goes high while $\overline{CS}$ is low (L).

The format of the phrase specification input is as follows.

| | $I_7$ | $I_6$ | $I_5$ | $I_4$ | $I_3$ | $I_2$ | $I_1$ | $I_0$ |
|---|---|---|---|---|---|---|---|---|
| 1st Byte | 1 | Phrase selection data | | | | | | |
| 2nd Byte | Channel specification | | | | Reduction specification | | | |

As shown in the above chart, $I_7$ of the first 1 data byte is always 1. $I_0$ ~$I_6$ of the first 1 data byte specifies the phrase. Phrase selection data has a selection of 127 phrases which corresponds to 0000001~1111111. The phrase selection data is used for to $A_3$~$A_9$ address outputs, and they specify both start and stop address which are stored in the external ROM.

**Relation between Phrase Selection Data and ROM Address**

| Phrase selection data | – | $I_6$ | $I_5$ | $I_4$ | $I_3$ | $I_2$ | $I_1$ | $I_0$ | – | – | – |
|---|---|---|---|---|---|---|---|---|---|---|---|
| External ROM address | $A_{17}$~$A_{10}$ | $A_9$ | $A_8$ | $A_7$ | $A_6$ | $A_5$ | $A_4$ | $A_3$ | $A_2$ | $A_1$ | $A_0$ |
| Selection | | | | | | | | | | | |
| Not valid | 0~0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Phrase 1 | 0~0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| Phrase 2 | 0~0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| Phrase 3 | 0~0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| Phrase 127 | 0~ | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |

* Phrases cannot be specified with all inputs = "0"

The second byte of data specifies the synthesis operation channel as well as specific channel reduction of the synthesized playback. The channel selection format is shown below.

It is not possible to specify multiple channels at the same time. For example, it is not possible to specify channel 1 and channel 3 simultaneously.

**Channel Specification**

| Channel | $I_7$ | $I_6$ | $I_5$ | $I_4$ |
|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 1 |
| 2 | 0 | 0 | 1 | 0 |
| 3 | 0 | 1 | 0 | 0 |
| 4 | 1 | 0 | 0 | 0 |

## REDUCTION SELECTION

All 0's is considered as 0 dB of the analyzed sound itself. The reduction is made through 9 levels from about 0 dB to - 24 dB with the steps of about - 3 dB. Reduction format is shown below.

**Reduction Specification**

| Attenuation level | $I_3$ | $I_2$ | $I_1$ | $I_0$ |
|---|---|---|---|---|
| 0 dB | 0 | 0 | 0 | 0 |
| –3.2 dB | 0 | 0 | 0 | 1 |
| –6.0 dB | 0 | 0 | 1 | 0 |
| –9.2 dB | 0 | 0 | 1 | 1 |
| –12.0 dB | 0 | 1 | 0 | 0 |
| –14.5 dB | 0 | 1 | 0 | 1 |
| –18 0 dB | 0 | 1 | 1 | 0 |
| –20 5 dB | 0 | 1 | 1 | 1 |
| –24.0 dB | 1 | 0 | 0 | 0 |

## 2. Voice Synthesis Channel Suspension

Voice synthesis operation of any channel can be suspended. Channel suspension is controlled by bits $I_3$~$I_6$ of data bytes $I_0$~$I_7$. To suspend a channel, make $I_7$=0, while $I_3$~$I_6$ represent the channels which should be suspended.

Channel suspension occurs even if multiple channels are selected. For example, if $I_3$~$I_6$ are all 1 and $I_7$=0, then channels 1~4 are suspended simultaneously.

| Suspended channel | $I_7$ | $I_6$ | $I_5$ | $I_4$ | $I_3$ | $I_2$ | $I_1$ | $I_0$ |
|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | 1 | X | X | X |
| 2 | 0 | 0 | 0 | 1 | 0 | X | X | X |
| 3 | 0 | 0 | 1 | 0 | 0 | X | X | X |
| 4 | 0 | 1 | 0 | 0 | 0 | X | X | X |

## 3. Data ROM

1) ADDRESS DATA

This specifies start and stop address of ADPCM speech data. One phrase start and end address consists of 8 bytes. The first 3 bytes show start address while the last 3 bytes show stop address. The other 2 bytes are empty.

By selecting the first address in which the start address is stored, the selected speech data is played back.

| Address | |
|---|---|
| 0 | $SA_1$ |
| 1 | $SA_2$ |
| 2 | $SA_3$ |
| 3 | $EA_1$ |
| 4 | $EA_2$ |
| 5 | $EA_3$ |
| 6 | EMPTY |
| 7 | EMPTY |

Start addresses ($SA_1$~$SA_3$) and stop addresses ($EA_1$~$EA_3$) are stored according to the chart shown below.

| | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|
| $SA_1/EA_1$ | 0 | 0 | 0 | 0 | 0 | 0 | $A_{17}$ | $A_{16}$ |
| $SA_2/EA_2$ | $A_{15}$ | $A_{14}$ | $A_{13}$ | $A_{12}$ | $A_{11}$ | $A_{10}$ | $A_9$ | $A_8$ |
| $SA_3/EA_3$ | $A_7$ | $A_6$ | $A_5$ | $A_4$ | $A_3$ | $A_2$ | $A_1$ | $A_0$ |

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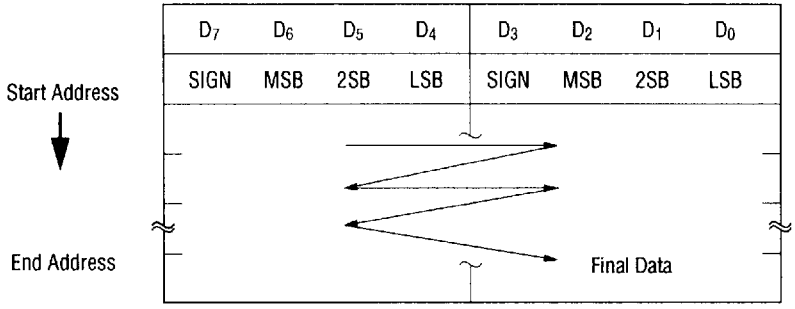
2) ADPCM SPEECH DATA

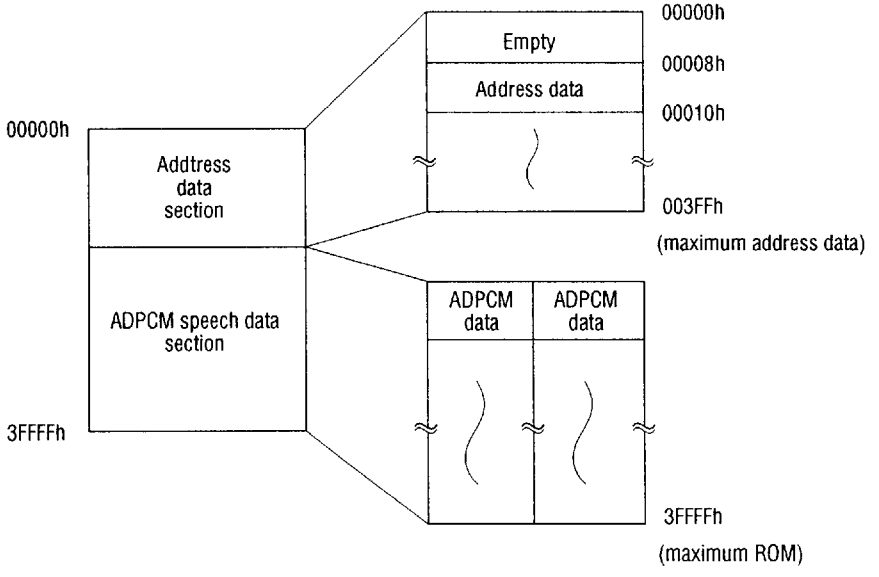
ADPCM speech data consists of (2) 4-bit samples. So, 1 byte stores 2 samples. Data arrangement proceeds from higher rank bits ($D_4$~$D_7$) to lower rank bits ($D_0$~$D_3$). The storage of speech data should always be ended with the lower rank bit. So, always store an even number of samples.

Speech data is produced by Speech Development Tool AR76-202.




3) DATA ROM STRUCTURE

The following chart shows the memory map of the source data ROM.




When the maximum 127 phrases are selected in address data section, the data is written up to ROM address 003FFh.

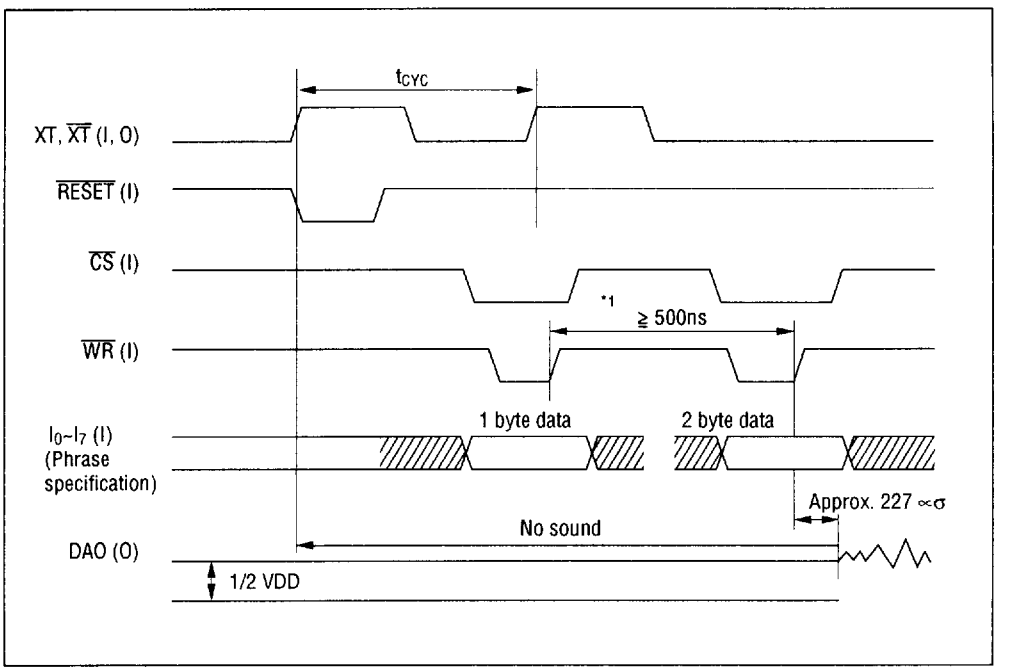
When 1 phrase is selected, address data is written from ROM address 00008h to 0000Fh, and the rest is used as the ADPCM data section.

## FUNCTIONAL DESCRIPTION

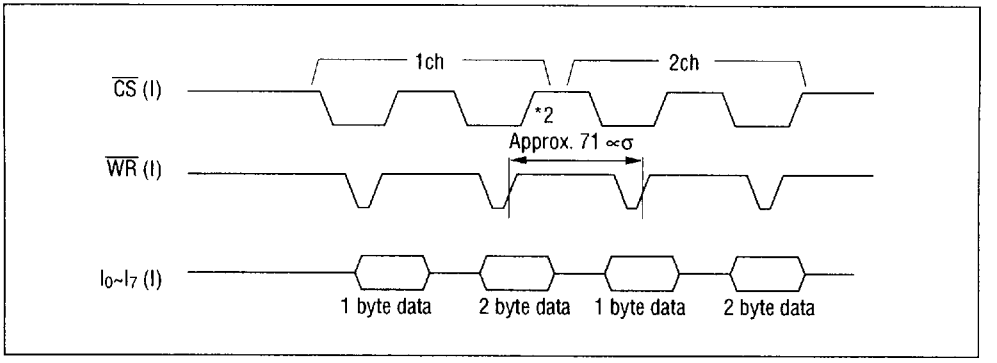
### 1. Phrase Selection Input

This procedure is to input phrase selection data onto the data bus inputs $I_0$~$I_7$. The data is latched internally when $\overline{WR}$ rises from "L" to "H", while $\overline{CS}$ remains "L".

Voice synthesis operation does not start till the second byte is fully latched.




**Note:** Phrase selection is from channel 1 to channel 4 continuously.
*1 An interval of 75 $T_{CYC}$ (max.) is needed between phrases.

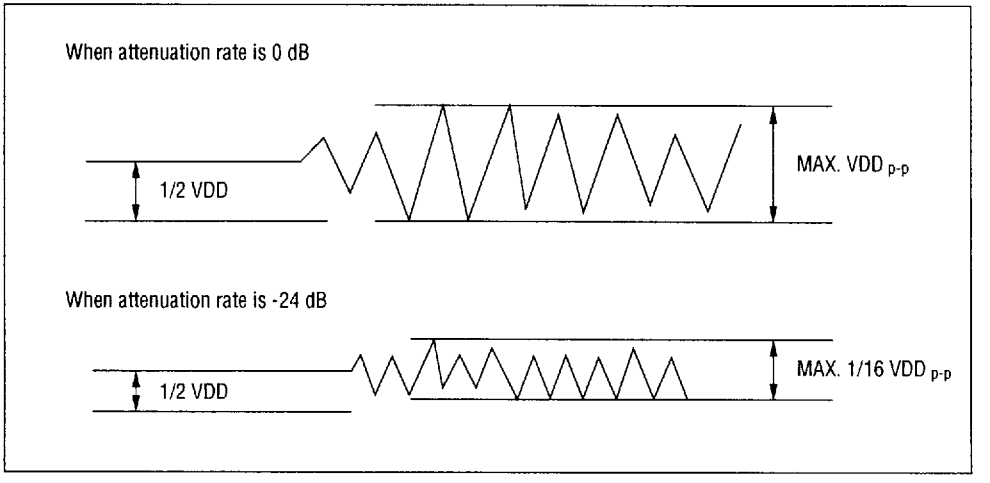



**Note:** *2 Oscillation frequency = 1 056 MHz SS = "L"

Voice synthesis playback can be started from any channel, 1 to 4. The arrangement of each channel can be in any order.

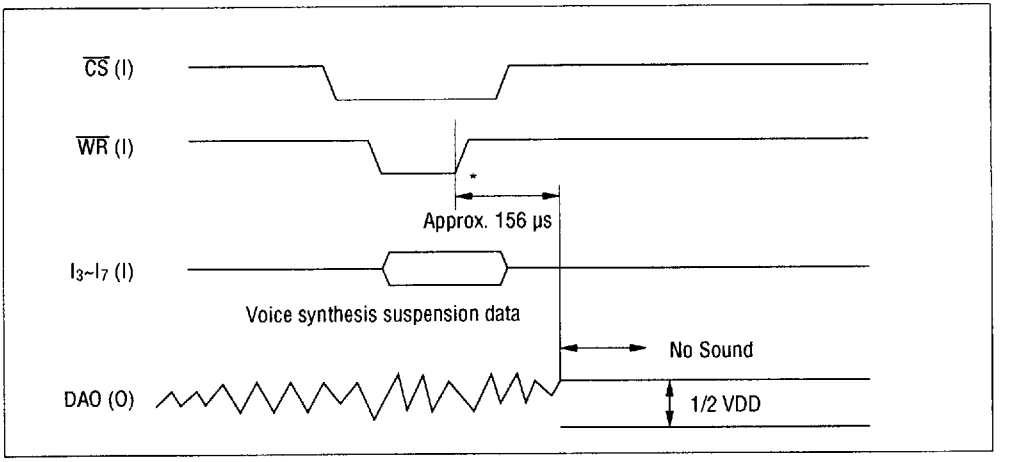
## 2. Attenuation of Synthesized Speech

The second byte of the phrase selection data contains the phrase attenuation data in bits D0 - D3. Synthesized data is attenuated in –3 dB steps from 0 dB to –24 dB.



### 3. Speech Synthesis Channel Suspension

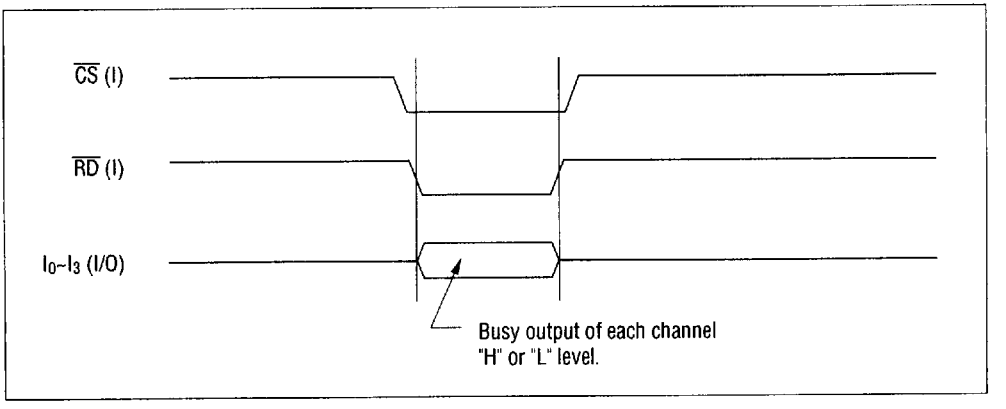
This is accomplished by writting synthesis channel suspension data onto data bus inputs $I_3$~$I_7$. The data is latched internally when $\overline{WR}$ goes from "L" to "H" while $\overline{CS}$ remains active (L). Since synthesis suspension data is 1 byte data, synthesis operation is suspended right after the rising edge of $\overline{WR}$. Multiple channels can be specified, making it possible to suspend channels 1~4 simultaneously.



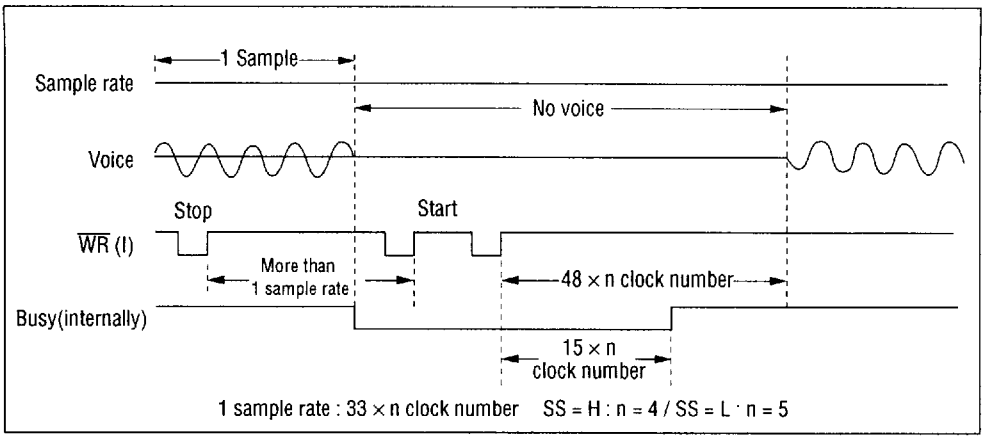

**Note:** * Oscillation frequency = 1.056 MHz SS = "L"

### 4. Reading the Busy Status

While $\overline{CS}$ is "L" and $\overline{RD}$ is "L", each operation state, the busy state of channels 1~4 is output on $I_0$~$I_3$. "H" is output during synthesized playback.



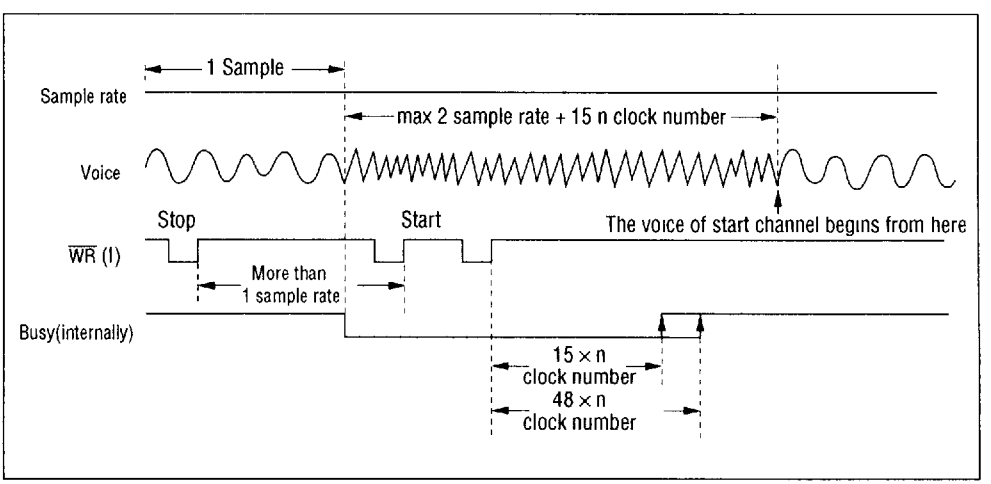
## 5. Start and Stop of 1 Channel




**Start and Stop of Signal Channel**

When a single channel (either of channels 1-4) starts again after it has stopped, the first write for start must be input with a delay of more than one sample rate from the stop write as shown in the figure above. When stop is entered, voice playback stops all the next sample and BUSY becomes "L".

When start is entered again, voice is output after 48 x n clock from the second byte write. BUSY becomes "H" after 15 x n clock internally.




**Start and Stop in Plural Channels**

When channels are operating, the first byte write for start must be input with a delay of more than one sample rate from stop write.

The channel where stop was input, stops at every sample.

Voice off the channel where stop was again input is output after a maximum 2 samples = 15 x n clocks from the preceding sample point.

BUSY becomes "H" during the 48 x n clock time.

## 6. Application Circuit