CX77304-17 PA Module for Tri-band EGSM DCS PCS / GPRS

Applications

- Tri-band cellular handsets encompassing
  - Class 4 EGSM900
  - Class 1 DCS1800
  - PCS1900, and
  - Up to Class 10 GPRS multi-slot operation

Features

- High efficiency
  - EGSM 55%
  - DCS 50%
  - PCS 45%

- Input/output matching
  - 50 Ω internal

- Small outline
  - 9.1 mm $\times$ 11.6 mm

- Low profile
  - 1.5 mm

- Low APC current
  - 10 μA typical

- Gold plated, lead-free contacts

Description

The CX77304-17 Power Amplifier Module (PAM) is designed in a compact form factor for tri-band cellular handsets comprising EGSM900, DCS1800, and PCS1900 operation. It also supports Class 10 General Packet Radio Service (GPRS) multi-slot operation.

The PAM consists of an EGSM900 PA block, a DCS1800/PCS1900 PA block, impedance-matching circuitry for 50 Ω input and output, and bias control circuitry. Two separate Heterojunction Bipolar Transistor (HBT) PA blocks are fabricated on a single Gallium Arsenide (GaAs) die. One PA block operates in the EGSM900 band and the other PA block supports both the DCS1800 and the PCS1900 bands. Optimized for lithium ion battery operation, both PA blocks share common power supply pins to distribute current. A custom CMOS integrated circuit provides the internal interface circuitry, including a current amplifier that minimizes the required power control current (I_{APC}) to 10 μA, typical. The GaAs die, the Silicon (Si) die, and passive components are mounted on a multi-layer laminate substrate. The assembly is encapsulated with plastic overmold.

The RF input and output ports are internally matched to 50 Ω to reduce the number of external components for a tri-band design. Extremely low leakage current (2 μA, typical) of the dual PA module maximizes handset standby time. The CX77304-17 also contains band-select switching circuitry to select EGSM (logic 0) and DCS/PCS (logic 1) as determined from the Band Select (BS) signal. In the block diagram shown below, the BS pin selects the PA output (DCS/PCS OUT or EGSM OUT) while the Analog Power Control (APC) controls the level of output power.
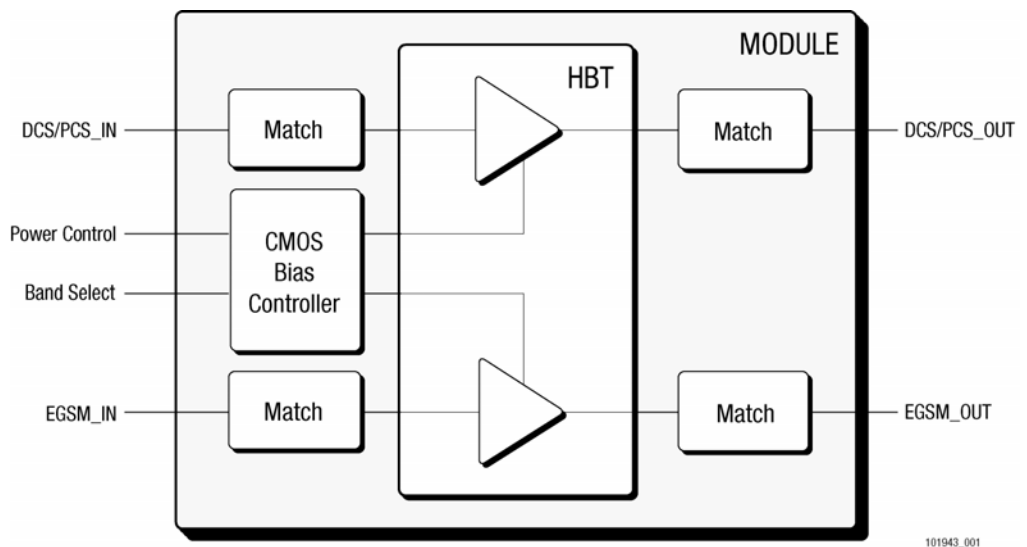

Figure 1. Functional Block Diagram

Electrical Specifications

The following tables list the electrical characteristics of the CX77304-17 Power Amplifier. Table 1 lists the absolute maximum ratings and Table 2 shows the recommended operating conditions. Table 3 shows the electrical characteristics of the CX77304-17 for EGSM, DCS, and PCS modes. A typical CX77304-17 application diagram appears in Figure 2.

The CX77304-17 is a static-sensitive electronic device and should not be stored or operated near strong electrostatic fields. Detailed ESD precautions along with information on device dimensions, pin descriptions, packaging and handling can be found in later sections of this data sheet.

Table 1. Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
Input Power (P_{IN})	—	15	dBm
Supply Voltage (V_{CC}), Standby, $V_{APC} \leq 0.3$ V	—	7	V
Control Voltage (V_{APC})	−0.5	$V_{CC\_MAX} - 0.2$ (See Table 3)	V
Storage Temperature	−55	+100	°C

Table 2. Recommended Operating Conditions [1]

Parameter	Minimum	Typical	Maximum	Unit
Supply Voltage (V_{CC})	2.9	3.5	4.8 [1]	V
Supply Current (I_{CC})	0.0		2.5 [1]	A

Operating Case Temperature (T_{CASE})
  1-Slot (12.5% duty cycle)
  2-Slot (25% duty cycle)
  3-Slot (37.5% duty cycle)
  4-Slot (50% duty cycle)
	−20
	−20
	−20
	−20
			100
			90
			75
			60
				°C

[1] For charging conditions with $V_{CC} > 4.8$ V, derate I_{CC} linearly down to 0.5 A max at $V_{CC} = 5.5$ V.

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Table 3. CX77304-17 Electrical Specifications [1] (1 of 6)

Parameter	Symbol	Test Condition	Minimum	Typical	Maximum	Units
General						
Supply voltage	V_{CC}	—	2.9	3.5	4.8	V
Power control current	I_{APC}	—	—	10	100	µA
Leakage Current	I_Q	V_{CC} = 4.5 V V_{APC} = 0.3 V T_{CASE} = +25 °C P_{IN} ≤ −60 dBm	—	—	5	µA
APC Enable Threshold	V_{APC_TH}	—	200	—	600	mV
APC Enable Switching Delay	t_{SW}	Time from V_{APC} ≥ V_{APC_TH} until P_{OUT} ≤ (P_{OUT_FINAL} − 3 dB)	5		8	µs
EGSM900 Mode (f = 880 to 915 MHz and P_{IN} = 7 to 12 dBm)						
Parameter	Symbol	Test Condition	Minimum	Typical	Maximum	Units
Frequency range	f	—	880	—	915	MHz
Input power	P_{IN}	—	7	—	12	dBm
Analog power control voltage	V_{APC}	P_{OUT} = 32 dBm	1.2	1.7	2.1	V
Power Added Efficiency	PAE	V_{CC} = 3.5 V P_{OUT} ≥ 34.5 dBm V_{APC} ≈ 2.0 V pulse width 577 µs duty cycle 1:8 T_{CASE} = +25 °C	50	55	—	%
	$PAE\_{LOW\ INPUT}$	V_{CC} = 3.5 V P_{OUT} ≥ 34.5 dBm V_{APC} ≈ 2.0 V pulse width 577 µs duty cycle 1:8 T_{CASE} = +25 °C P_{IN} = 4 dBm	—	52	—	
Harmonics 2nd to 13th	$2f_0$ to $13f_0$	BW = 3 MHz 5 dBm ≤ P_{OUT} ≤ 35 dBm	—	—	−7	dBm
Output power	P_{OUT}	V_{CC} = 3.5 V V_{APC} ≈ 2.0 V T_{CASE} = +25 °C	34.5	35.0	—	dBm
	P_{OUT_MAX}	V_{CC} = 3.5 V V_{APC} ≈ 2.0 V T_{CASE} = +25 °C P_{IN} = 4 dBm	—	34.75	—	
	P_{OUT_MAX}	V_{CC} = 2.9 V V_{APC} ≤ 2.6 V T_{CASE} = −20 °C to +100 °C (See Table 2 for multislot) P_{IN} = 7 dBm	32.0	33.0	—	
	P_{OUT_MAX}	V_{CC} = 4.8 V V_{APC} ≤ 2.6 V T_{CASE} = −20 °C to +100 °C (See Table 2 for multislot) P_{IN} = 7 dBm	32.0	33.0	—	

Table 3. CX77304-17 Electrical Specifications [1] (2 of 6)

Parameter	Symbol	Test Condition	Minimum	Typical	Maximum	Units
EGSM900 Mode (f = 880 to 915 MHz and P_{IN} = 7 to 12 dBm) [continued]						
Input VSWR	Γ_{IN}	P_{OUT} = 5 to 35 dBm controlled by V_{APC}	—	1.5:1	2:1	—
Forward isolation	$P_{OUT\_STANDBY}$	P_{IN} = 12 dBm V_{APC} = 0.3 V	—	−35	−30	dBm
Switching time	τ_{RISE}, τ_{FALL}	Time from P_{OUT} = −10 dBm to P_{OUT} = +5 dBm $\tau \approx 90\%$	—	5	8	μs
		Time from P_{OUT} = −10 dBm to P_{OUT} = +20 dBm $\tau \approx 90\%$	—	5	8	
		Time from P_{OUT} = −10 dBm to P_{OUT} = +34.5 dBm $\tau \approx 90\%$	—	2	4	
Spurious	Spur	All combinations of the following parameters: V_{APC} = controlled [2] P_{IN} = min. to max. V_{CC} = 2.9 V to 4.8 V Load VSWR = 8:1, all phase angles	No parasitic oscillation > −36 dBm			
Load mismatch	Load	All combinations of the following parameters: V_{APC} = controlled [2] P_{IN} = min. to max. V_{CC} = 2.9 V to 4.8 V Load VSWR = 10:1, all phase angles	No module damage or permanent degradation			
Noise power	P_{NOISE}	At f_0 + 20 MHz RBW = 100 kHz V_{CC} = 3.5 V 5 dBm $\leq P_{OUT} \leq$ 34.5 dBm	—	—	−82	dBm
		At f_0 + 10 MHz RBW = 100 kHz V_{CC} = 3.5 V 5 dBm $\leq P_{OUT} \leq$ 34.5 dBm	—	—	−76	
		At 1805 to 1880 MHz RBW = 100 kHz V_{CC} = 3.5 V 5 dBm $\leq P_{OUT} \leq$ 34.5 dBm	—	—	−90	
Coupling of 2nd and 3rd harmonic from the EGSM band into the DCS / PCS band	f_0	Measured at the DCS output −15 dBm $\leq P_{OUT} \leq$ 34 dBm	—	6	9	dBm
	$2f_0$		—	−25	−20	
	$3f_0$		—	−18	−15	

Table 3. CX77304-17 Electrical Specifications [1] (3 of 6)

DCS1800 Mode (f = 1710 to 1785 MHz and P_{IN} = 6 to 11 dBm)						
Parameter	**Symbol**	**Test Condition**	**Minimum**	**Typical**	**Maximum**	**Units**
Frequency range	f	—	1710	—	1785	MHz
Input power	P_{IN}	—	6	—	11	dBm
Analog power control voltage	V_{APC}	P_{OUT} = 29.5 dBm	1.35	1.7	2.1	V
Power Added Efficiency	PAE	V_{CC} = 3.5 V $P_{OUT} \geq$ 32 dBm $V_{APC} \approx$ 2.0 V pulse width 577 µs duty cycle 1:8 T_{CASE} = +25 °C	45	50	—	%
	$PAE_{LOW\ INPUT}$	V_{CC} = 3.5 V $P_{OUT} \geq$ 32 dBm $V_{APC} \approx$ 2.0 V pulse width 577 µs duty cycle 1:8 T_{CASE} = +25 °C P_{IN} = 4 dBm	—	49	—	
Harmonics 2nd	$2f_0$	BW = 3 MHz 5 dBm $\leq P_{OUT} \leq$ 32 dBm	—	—	−5	dBm
3rd to 7th	$3f_0$ to $7f_0$	0 °C $\leq T_{CASE} \leq$ +90 °C 2.9 V $\leq V_{CC} \leq$ 4.0 V	—	—	−7	
Output power	P_{OUT}	V_{CC} = 3.5 V $V_{APC} \approx$ 2.0 V T_{CASE} = +25 °C	32.0	32.5	—	dBm
	P_{OUT_MAX}	V_{CC} = 3.5 V $V_{APC} \approx$ 2.0 V T_{CASE} = +25 °C P_{IN} = 4 dBm	—	32.1	—	
	P_{OUT_MAX}	V_{CC} = 2.9 V $V_{APC} \leq$ 2.6 V T_{CASE} = −20 °C to +100 °C (See Table 2 for multislot) P_{IN} = 6 dBm	29.5	30.5	—	
	P_{OUT_MAX}	V_{CC} = 4.8 V $V_{APC} \leq$ 2.6 V T_{CASE} = −20 °C to +100 °C (See Table 2 for multislot) P_{IN} = 6 dBm	29.5	30.5	—	

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Table 3. CX77304-17 Electrical Specifications [1] (4 of 6)

DCS1800 Mode (f = 1710 to 1785 MHz and P_{IN} = 6 to 11 dBm) [continued]						
Parameter	**Symbol**	**Test Condition**	**Minimum**	**Typical**	**Maximum**	**Units**
Input VSWR	Γ_{IN}	P_{OUT} = 0 to 32 dBm controlled by V_{APC}	—	—	2:1	—
Forward isolation	$P_{OUT\_STANDBY}$	P_{IN} = 10 dBm V_{APC} = 0.3 V	—	–40	–35	dBm
Switching time	τ_{RISE}, τ_{FALL}	Time from P_{OUT} = –10 dBm to P_{OUT} = 0 dBm $\tau \approx$ 90%	—	10	12	µs
		Time from P_{OUT} = –10 dBm to P_{OUT} = +20 dBm $\tau \approx$ 90%	—	5	8	
		Time from P_{OUT} = –10 dBm to P_{OUT} = +32 dBm $\tau \approx$ 90%	—	2	5	
Spurious	Spur	All combinations of the following parameters: V_{APC} = controlled [3] P_{IN} = min. to max. V_{CC} = 2.9 V to 4.8 V Load VSWR = 8:1, all phase angles	No parasitic oscillation > –36 dBm			
Load mismatch	Load	All combinations of the following parameters: V_{APC} = controlled [3] P_{IN} = min. to max. V_{CC} = 2.9 V to 4.8 V Load VSWR = 10:1, all phase angles	No module damage or permanent degradation			
Noise power	P_{NOISE}	At f_0 + 20 MHz RBW = 100 kHz V_{CC} = 3.5 V 5 dBm $\leq P_{OUT} \leq$ 32 dBm	—	—	–80	dBm
		At 925 to 960 MHz RBW = 100 kHz V_{CC} = 3.5 V 5 dBm $\leq P_{OUT} \leq$ 32 dBm	—	—	–95	

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Table 3. CX77304-17 Electrical Specifications [1] (5 of 6)

PCS1900 Mode (f = 1850 to 1910 MHz and P_{IN} = 6 to 11 dBm)						
Parameter	Symbol	Test Condition	Minimum	Typical	Maximum	Units
Frequency range	f	—	1850	—	1910	MHz
Input power	P_{IN}	—	6	—	11	dBm
Analog power control voltage	V_{APC}	P_{OUT} = 29.5 dBm	1.35	1.7	2.1	V
Power Added Efficiency	PAE	V_{CC} = 3.5 V $P_{OUT} \geq$ 32 dBm $V_{APC} \approx$ 2.0 V pulse width 577 µs duty cycle 1:8 T_{CASE} = +25 °C	45	50	—	%
	$PAE_{LOW\ INPUT}$	V_{CC} = 3.5 V $P_{OUT} \geq$ 32 dBm $V_{APC} \approx$ 2.0 V pulse width 577 µs duty cycle 1:8 T_{CASE} = +25 °C P_{IN} = 4 dBm	—	44.5	—	
Harmonic 2nd to 7th	$2f_0$ to $7f_0$	BW = 3 MHz 5 dBm $\leq P_{OUT} \leq$ 32 dBm	—	—	–7	dBm
Output power	P_{OUT}	V_{CC} = 3.5 V $V_{APC} \approx$ 2.0 V T_{CASE} = +25 °C	32.0	32.5	—	dBm
	P_{OUT_MAX}	V_{CC} = 3.5 V $V_{APC} \approx$ 2.0 V T_{CASE} = +25 °C P_{IN} = 4 dBm	—	32.3	—	
	P_{OUT_MAX}	V_{CC} = 2.9 V $V_{APC} \leq$ 2.6 V T_{CASE} = –20 °C to +100 °C (See Table 2 for multislot) P_{IN} = 6 dBm	29.5	30.5	—	
	P_{OUT_MAX}	V_{CC} = 4.8 V, $V_{APC} \leq$ 2.6 V T_{CASE} = –20 °C to +100 °C (See Table 2 for multislot) P_{IN} = 6 dBm	29.5	30.5	—	
Input VSWR	Γ_{IN}	P_{OUT} = 0 to 32 dBm controlled by V_{APC}	—	—	2.2:1	—
Forward isolation	$P_{OUT\_STANDBY}$	P_{IN} = 10 dBm V_{APC} = 0.3 V	—	–40	–35	dBm
Switching time	τ_{RISE}, τ_{FALL}	Time from P_{OUT} = –10 dBm to P_{OUT} = 0 dBm $\tau \approx$ 90%	—	10	12	µs
		Time from P_{OUT} = –10 dBm to P_{OUT} = +20 dBm $\tau \approx$ 90%	—	5	8	
		Time from P_{OUT} = –10 dBm to P_{OUT} = +32 dBm $\tau \approx$ 90%	—	2	5	

Table 3. CX77304-17 Electrical Specifications [1] (6 of 6)

Parameter	Symbol	Test Condition	Minimum	Typical	Maximum	Units
Spurious	Spur	All combinations of the following parameters: V_{APC} = controlled [3] P_{IN} = min. to max. V_{CC} = 2.9 V to 4.8 V Load VSWR = 8:1, all phase angles	No parasitic oscillation > −36 dBm			
Load mismatch	Load	All combinations of the following parameters: V_{APC} = controlled [3] P_{IN} = min. to max. V_{CC} = 2.9 V to 4.8 V Load VSWR = 10:1, all phase angles	No module damage or permanent degradation			
Noise power	PNOISE	At f_0 + 20 MHz RBW = 100 kHz V_{CC} = 3.5 V 5 dBm ≤ P_{OUT} ≤ 32 dBm	—	—	−77	dBm
		At 869 to 894 MHz RBW = 100 kHz V_{CC} = 3.5 V 5 dBm ≤ P_{OUT} ≤ 32 dBm	—	—	−95	

PCS1900 Mode (f = 1850 to 1910 MHz and PIN = 6 to 11 dBm) [continued]

[1] Unless specified otherwise: T_{CASE} = −20 °C to max. operating temperature (see Table 2), RL = 50 Ω, pulsed operation with pulse width ≤ 2308 μs and duty cycle ≤ 4:8, V_{CC} = 2.9 V to 4.8 V.

[2] I_{CC} = 0A to xA, where x = current at P_{OUT} = 34.5 dBm, 50 Ω load, and V_{CC} = 3.5 V.

[3] I_{CC} = 0A to xA, where x = current at P_{OUT} = 32.0 dBm, 50 Ω load, and V_{CC} = 3.5 V.
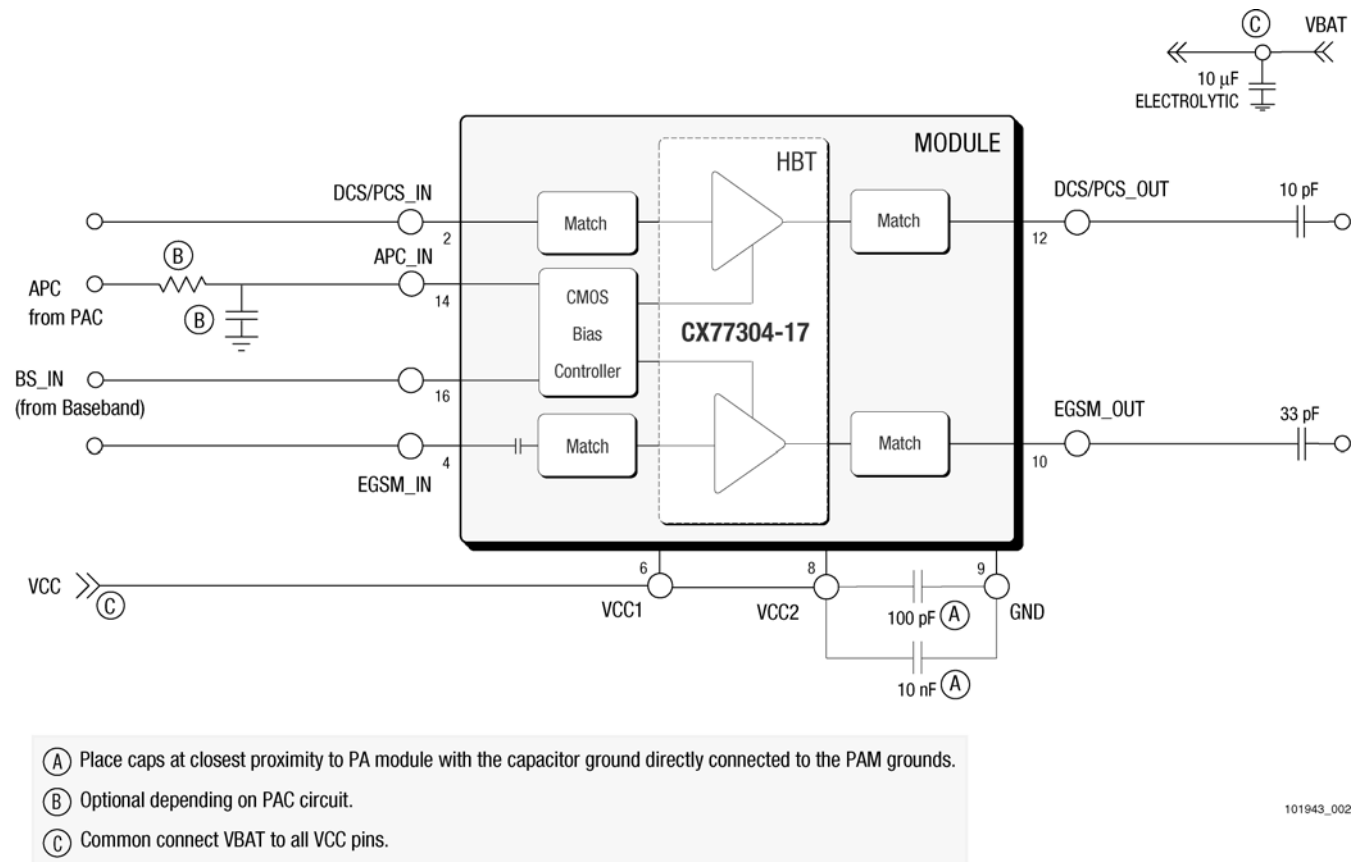
Figure 2. Typical CX77304-17 PAM Application

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Package Dimensions and Pin Descriptions

Figure 3 is a mechanical diagram of the pad layout for the 16-pin leadless CX77304-17 tri-band PA module. Figure 4 provides a recommended phone board footprint for the PAM to help the designer attain optimum thermal conductivity, good grounding, and minimum RF discontinuity for the 50-ohm terminals.

Table 4 lists the pin labels and descriptions and Figure 5 shows the device pin configuration and pin numbering, which starts with pin 1 in the upper left, as shown, and increments counter-clockwise around the package. Figure 6 interprets typical case markings.
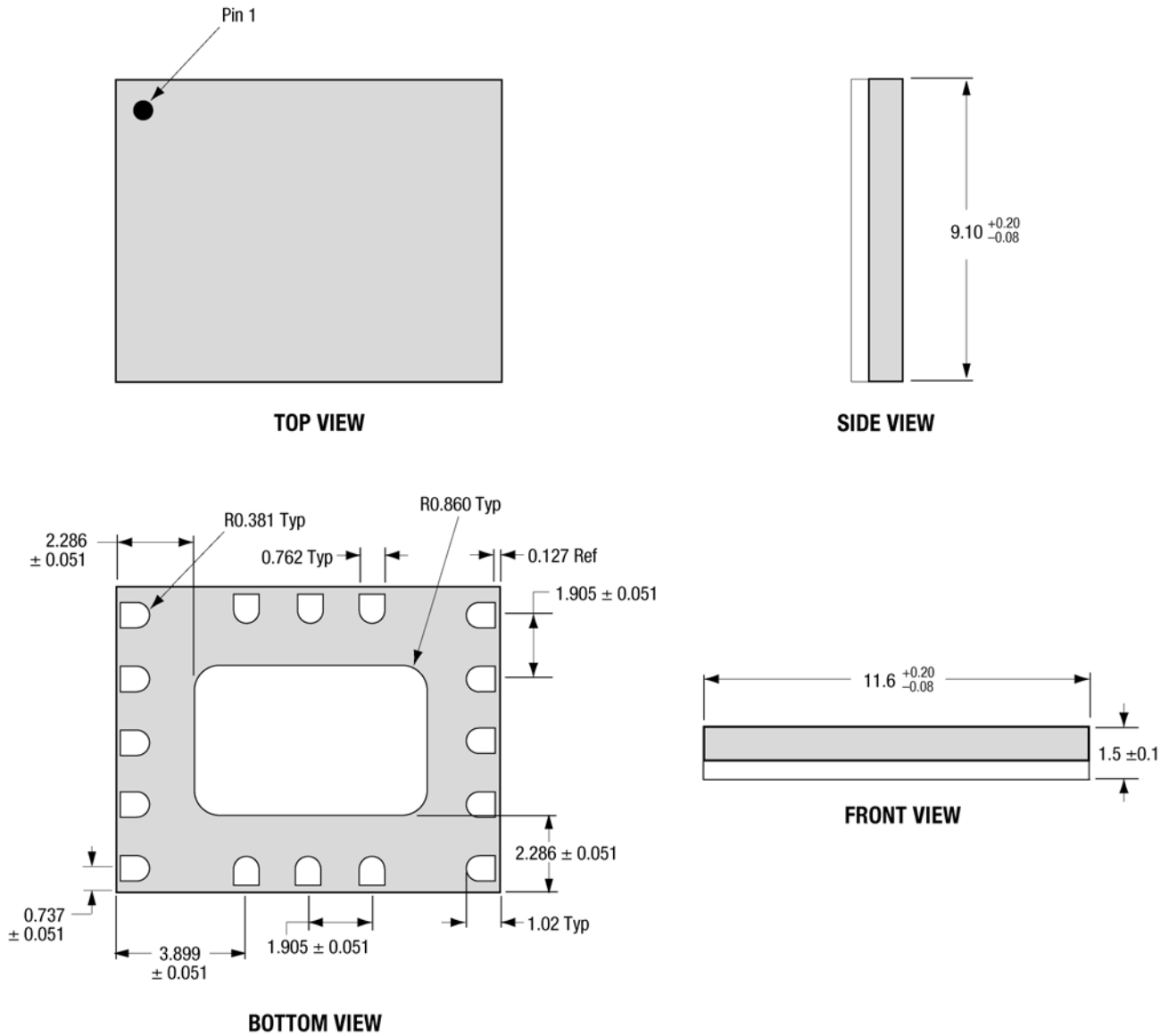
NOTE(S):
1. All contact points are gold plated, lead free-surfaces.
2. All dimensions are in millimeters.

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Figure 3. CX77304-17 PAM Package Dimensions—16-pin Module (All Views)
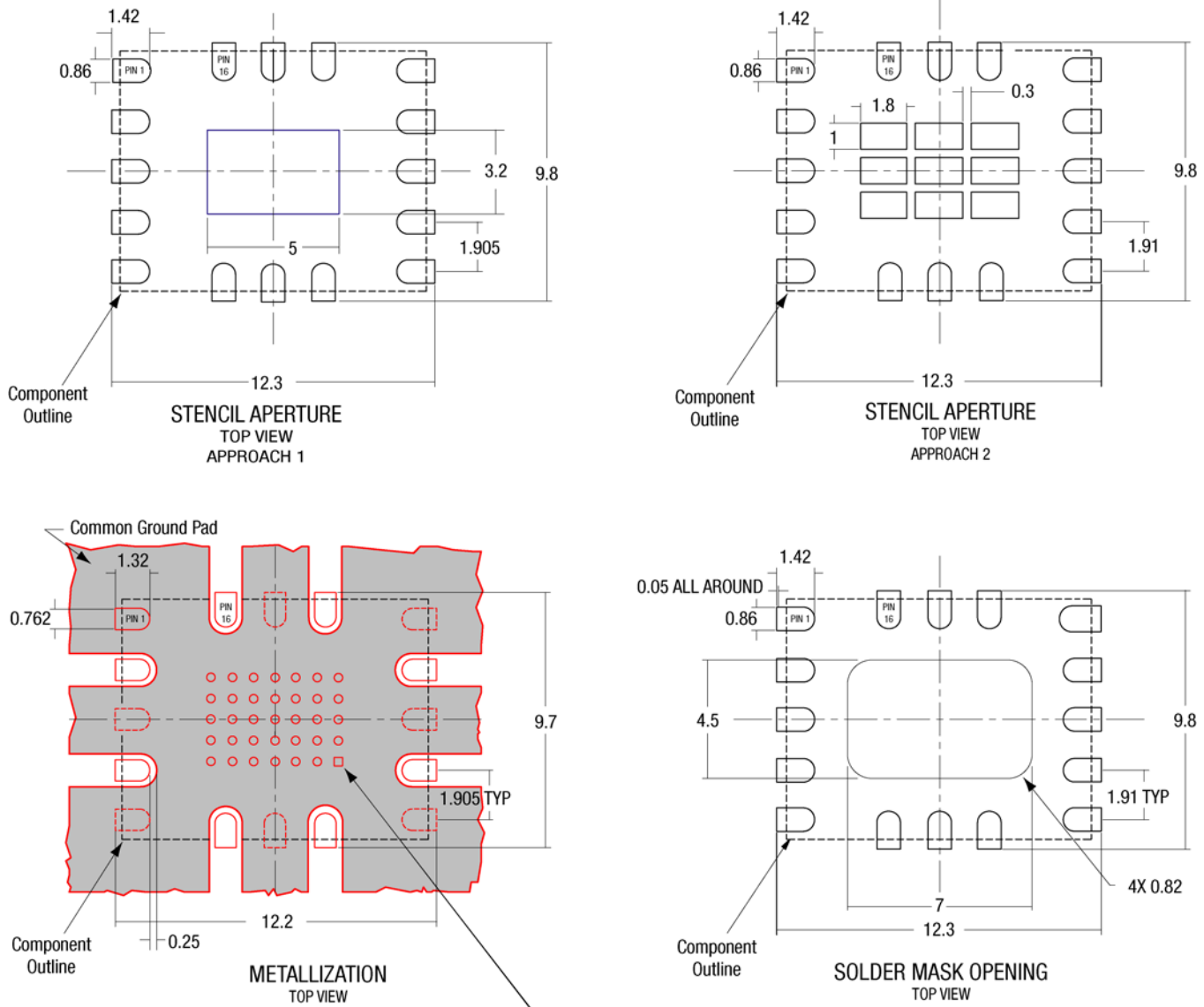
Figure 4. Phone Board Layout Footprint for 9.1 mm x 11.6 mm Package

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Table 4. CX77304-17 Signal Description

Pin	Name	Description	Pin	Name	Description
1	GND	Ground	9	GND	Ground
2	DCS/PCS_IN	RF input to DCS/PCS PA	10	EGSM_OUT	EGSM RF output (DC coupled)
3	GND	Ground	11	GND	Ground
4	EGSM_IN	RF input to EGSM PA	12	DCS/PCS_OUT	DCS/PCS RF output (DC coupled)
5	GND	Ground	13	GND	Ground
6	VCC1	Power supply for PA driver stages	14	APC	Analog Power Control
7	GND	Ground	15	GND	Ground
8	VCC2	Power supply for PA output stages	16	BS	Band Select
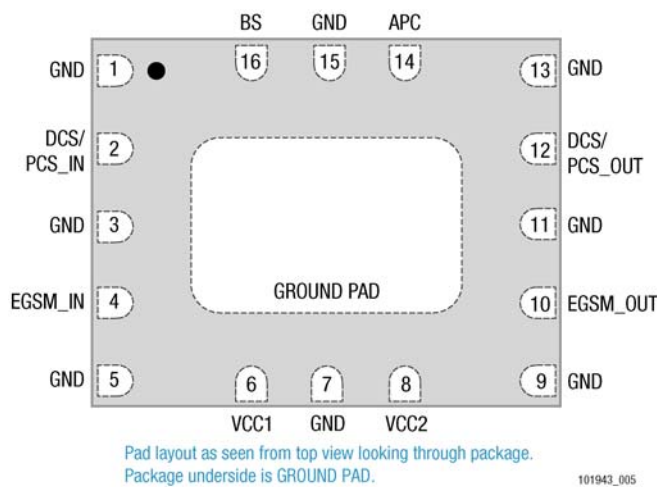
Figure 5. CX77304-17 Pin Configuration—16-Pin Leadless PAM (Top View)

Figure 6. Typical Case Markings

Package and Handling Information

Because of its sensitivity to moisture absorption, this device package is baked and vacuum packed prior to shipment. Instructions on the shipping container label must be followed regarding exposure to moisture after the container seal is broken, otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The CX77304-17 is capable of withstanding an MSL 3/240 °C solder reflow. Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. If the part is attached in a reflow oven, the temperature ramp rate should not exceed 5 °C per second; maximum temperature should not exceed 240 °C. If the part is manually attached, precaution should be taken to insure that the part is not subjected to temperatures exceeding 240 °C for more than 10 seconds. For details on both attachment techniques, precautions, and handling procedures recommended by Skyworks, please refer to *Skyworks Application Note: PCB Design and SMT Assembly/Rework, Document Number 101752*.

Additional information on standard SMT reflow profiles can also be found in the *JEDEC Standard J–STD–020*.

Production quantities of this product are shipped in the standard tape-and-reel format. For packaging details, refer to *Skyworks Application Note: Tape and Reel, Document Number 101568.*

Electrostatic Discharge Sensitivity

The CX77304-17 is a Class I device. Figure 7 lists the Electrostatic Discharge (ESD) immunity level for each pin of the CX77304-17 product. The numbers in Figure 7 specify the ESD threshold level for each pin where the I-V curve between the pin and ground starts to show degradation. The ESD testing was performed in compliance with MIL-STD-883E Method 3015.7 using the Human Body Model. If ESD damage threshold magnitude is found to consistently exceed 2000 volts on a given pin, this so is indicated. If ESD damage threshold below 2000 volts is measured for either polarity, numbers are indicated that represent worst case values observed in product characterization.
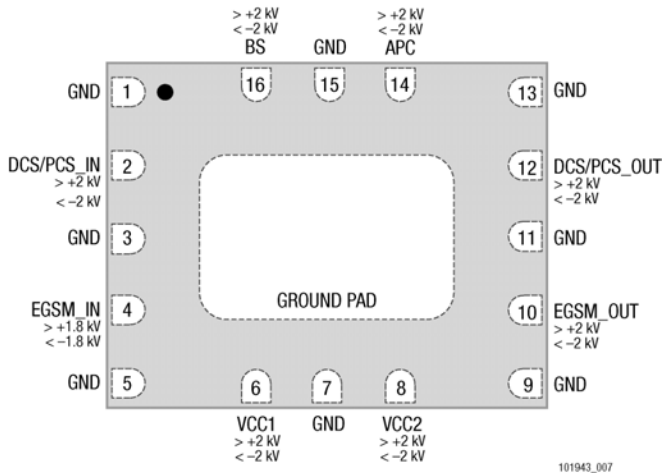
Figure 7. ESD Sensitivity Areas

Various failure criteria can be utilized when performing ESD testing. Many vendors employ relaxed ESD failure standards, which fail devices only after "the pin fails the electrical specification limits" or "the pin becomes completely non-functional". Skyworks employs most stringent criteria, fails devices as soon as the pin begins to show any degradation on a curve tracer.

To avoid ESD damage, latent or visible, it is very important the Class-1 ESD handling precautions listed below are observed in the product assembly and test areas.

- Personnel Grounding
  - Wrist Straps
  - Conductive Smocks, Gloves and Finger Cots
  - Antistatic ID Badges

- Facility
  - Relative Humidity Control and Air Ionizers
  - Dissipative Floors (less than 10^9 Ω to GND)

- Protective Workstation
  - Dissipative Table Tops
  - Protective Test Equipment (Properly Grounded)
  - Grounded Tip Soldering Irons
  - Conductive Solder Suckers
  - Static Sensors

- Protective Packaging & Transportation
  - Bags and Pouches (Faraday Shield)
  - Protective Tote Boxes (Conductive Static Shielding)
  - Protective Trays
  - Grounded Carts
  - Protective Work Order Holders

Technical Information

CMOS Bias Controller Characteristics

The CMOS die within the PAM performs several functions that are important to the overall module performance. Some of these functions must be considered for development of the power ramping features in a 3GPP compliant transmitter power control loop. Power ramping considerations will be discussed later in this section.

NOTE: Please refer to 3GPP TS 05.05, Digital Cellular Communications System (Phase 2+); Radio Transmission and Reception. All GSM specifications are now the responsibility of 3GPP. The standards are available at http://www.3GPP.org/specs/specs.htm

The four main functions described in this section are Standby Mode Control, Band Select, Voltage Clamp, and Current Buffer. The functional block diagram is shown in Figure 8.
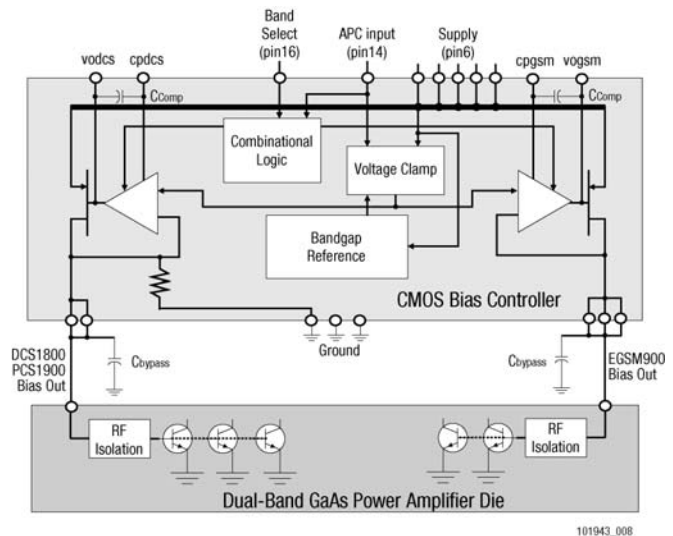
Figure 8. Functional Block Diagram

Standby Mode Control

The Combinational Logic cell includes enable circuitry that monitors the APC ramping voltage from the power amplifier controller (PAC) circuit in the GSM transmitter. Typical handset designs directly connect the PA V_{CC} to the battery at all times, and for some PA manufacturers this requires a control signal to set the device in or out of standby mode. The Skyworks PAM does not require a Transmit Enable input because it contains a standby detection circuit that senses the V_{APC} to enable or disable the PA. This feature helps minimize battery discharge when the PA is in standby mode. When V_{APC} is below the enable threshold voltage, the PA goes into a standby mode, which reduces battery current (I_{CC}) to 6 μA, typical, under nominal conditions.

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For voltages less than 700 mV at the APC input (pin 14), the PA bias is held at ground. As the APC input exceeds the enable threshold, the bias will activate. After an 8 μs delay, the amplifier internal bias will ramp quickly to match the ramp voltage applied to the APC input. In order for the internal bias to precisely follow the APC ramping voltage, it is critical that a ramp pedestal is set to the APC input at or above the enable threshold level with a timing at least 8 μs prior to ramp-up. This will be discussed in more detail in the following section, "Power Ramping Considerations for 3GPP Compliance".

Band Select

The Combinational Logic cell also includes a simple gate arrangement that selects the desired operational band by activating the appropriate current buffer. The voltage threshold level at the Band Select input (pin 16) will determine the active path of the bias output to the GaAs die.

Voltage Clamp

The Voltage Clamp circuit will limit the maximum bias voltage output applied to the bases of the HBT devices on the GaAs die. This provides protection against electrical overstress (EOS) of the active devices during high voltage and/or load mismatch conditions. Figure 9 shows the typical transfer function of the APC input to buffer output under resistively loaded conditions. Notice the enable function near 600 mV, and the clamp acting at 2.15 V, corresponding to a supply voltage of 4.0 V.
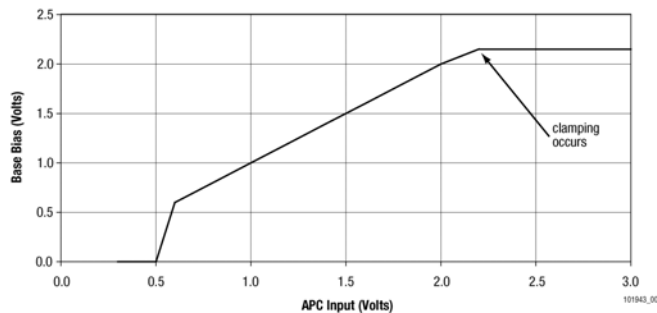
Figure 9. Base Bias Voltage vs. APC Input, VCC = 4.0 V

Due to output impedance effects, the bias of the GaAs devices increases as the supply voltage increases. The Voltage Clamp is designed to gradually decrease in level as the battery voltage increases. The performance of the clamp circuit is enhanced by the band gap reference that provides a supply-, process-, and temperature-independent reference voltage. The transfer function relative to V$_{BAT}$ is shown in Figure 10. For battery voltages below 3.4 V, the base bias voltage is limited by the common mode range of the buffer amplifier. For battery voltages above 3.4 V, the clamp limits the base bias.
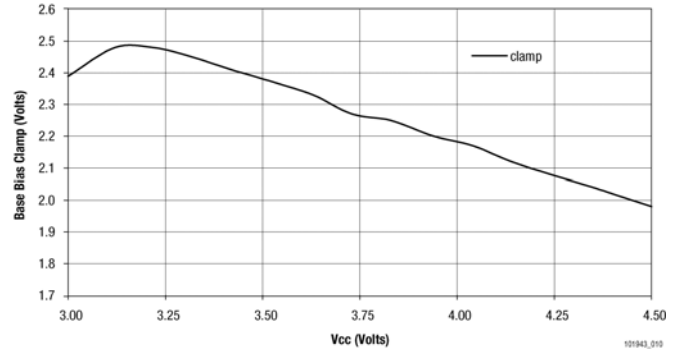
Figure 10. Base Bias Clamp Voltage vs. Supply Voltage

Current Buffer

The output buffer amplifier performs a vital function in the CMOS device by transferring the APC input voltage ramp to the base of the GaAs power devices. This allows the APC input to be a high impedance port, sinking only 10 μA, typical, assuring no loading effects on the PAC circuit. The buffers are designed to source the high GaAs base currents required, while allowing a settling time of less than 8 μs for a 1.5 V ramp.

Power Ramping Considerations for 3GPP Compliance

The primary variables in the power control loop that the system designer must control are:

- Software control of the DSP / DAC

- Software control of the transmitter timing signals

- Ramp profile attributes - pedestal, number of steps, duration of steps

- Layout of circuit / parasitics

- RC time constants within the PAC circuit design

All of these variables will directly influence the ability of a GSM transmitter power control loop to comply with 3GPP specifications.

Although there is a specific time mask template in which the transmitter power is allowed to ramp up, the method is very critical. The 3GPP system specification for switching transients results in a requirement to limit the edge rate of output power transitions of the mobile. Switching transients are caused by the transition from minimum output power to the desired output power, and vice versa. The spectrum generated by this transition is due to the ramping waveform amplitude modulation imposed on the carrier. Sharper transitions tend to produce more spectral "splatter" than smooth transitions. If the transmit output power is ramped up too slowly, the radio will violate the time mask specification. In this condition, the radio may not successfully initiate or maintain a phone call. If the transmit output power is ramped up too quickly, this will cause RF "splatter" at certain frequency offsets from the carrier as dictated by the 3GPP specification. This splatter, known as Output RF Spectrum (ORFS)

due to Switching Transients, will increase the system noise level, which may knock out other users on the system. The main difficulty with TDMA power control is allowing the transmitter to ramp the output power up and down gradually so switching transients are not compromised while meeting the time mask template at all output power levels in all operational bands. The transmitter has 28 µs to ramp up power from an off state to the desired power level.

The GSM transmitter power control loop generally involves feedback around the GaAs PA, which limits the bandwidth of signals that can be applied to the PA bias input. Since the PA is within the feedback loop, its own small-signal frequency response must exhibit a bandwidth 5 to 10 times that of the power control loop. As discussed in the previous section, the PA bias is held at ground for inputs less than 700 mV. As the APC input exceeds the enable threshold, the bias will activate. After an 8 µs delay, the amplifier internal bias will quickly ramp to match the ramp voltage applied to the V_{APC} input. Since the bias must be wide band relative to the power control loop, the ramp will exhibit a fast edge rate. If the APC input increases beyond 1 V before the 8 µs switching delay is allowed to occur after the bias is enabled, the PA will have significant RF output as the internal bias approaches the applied bias. During this ramp, the internal power control is running "open loop" and the edge rates are defined by the frequency response of the PA bias rather than that of the power control loop. This open loop condition will result in switching transients that are directly correlated to the PA bias bandwidth.

Application of an initial APC voltage, which enables the bias at least 8 µs before the V_{APC} voltage is ramped, will ensure that the internal bias of the PAM will directly follow the applied V_{APC}. As a result, the power control loop will define all edge transitions rather than the PA internal bandwidth defining the transition. Figure 11 and Figure 12 show the relationships of the internal bias relative to the applied APC in two cases. One case has ramping starting from ground; the other case has ramping starting with an initial enable pedestal of 700 mV. It is evident that the pedestal level is critical to ensure a predictable and well behaved power control loop.

To enable the CMOS driver in the PAM prior to ramp-up, a PAC output pedestal level to the APC input of the PAM (pin 14) should be set to about 700 mV. This pedestal level should have a duration of at least 8 ms directly prior to the start of ramp up.

Figure 13 shows typical signals and timings measured in a GSM transmitter power control loop. This particular example is at GSM Power Level 5, Channel 62. The oscilloscope traces are TxVCO_enable, PAC_enable, DAC Ramp, and V_{APC} (pin 14).

NOTE: When the TxVCO is enabled, the pedestal becomes set at the APC input of the PAM, then the PAC is enabled, and finally the DAC ramp begins.

The device specifications for enable threshold level and switching delay are shown in Table 3.
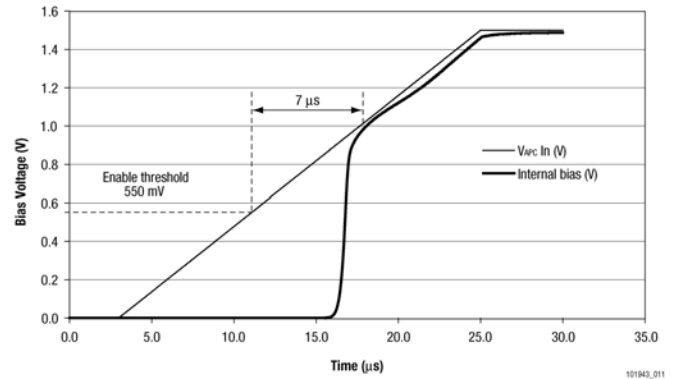

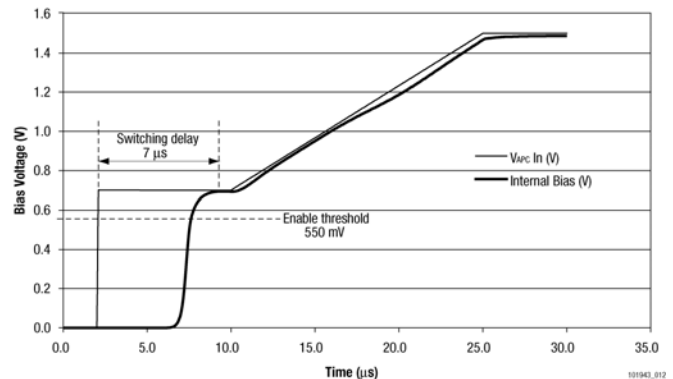Figure 11. PAM Internal Bias Performance—No Pedestal Applied

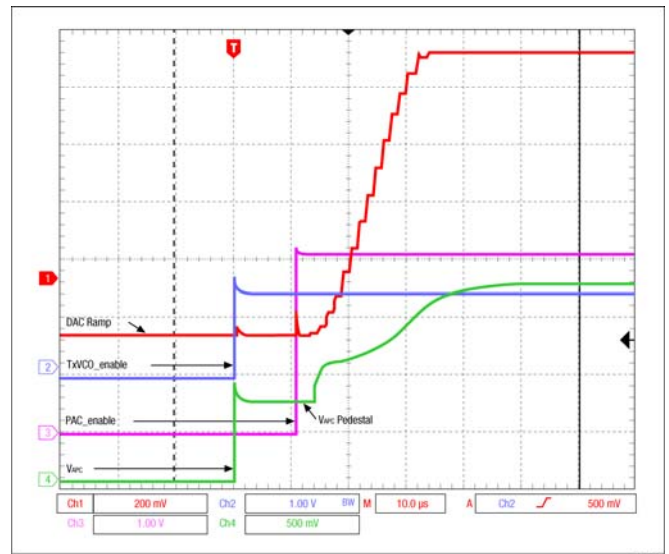Figure 12. PAM Internal Bias Performance—Pedestal Applied

Figure 13. GSM Transmitter – Typical Ramp-up Signals

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Ordering Information

Model Number	Manufacturing Part Number	Product Revision	Package	Operating Temperature
CX77304-17	CX77304-17	17	9.1 x 11.6 x 1.5 mm	−20 °C to +100 °C

Revision History

Revision	Level	Date	Description
A		September 19, 2003	Initial Release
B		July 29, 2004	Revise: Figure 3 <changed thickness dimension from "1.50 mm max." to "1.5 ±0.1 mm" >

References

Application Note: Tape and Reel, Document Number 101568

Application Note: PCB Design and SMT Assembly/Rework, Document Number 101752

JEDEC Standard J-STD-020