SONY

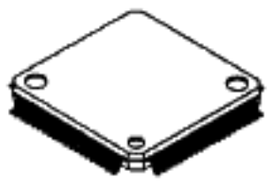
CXD2531BR

ATRAC Encoder/Decoder

Description

The CXD2531BR is an ATRAC processing LSI. ATRAC (adaptive transform acoustic coding) is a technique for compressing sound featured by MiniDisc recorders. By combining this LSI with the CXD2525 MiniDisc encoder/decoder processing LSI and the CXD2526 shock-proof control LSI, real-time processing for band compression/expansion can be performed.

80 pin LQFP (Plastic)



Features

- Two-channel ATRAC processing on a single chip
- Supports error processing for playback data
- Low power consumption

Structure

Silicon gate CMOS IC

Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{DD}	Vss–0.5 to +7.0	V
• Input voltage	V_I	Vss–0.5 to V_{DD}+0.5	V
• Output voltage	V_O	Vss–0.5 to V_{DD}+0.5	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–55 to +150	°C

Recommended Operating Conditions

• Supply voltage	V_{DD}	+3.0 to +5.5	V
• Operating temperature	Topr	–20 to +75	°C

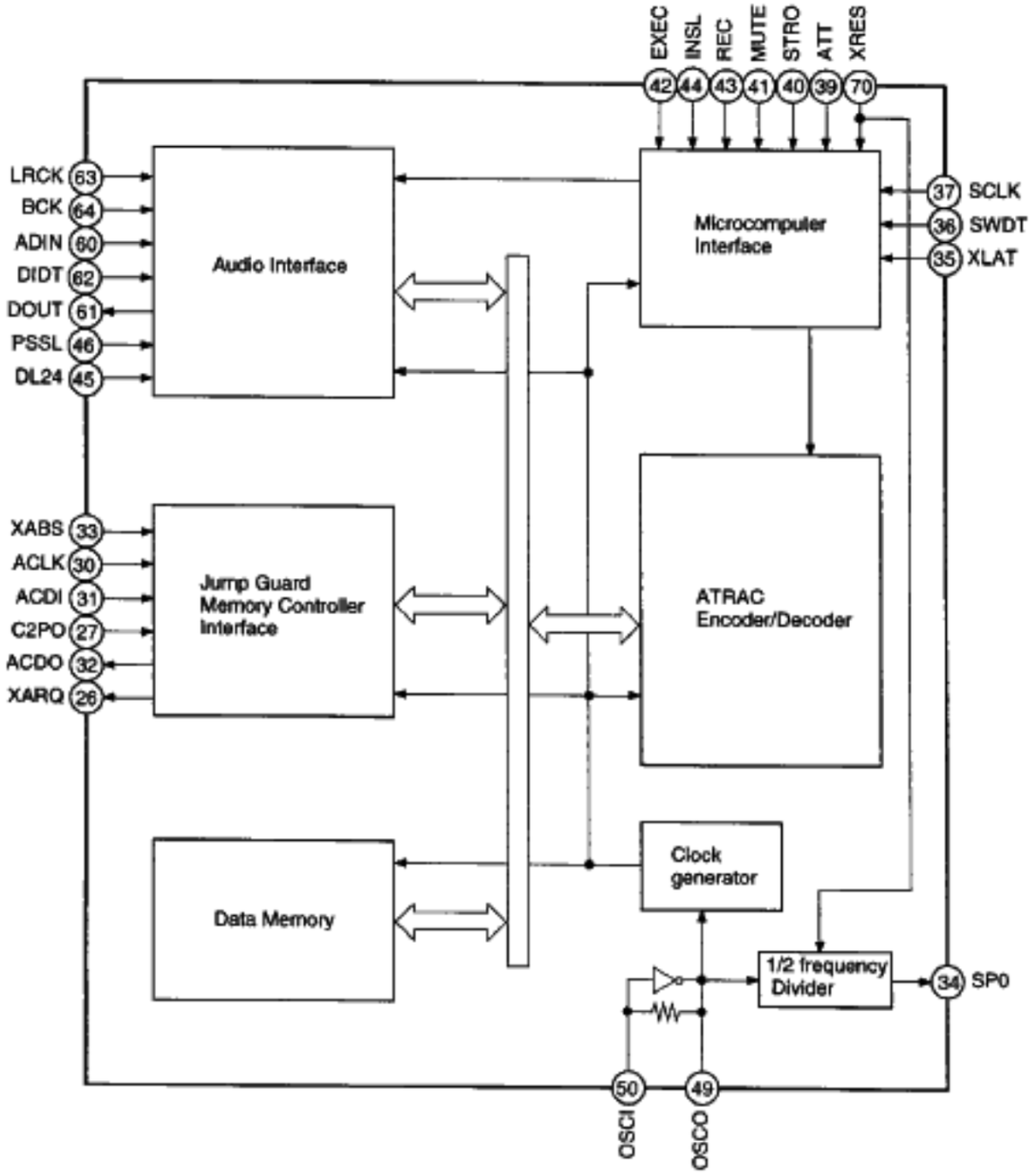
Input/Output Capacitances

• Input capacitance	C_I	9 (max.)	pF	
• Input/output capacitances	$C_{I/O}$	11 (max.)	pF	for high impedance

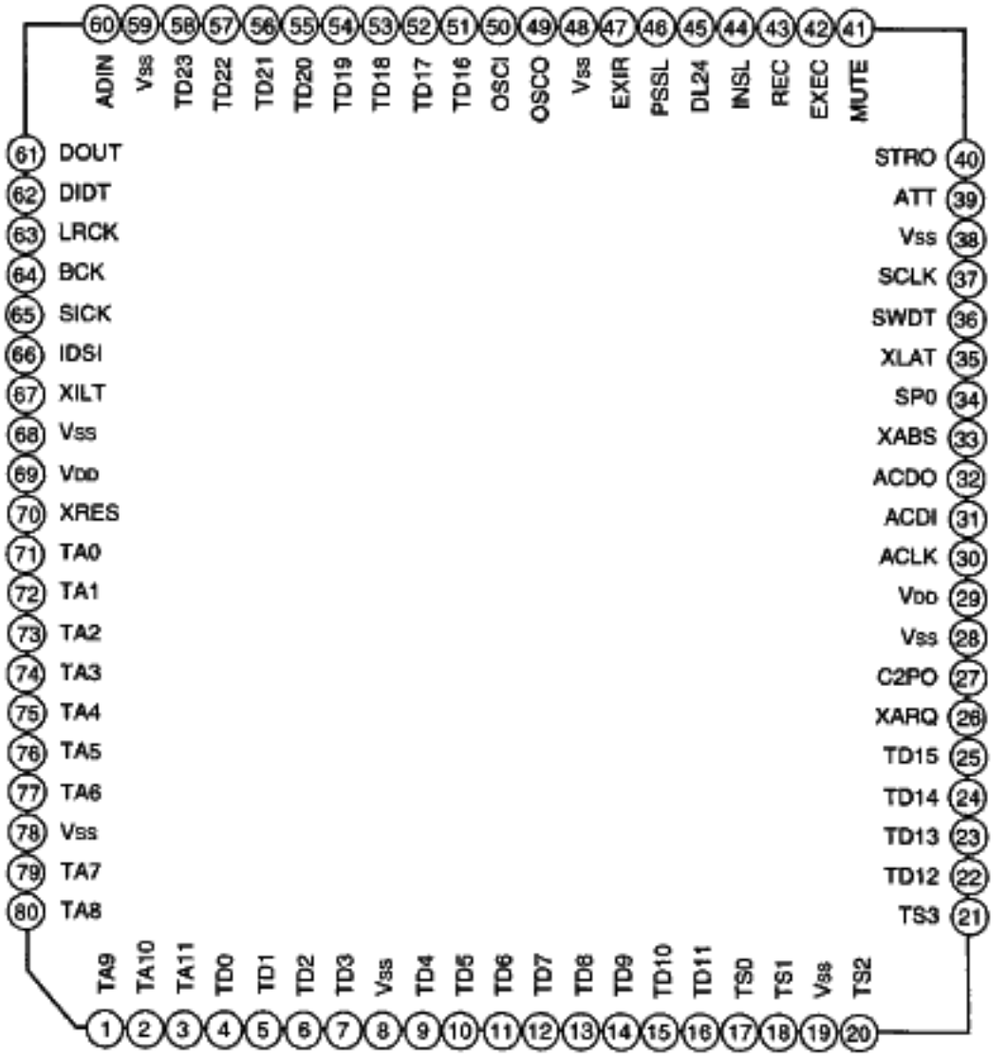
Note) Measurement conditions $V_{DD}=V_I=0V$
f_M=1MHz

E93Y27-PK

Block Diagram



Pin Configuration



Pin Description

Pin No.	Symbol	I/O	Description
1	TA9	I	Test; connect to GND.
2	TA10	I	Test; connect to GND.
3	TA11	I	Test; connect to GND.
4	TD0	I	Test; connect to GND.
5	TD1	I	Test; connect to GND.
6	TD2	I	Test; connect to GND.
7	TD3	I	Test; connect to GND.
8	Vss	—	GND
9	TD4	I	Test; connect to GND.
10	TD5	I	Test; connect to GND.

Pin No.	Symbol	I/O	Description
11	TD6	I	Test; connect to GND.
12	TD7	I	Test; connect to GND.
13	TD8	I	Test; connect to GND.
14	TD9	I	Test; connect to GND.
15	TD10	I	Test; connect to GND.
16	TD11	I	Test; connect to GND.
17	TS0	I	Test; connect to GND.
18	TS1	I	Test; connect to GND.
19	Vss	—	GND
20	TS2	I	Test; connect to GND.
21	TS3	I	Test; connect to GND.
22	TD12	I	Test; connect to GND.
23	TD13	I	Test; connect to GND.
24	TD14	I	Test; connect to GND.
25	TD15	I	Test; connect to GND.
26	XARQ	O	Data transfer request to the CXD2526
27	C2PO	I	Input data error status from the CXD2526
28	Vss	—	GND
29	VDD	—	Power supply
30	ACLK	I	Serial transfer clock input (128Fs) from the CXD2526
31	ACDI	I	Data input from the CXD2526
32	ACDO	O	Data output to the CXD2526
33	XABS	I	Serial transfer sync pulse input from the CXD2526
34	SP0	O	Clock output of oscillation clock divided by 2 (512Fs). The duty is not guaranteed.
35	XLAT	I	Latch pulse input for serial microcomputer interface (active at Low)
36	SWDT	I	Data input for serial microcomputer interface
37	SCLK	I	Transfer clock input for serial microcomputer interface
38	Vss	—	GND
39	ATT	I	Attenuation setting input (–12dB attenuation at High)*1
40	STRO	I	Stereo/monaural setting input (monaural at High)*1
41	MUTE	I	Mute setting input (mute ON at High)*1
42	EXEC	I	Start/stop setting input (start at High)*1
43	REC	I	Recording/playback setting input (recording at High)*1
44	INSL	I	Recording input selection (DIDT pin at High; ADIN pin at Low)*1
45	DL24	I	Data word length selection (24 bits at High; 16 bits at Low)
46	PSSL	I	ADIN pin frontward/rearward truncation selection (rearward truncation at High)

Pin No.	Symbol	I/O	Description
47	EXIR	I	Test; connect to GND.
48	Vss	—	GND
49	OSCO	O	Crystal oscillation circuit output (1024Fs)*2
50	OSCI	I	Crystal oscillation circuit input (1024Fs)*2
51	TD16	I	Test; connect to GND.
52	TD17	I	Test; connect to GND.
53	TD18	I	Test; connect to GND.
54	TD19	I	Test; connect to GND.
55	TD20	I	Test; connect to GND.
56	TD21	I	Test; connect to GND.
57	TD22	I	Test; connect to GND.
58	TD23	I	Test; connect to GND.
59	Vss	—	GND
60	ADIN	I	Analog recording input (connects the external A/D converter output)
61	DOUT	O	Monitor output (for recording)/decoded audio data output (for playback)
62	DIDT	I	Digital recording input
63	LRCK	I	44.1kHz (Fs) (LRCK input pin)
64	BCK	I	2.8224MHz (64Fs) (BCK input pin)
65	SICK	I	Test; connect to V_{DD}.
66	IDSI	I	Test; connect to V_{DD}.
67	XILT	I	Test; connect to V_{DD}.
68	Vss	—	GND
69	V_{DD}	—	Power supply
70	XRES	I	Reset input (reset at Low)
71	TA0	I	Test; connect to GND.
72	TA1	I	Test; connect to GND.
73	TA2	I	Test; connect to GND.
74	TA3	I	Test; connect to GND.
75	TA4	I	Test; connect to GND.
76	TA5	I	Test; connect to GND.
77	TA6	I	Test; connect to GND.
78	Vss	—	GND
79	TA7	I	Test; connect to GND.
80	TA8	I	Test; connect to GND.

*1 Refer to "1.Microcomputer Interface of Description of Functions".

*2 Feedback resistance included.

Note) Pins 39 to 46 are pulled down in the chip.
Pins 35 to 37 and 70 are pulled up in the chip.

Electrical Characteristics

DC characteristics 1

(V_{DD}=3.0±0.3V, Vss=0V, Topr=–20 to +75°C)

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Applicable pins
Input voltage (1)	High level input voltage	V_{IH} (1)		0.7V_{DD}			V	*1
	Low level input voltage	V_{IL} (1)				0.3V_{DD}	V	
Input voltage (2)	High level input voltage	V_{IH} (2)		1.8			V	All pins except for those listed under *1
	Low level input voltage	V_{IL} (2)				0.5	V	
Output voltage	High level output voltage	V_{OH}	I_{OH}=–1.2mA	V_{DD}–0.8			V	All output pins
	Low level output voltage	V_{OL}	I_{OL}=2.4mA			0.4	V	
Input leak current (1)		I_{LI} (1)	V_I=0 to 3.6V			±10	µA	*2
Input leak current (2)		I_{LI} (2)	V_I=0 to 3.6V			±40	µA	*3
Input leak current (3)		I_{LI} (3)	V_I=Vss	–12	–30	–75	µA	*4
Input leak current (4)		I_{LI} (4)	V_I=V_{DD}	12	30	75	µA	*5

DC characteristics 2

(V_{DD}=5.0±0.5V, Vss=0V, Topr=–20 to +75°C)

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Applicable pins
Input voltage (1)	High level input voltage	V_{IH} (1)		0.7V_{DD}			V	*1
	Low level input voltage	V_{IL} (1)				0.3V_{DD}	V	
Input voltage (2)	High level input voltage	V_{IH} (2)		2.2			V	All pins except for those listed under *1
	Low level input voltage	V_{IL} (2)				0.8	V	
Output voltage	High level output voltage	V_{OH}	I_{OH}=–2.0mA	V_{DD}–0.8			V	All output pins
	Low level output voltage	V_{OL}	I_{OL}=4.0mA			0.4	V	
Input leak current (1)		I_{LI} (1)	V_I=0 to 5.5V			±10	µA	*2
Input leak current (2)		I_{LI} (2)	V_I=0 to 5.5V			±40	µA	*3
Input leak current (3)		I_{LI} (3)	V_I=Vss	–40	–100	–240	µA	*4
Input leak current (4)		I_{LI} (4)	V_I=V_{DD}	40	100	240	µA	*5

Applicable pins

*1 TS0, TS1, TS2, TS3, C2PO, ACLK, ACDI, XABS, DL24, PSSL, EXIR, ADIN, DIDT, LRCK, BCK

*2 C2PO, ACLK, ACDI, XABS, ADIN, DIDT, LRCK, BCK, EXIR

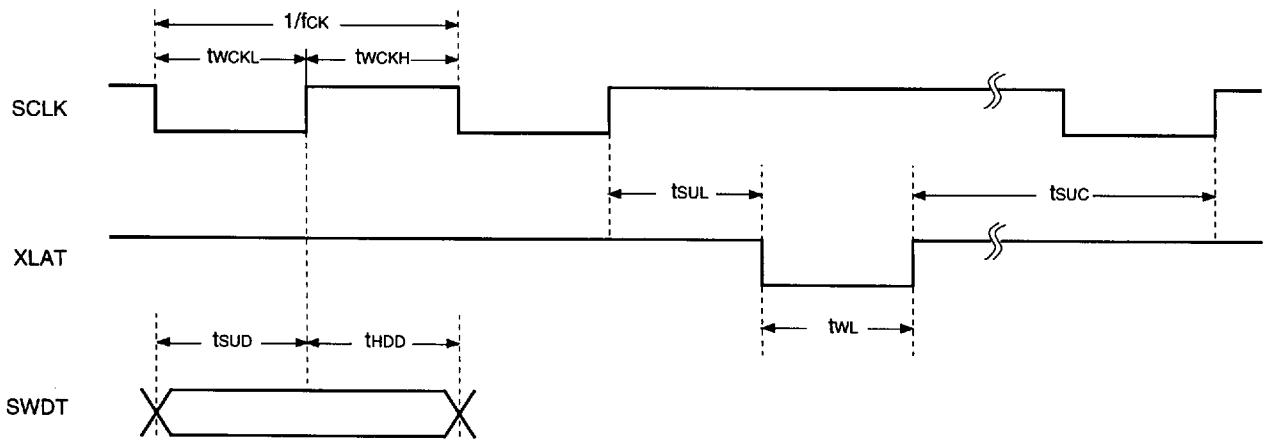
*3 TA0 to 11, TD0 to 23

*4 XLAT, SWDT, SCLK, SICK, IDSI, XILT, XRES

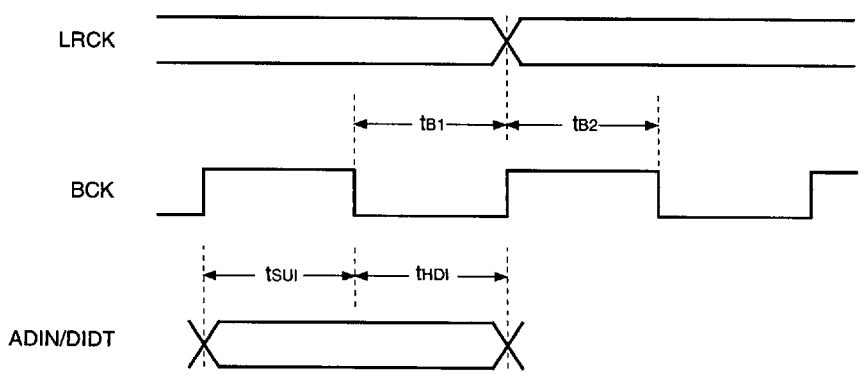
*5 TS0 to 3, ATT, STRO, MUTE, EXEC, REC, INSL, DL24, PSSL

AC characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
SCLK pulse width (Low)	t_{WCKL}	100			ns
SCLK pulse width (High)	t_{WCKH}	100			ns
SCLK frequency	fck			5.0	MHz
XLAT setup time	t_{SUL}	100			ns
XLAT pulse width	t_{WL}	100			ns
SWDT setup time	t_{SUD}	30			ns
SWDT hold time	t_{HDD}	30			ns
SCLK setup time	t_{SUC}	200			ns



Item	Symbol	Min.	Typ.	Max.	Unit
LRCK hold time	t_{B1}	100			ns
LRCK setup time	t_{B2}	100			ns
ADIN/DIDT setup time	t_{SUI}	30			ns
ADIN/DIDT hold time	t_{HDI}	30			ns



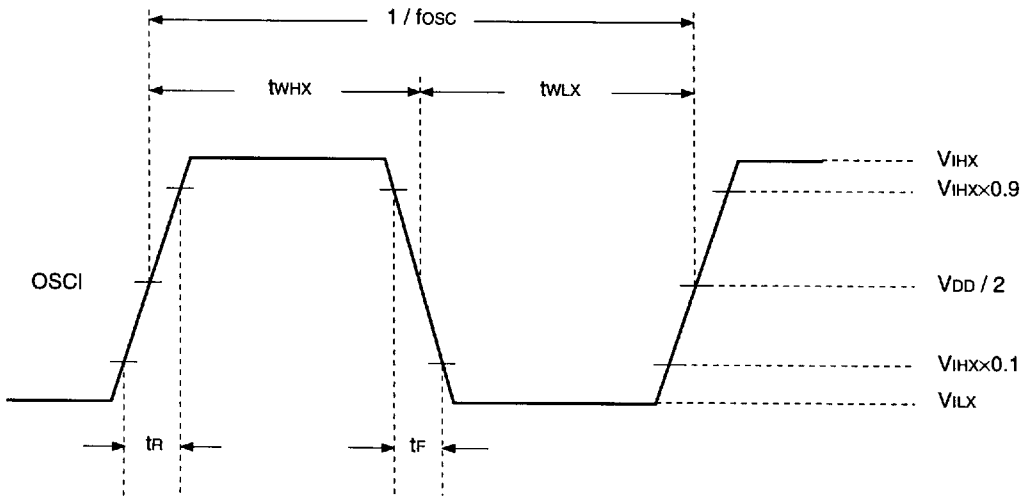
OSCI pin

(1) When self-excited oscillation

Item	Symbol	Min.	Typ.	Max.	Unit
Oscillation frequency	fosc	44.8	45.1584	45.6	MHz

(2) When the pulse is input

Item	Symbol	Min.	Typ.	Max.	Unit
High level pulse width	t_{WHX}	7			ns
Low level pulse width	t_{WLX}	7			ns
Input High level	V_{IHX}	0.7V_{DD}			V
Input Low level	V_{ILX}			0.3V_{DD}	V
Rising time	t_R			7	ns
Falling time	t_F			7	ns



• Be sure to input the pulse to the OSCI pin via an capacitor.

(3) When the sine wave is input to the OSCI pin via an capacitor

(Topr=–20 to +75°C, V_{DD}=3.0 to 5.5V)

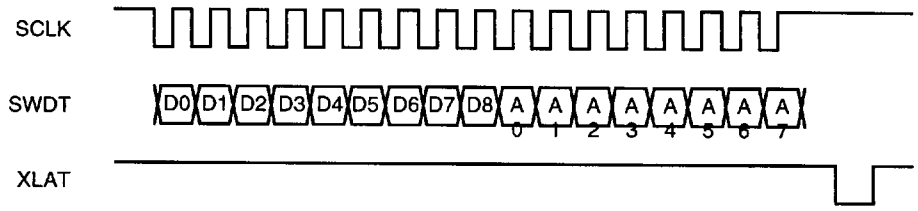
Item	Symbol	Min.	Typ.	Max.	Unit
Input amplitude	V_I	2.0		V_{DD}+0.3	Vp-p

Description of Functions

1. Microcomputer Interface

(1) Mode setting

The CXD2531BR mode setting consists of two systems, one is set directly in parallel from the pins (parallel command) and the other is set through serial input from the SWDT pin (serial command). The timing for the serial input is shown below.

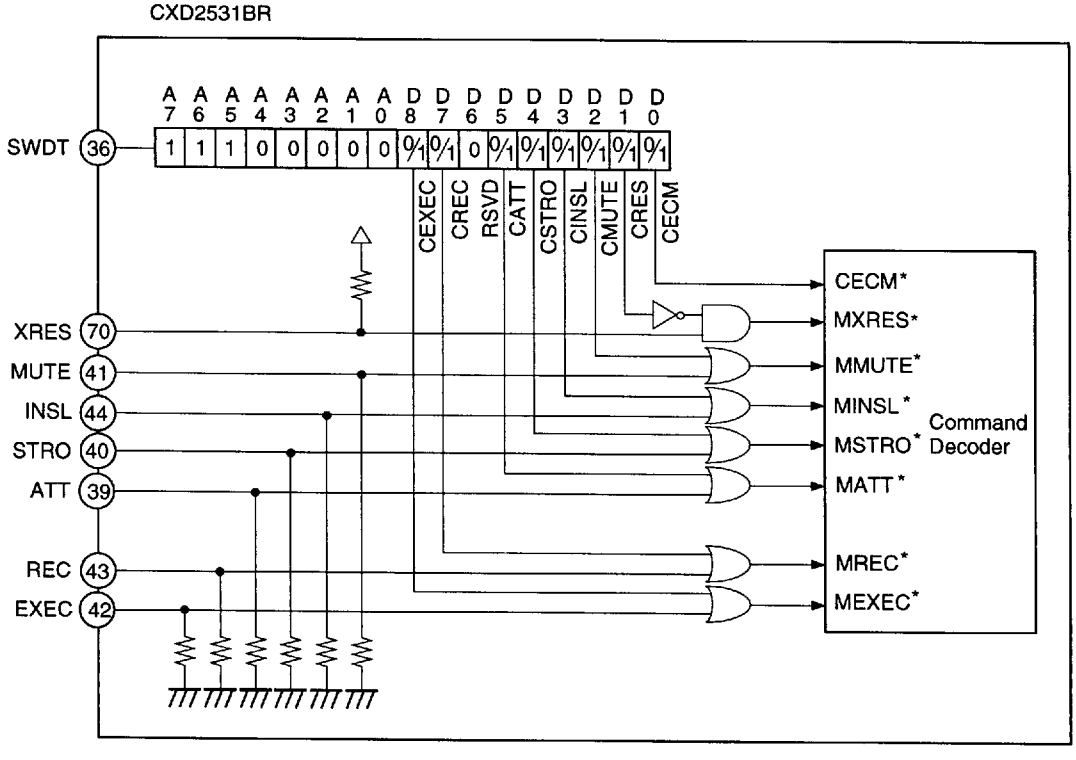


Serial Transfer Timing

Write a 9-bit command followed by the address "E0h" from the SWDT pin and then supply XLAT.

The relationship between the serial commands and the parallel commands is shown below. When using one command, initialize the other; set the XRES pin High when the serial command is used and set the MUTE, INSL, STRO, REC and EXEC pins Low.

Serial command D6 should always be "0".



Relationship of the Serial Command and Parallel Command

* Refer to "Command Table for Mode Setting" for the description of each command on the next page.
* Use the serial command to control MEXEC, MXRES, and MMUTE when start/stop (refer to "Control with the Microcontroller").

The description of each command is as follows.

Command Name	Description of Command		
CECM	Error concealment mode selection command	0	Normal mode
		1	Mute the sound frames that include even one byte of error
MXRES	Reset input	0	Reset off
		1	Reset on
MMUTE	Mute command	0	Mute off
		1	Mute on
MINSL	Audio interface input selection command	0	ADIN pin
		1	DIDT pin
MSTRO	Stereo/monaural selection command	0	Stereo
		1	Monaural
MATT	Attenuation command	0	Attenuation off
		1	Attenuation on (–12dB attenuation)
MREC	Recording/playback selection command	0	Playback (decoder)
		1	Recording (encoder)
MEXEC	Start/stop command	0	Stop
		1	Start

Command Table for Mode Setting

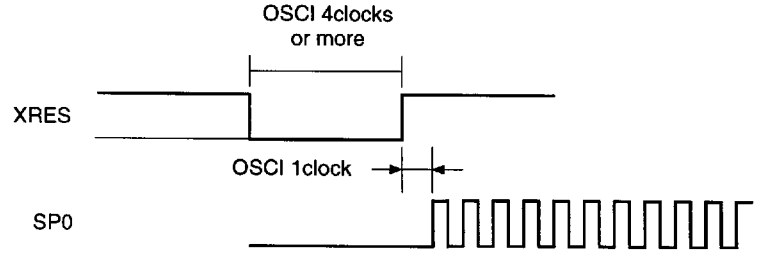
(2) 512Fs clock output and reset

When the chip is reset by setting the XRES pin Low, the 512Fs clock output from the SP0 pin is halted; whereas when the reset is applied by the serial command, the 512Fs clock is not halted. Therefore, when using SP0 (512Fs clock output), use the XRES pin only for the power on reset; afterwards, use the serial command reset.

Reset	SP0 pin output
XRES pin=Low	Fix to Low. (Output is stopped.)
CRES=1	512Fs clock is output. (Outputs regardless of CRES=0/1.)

Reset and SP0 Pin Output

Reset Timing



2. Audio Interface

(1) Recoding interface (Refer to the Audio Interface Timing Charts 1 and 2.)

• Recording input selection and input format setting

The digital interface demodulated input from the CXD2525 (DIDT pin) and the input from the A/D converter (ADIN pin) can be selected as the recording input through either the INSL pin or the serial command CINSL (D3). With ADIN pin input, the data word length can be selected as either 16 bits or 24 bits through the DL24 pin, and frontward truncation or rearward truncation can be selected in the 32-bit slot data through the PSSL pin. However, when the data word length is 24 bits, frontward truncation is selected regardless of the PSSL pin. The DIDT input format is always 16-bit, MSB first, and rearward truncation.

MINSL	DL24	PSSL	Input pin	Input format
1	*	*	DIDT	16 bits, MSB first, rearward truncation
0	1	*	ADIN	24 bits, MSB first, frontward truncation
0	0	1	ADIN	16 bits, MSB first, rearward truncation
0	0	0	ADIN	16 bits, MSB first, frontward truncation

Selection of the Recording Input *...don't care

• Recording Monitor

During recoding, the DOUT pin is for recording monitor; the ADIN/DIDT input data is output as it is without encoding to decoding. (The output format is 16 bits, MSB first and rearward truncation regardless of the setting of the INSL, DL24 and PSSL pins.)

Note that this recording monitor output is output even when the reset is applied using the serial command, but it stops (DOUT output=Low) when the reset is applied using the XRES pin.

• Recording Mute

The MUTE pin or the serial command CMUTE (D2) can be used to mute the recording. During recording, the output data from the ACDO pin is made by encoding the 0 data. However, the recording monitor output from the DOUT pin is not muted.

• Monaural Recording

When monaural recording is selected through the STRO pin or the serial command CSTRO (D4), only the left-channel input data is encoded.

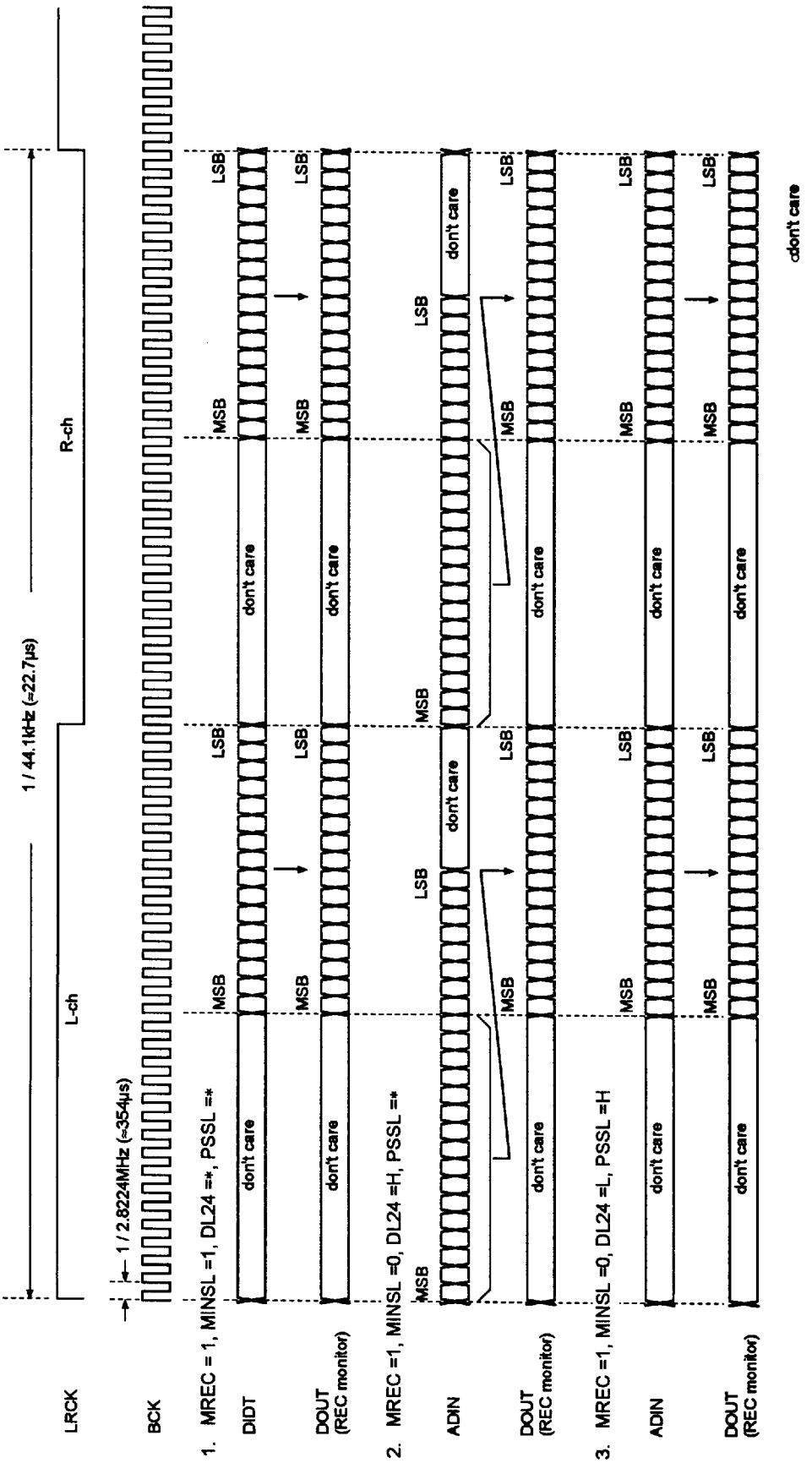
(2) Playback interface (Refer to the Audio Interface Timing Chart 2)

ATRAC-decoded playback data is output from the DOUT pin. The data occupies the last 16 bits of the 32-bit slot regardless of the setting of the INSL, DL24 and PSSL pins.

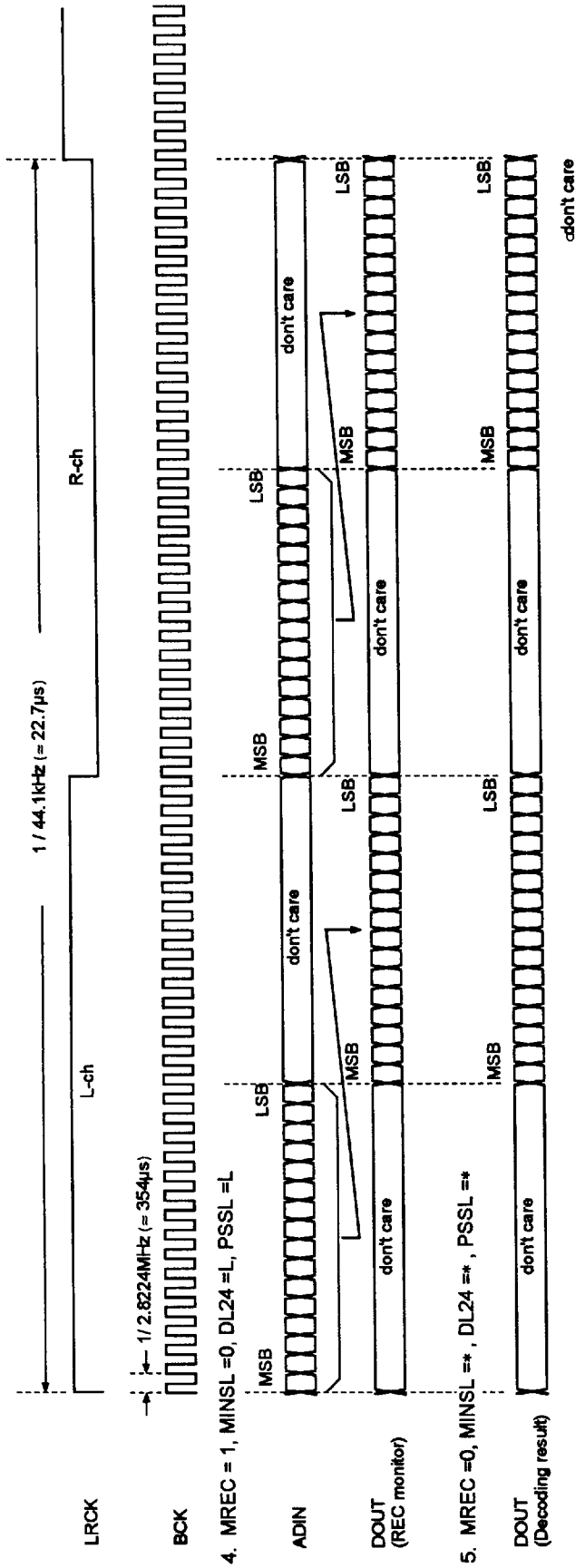
Playback mute can be applied to the DOUT output through the MUTE pin or the serial command CMUTE (D2). In addition, if playback attenuation is applied through the ATT pin or the serial command CATT (D5), the DOUT output is attenuated by –12dB.

When monaural playback is selected through the STRO pin or the serial command CSTRO (D4), the left-channel decoded value is output on the right channel as well.

Audio Interface Timing Chart 1

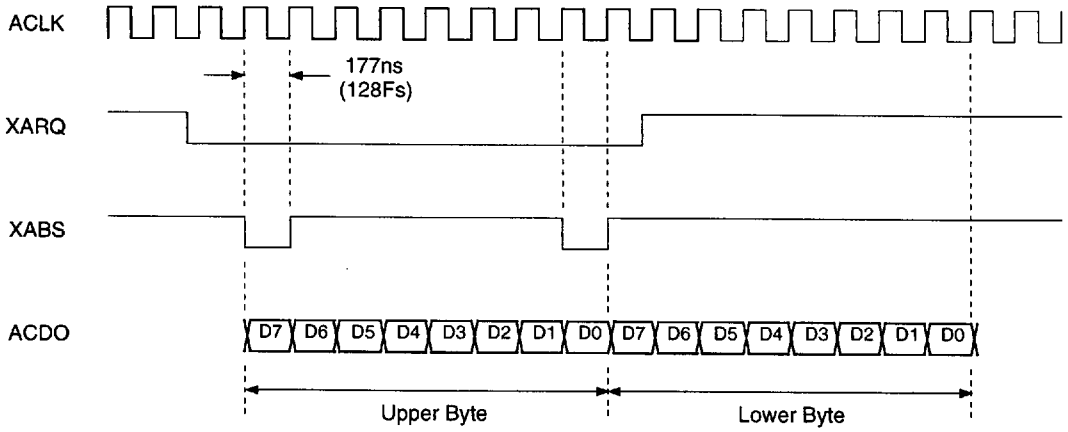


Audio Interface Timing Chart 2



3. Jump Guard Memory Controller Interface

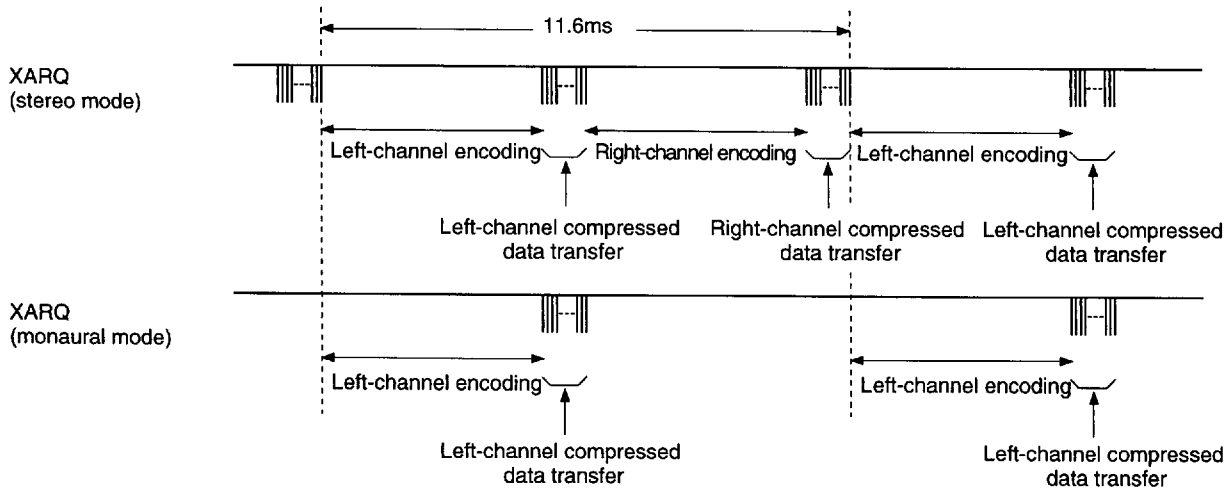
(1) Recording interface



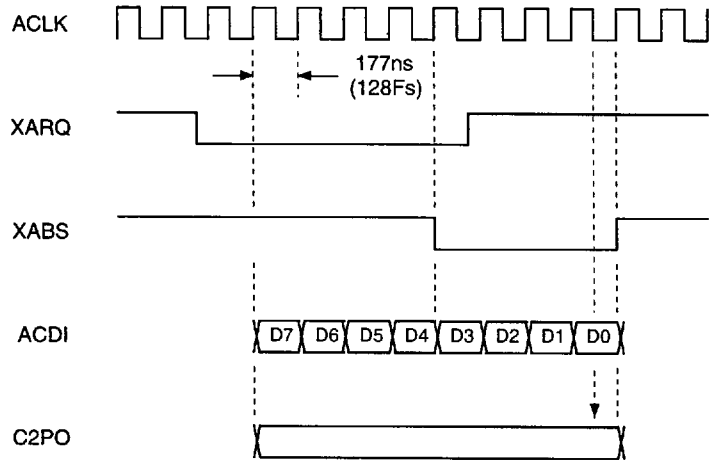
The above chart shows the transfer cycle for one word (two bytes) of compressed data. The transfer is performed for every one sound frame (212) bytes, and this cycle is executed 106 times.

When the CXD2531BR sets the transfer request XARQ Low, the CXD2526 outputs the synchronization pulse XABS for one ACLK cycle. The CXD2531BR synchronizes with the XABS pulse and outputs the upper byte of the compressed data from the ACDO pin. When the second XABS pulse is input, the lower byte is output and at the same time the transfer request XARQ is set High.

In stereo mode, audio data compression and compressed data transfer are both performed starting with the left channel; once the 212 bytes for the left channel have been transferred, the right-channel data is compressed and transferred. In monaural mode, only the left-channel data is compressed and transferred.



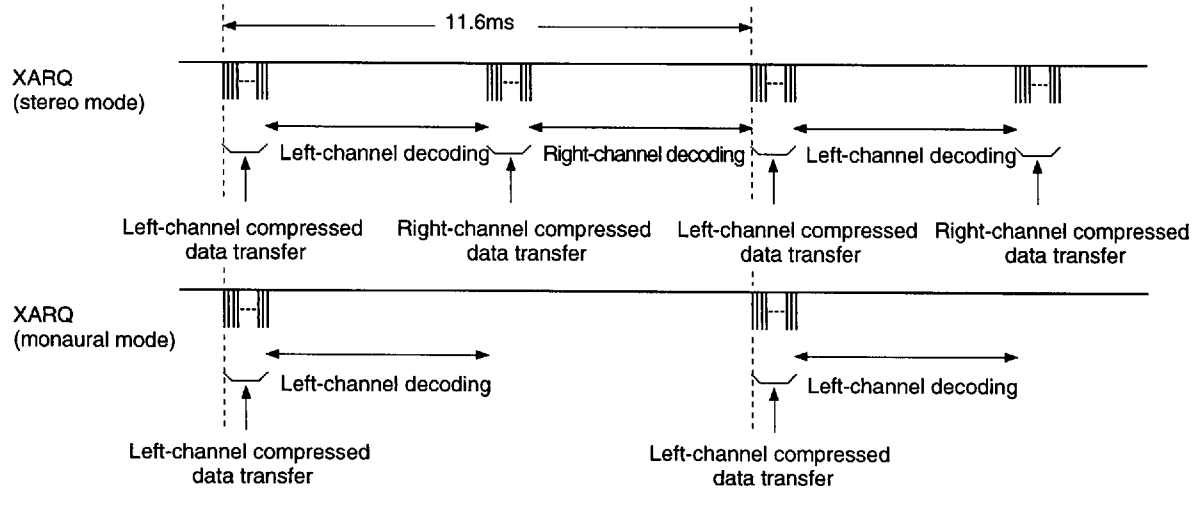
(2) Playback interface



The above chart shows the transfer cycle for one byte of compressed data. The transfer is performed for every one sound frame (212 bytes), and this cycle is executed 212 times.

When the CXD2531BR sets the transfer request XARQ Low, the CXD2526 outputs the compressed data and the synchronization pulse XABS by the byte. XABS is output for four ACLK cycles. In addition, the error status of the compressed data (High when an error occurs) is output by the byte and this is input to the C2PO pin of the CXD2531BR. When XABS goes from High to Low, the CXD2531BR returns the transfer request XARQ to High.

In stereo mode, the compressed data is transferred starting with the left channel; once the 212 bytes for the left channel have been transferred and decoded, the right-channel data is transferred. In monaural mode, only the left-channel data is transferred and decoded.

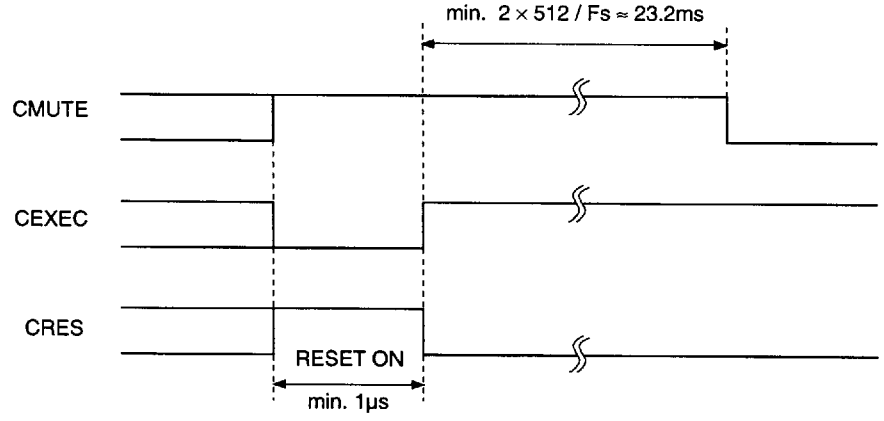


Control with the Microcontroller

The start/stop of the CXD2531BR operation should be executed as follows using the serial command.

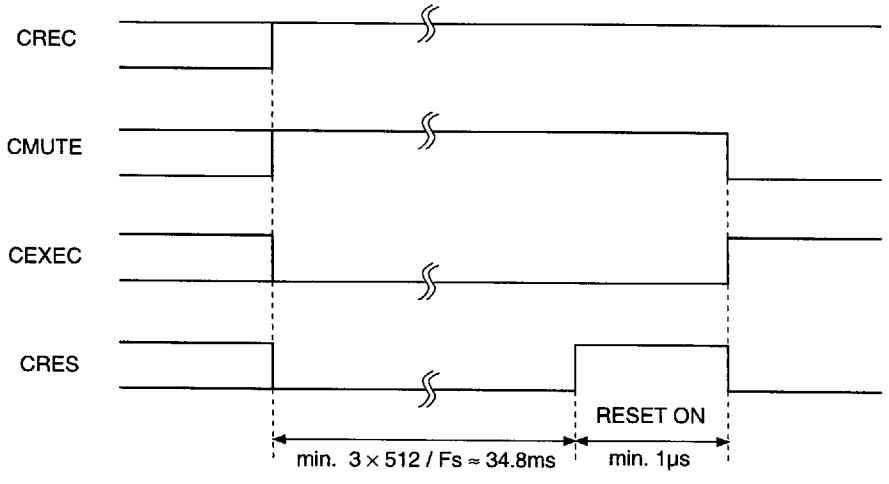
1. Playback start and pause release

(1) Set CMUTE=1, CEXEC=0, and CRES=1.
(2) Set CEXEC=1 and CRES=0 after 1µs or more. At this time, set CMUTE=1 to prevent the noise output from the DOUT pin.
(3) Set CEXEC=1, and then set CMUTE=0 after 2 × 512/Fs or more.



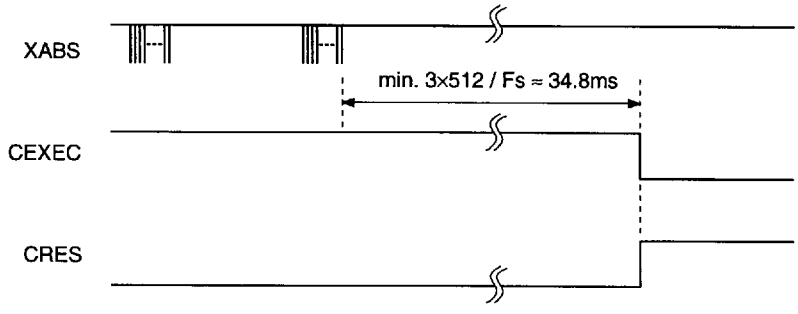
2. Recording start and recording pause release

(1) Set CMUTE=1, CEXEC=0, CRES=0, and CREC=1.
(2) Set CRES=1 after 3 × 512/Fs or more.
(3) Set CMUTE=0, CEXEC=1, and CRES=0 after 1µs or more.
(4) Do not record the first two sound groups of compressed data, which is output to the CXD2526, to the disc (not transfer them to the CXD2525), but record the data from the third sound group.



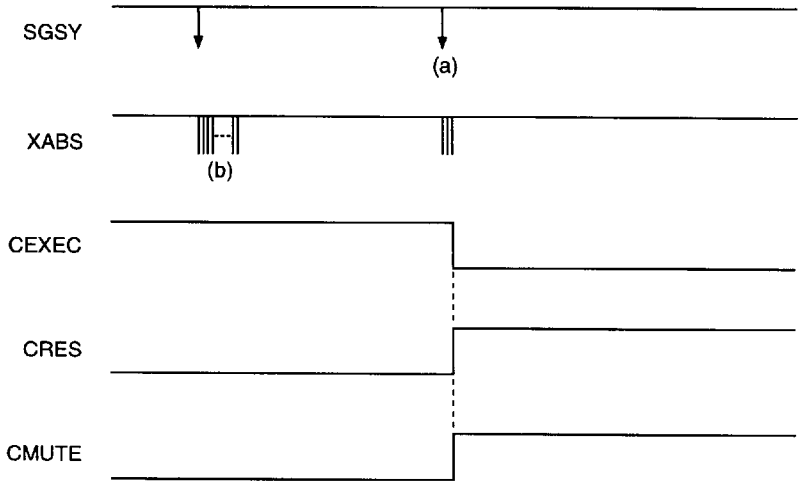
3. Playback stop and pause

(1) The data transfer from the CXD2526 is stopped. And, the CXD2531BR becomes muted when the data playback which was transferred from the CXD2526 is finished.
(2) Set CEXEC=0 and CRES=1 after 3 x 512/Fs or more since the last data is transferred.



4. Recording stop and recording pause

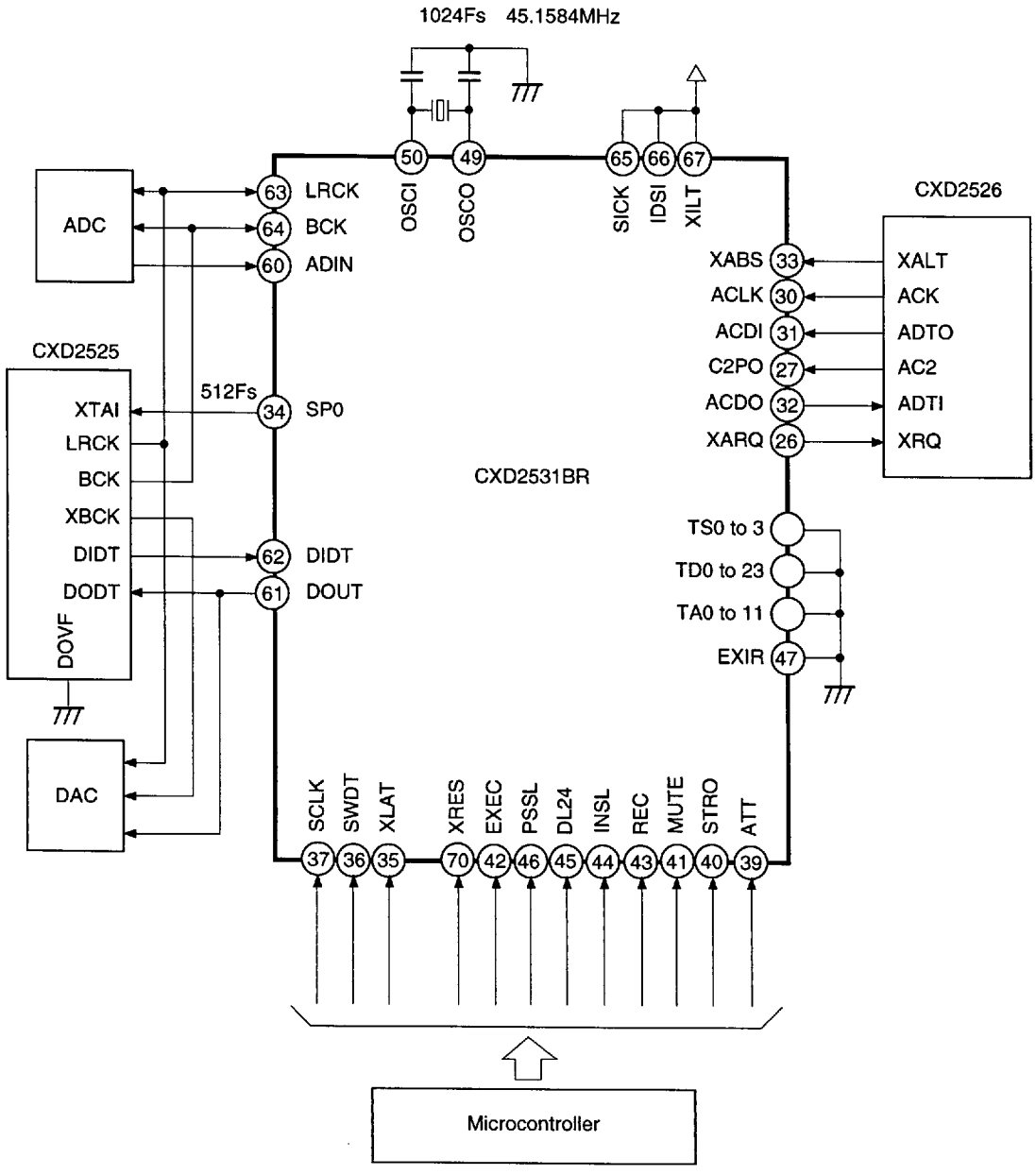
(1) Set CEXEC=0, CMUTE=1, and CRES=1 within 2 ms after the compressed data for one sound frame has been transferred from the CXD2531BR to the CXD2526.



5. Switching between STEREO and MONO

First, stop the recording/playback operation once and then set the mode (MSTRO) to resume the recording/playback operation.
The process for "Playback start and pause release" or "Recording start and recording pause release" described before should be performed to resume the recording/playback operation.

Application Circuit



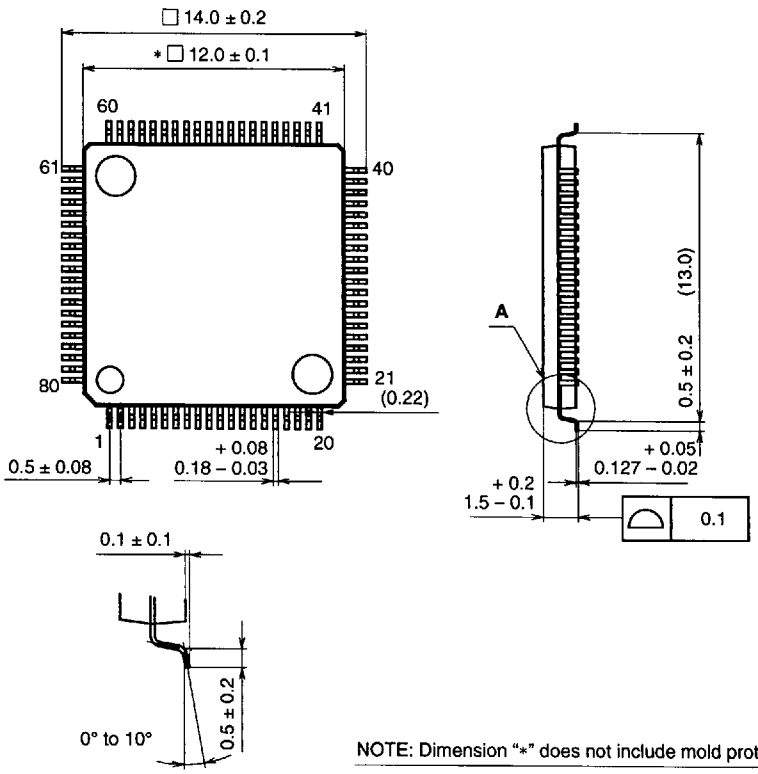
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Note on Power ON

- For using this IC, the voltage mentioned on the data sheet is supplied and each clock and data are input and the reset is released.
- Note that the clock or data is supplied during the power off because the IC may be damaged.
- Refer to "512Fs clock output and reset" on page 10 for the relationship of the SP0 pin and the reset.

Package Outline Unit: mm

80PIN LQFP (PLASTIC)



NOTE: Dimension "*" does not include mold protrusion.

DETAIL A

SONY CODE	LQFP-80P-L01
EIAJ CODE	*QFP080-P-1212-A
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY / PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.5g