HI2570, CXD2570

NOT RECOMMENDED FOR NEW DESIGNS

September 1997

1-Bit AD/DA Converter For Audio Application

Features

- **Two-Channel AD/DA Converters and Their Each Decimation and Oversampling Digital Filter in a Single Chip**
- **Simplified External Parts with a Built-In Analog Circuit Around AD Converter**
- **Distortion**
  - **ADC 0.015%**
  - **DAC . . . . . 0.009% (-3dB)**
- **S/N Ratio (Typical Values when F_S = 16kHz)**
  - **ADC 80dB**
  - **DAC 90dB**
- **Ripple in the Digital Filter Pass Band . . . . . ±0.05dB<**
- **Attenuation in the Digital Filter Rejection Band. . . 45dB>**

Applications

- **Telephones, TV Conference Systems, Language Laboratory Equipment, TV Game Equipment and Electronic Musical Instrument**

Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
HI2570JCQ	-20 to 55	48 Ld MPQF	Q48.12x12-S
CXD2570Q	-20 to 55	48 Ld MPQF	Q48.12x12-S

Description

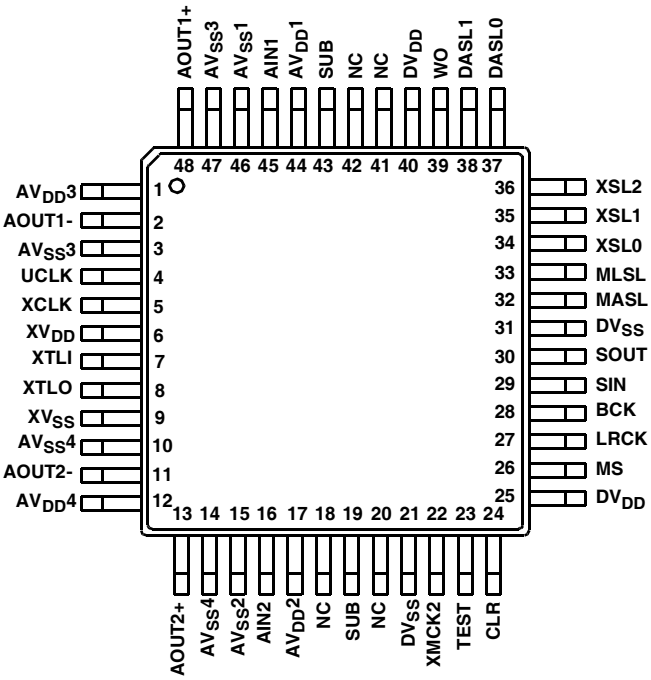
The HI2570, CXD2570 is a 1-bit stereo AD/DA converter which uses a 2nd-order $\Delta\Sigma$ system noise shaper. This LSI is especially suited for sampling frequency between 8kHz and 32kHz.

Function

- **Data Can Be Input/Output at Rate of 1xF_S with a Built-In Digital Filter**
- **Multi-Channel Systems can be Connected Using Several HI2570, CXD2570Qs**
- **The 32-Slot Serial Data Interface Enables Independent Selection of Data Frontward Truncation/Rearward Truncation and MSB First/LSB First**
- **512F_S/1024F_S (when F_S = 8 to 16kHz) or 256F_S/512F_S/768F_S/1024F_S (When F_S = 16 to 32kHz) Can be Used as the Master Clock**
- **The Sampling Frequency of Not Only 8kHz or 16kHz, but 32kHz or 44.1kHz Can Be Used for Audio Equipment**
- **Various Frequency Divided Clocks are Output for LSIs Connected**

Pinout

HI2570, CXD2570 (48 LEAD MQFP)
TOP VIEW



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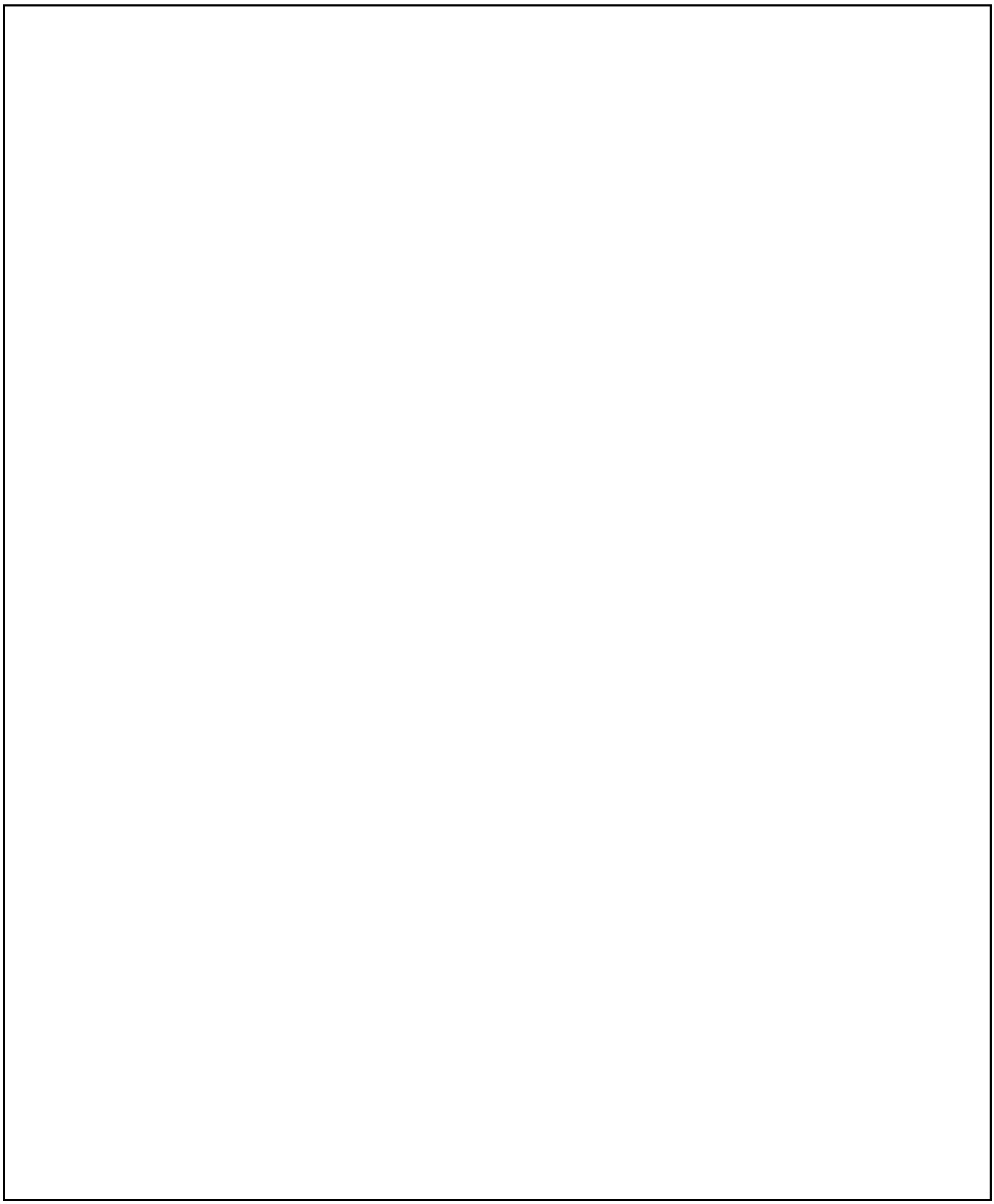


Pin Descriptions

PIN NO.	SYMBOL	I/O	DESCRIPTION
1	$AV_{DD}3$	—	Analog power supply for channel-1 DA converter
2	AOUT1 (-)	O	Analog reversed phase output of channel-1 DA converter
3	$AV_{SS}3$	—	Analog GND for channel-1 DA converter
4	UCLK	O	Outputs a 1/2 frequency divider of clock input from oscillation pin XTLI (Pin 7). User clock output for the externally connected ICs.
5	XCLK	O	256Fs/512Fs clock output. This provides the master clock for ICs operating in the slave mode when multiple CXD2570Qs are connected.
6	XV_{DD}	—	Digital power supply for the master clock
7	XTLI	I	Crystal oscillation circuit input. Connects the crystal oscillator selected by the crystal selector pins XSL0 to 2 (Pins 34, 35 and 36). To input an external master clock, this pin is used.
8	XTLO	O	Crystal oscillation circuit output. Connects the crystal oscillator selected by the crystal selector pins XSL0 to 2 (Pins 34, 35 and 36).
9	XV_{SS}	—	Digital GND for the master clock
10	$AV_{SS}4$	—	Analog GND for channel-2 DA converter
11	AOUT2 (-)	O	Analog reversed phase output of channel-2 DA converter
12	$AV_{DD}4$	—	Analog power supply for channel-2 DA converter
13	AOUT2 (+)	O	Analog forward phase output of channel-2 DA converter
14	$AV_{SS}4$	—	Analog GND for channel-2 DA converter
15	$AV_{SS}2$	—	Analog GND for channel-2 AD converter
16	AIN1	I	Analog input of channel-2 converter
17	$AV_{DD}2$	—	Analog power supply for channel-2 AD converter
18	NC	—	
19	SUB	—	Connected to the substrate in the IC (having the same potential as power supply). Connect this pin to GND via a capacitor on the external printed wiring board.
20	NC	—	
21	DV_{SS}	—	Digital GND
22	XMCK2	O	IC measurement. Normally, Low is output.
23	TEST	I	Test. Normally, fixed at Low. Equipped with a pull-down resistor.
24	CLR	I	System clear input. Normally, fixed at High; cleared at Low. Equipped with a pull-up resistor.
25	DV_{DD}	—	Digital power supply.
26	MS	I	Master/slave mode switching input. High = Master mode. Low = Slave mode. Equipped with a pull-up resistor.
27	LRCK	I/O	Sampling frequency clock pin of serial I/O. Outputs in master mode (when Pin 26 is High). Inputs in slave mode (when Pin 26 is Low). Transfers channel-1 data at High; transfers channel-2 data at Low.

Pin Descriptions (Continued)

PIN NO.	SYMBOL	I/O	DESCRIPTION
28	BCK	I/O	Serial bit transfer clock for serial input data SIN or serial output data SOUT (64FS). Outputs in master mode (when Pin 26 is High). Inputs in slave mode (when Pin 26 is Low). Retrieves serial input data at ↑; send serial output data at ↓.
29	SIN	I	Serial data input of 2-channel sampling. The data format is 2's complement, and consists of 32-bit slot.
30	SOUT	O	Serial data output of 2-channel per sampling. The data format is 2's complement, and consists of 32-bit slot.
31	DV_{SS}	—	Digital GND
32	MASL	I	Selects whether 16-bit serial data is applied in the first 16-bits or the last 16-bit of 32-bit slot in serial I/O. High = Frontward truncation; Low = Rearward truncation
33	MLSL	I	Selects whether 16-bit serial data is input/output at LSB first or MSB first in serial I/O. High = MSB first; Low = LSB first
34	XSL0	I	Crystal oscillator selection. Three bits, XSL0 to 2. Selects the clock frequency to be input from XTLI (Pin 7).
35	XSL1	I	Crystal oscillator selection. Three bits, XSL0 to 2. Selects the clock frequency to be input from XTLI (Pin 7).
36	XSL2	I	Crystal oscillator selection. Three bits, XSL0 to 2. Selects the clock frequency to be input from XTLI (Pin 7).
37	DASL0	I	IC measurement. Normally, fixed at High.
38	DASL1	I	IC measurement. Normally fixed at Low.
39	WO	I	Window masked when High; window open when Low (forced synchronization). Equipped with a pull-up resistor.
40	DV_{DD}	—	Digital power supply
41	NC	—	
42	NC	—	
43	SUB	—	Connected to the substrate in the IC (having the same potential as power supply). Connect this pin to GND via capacitor on the external printed wiring board.
44	$AV_{DD}1$	—	Analog power supply for channel-1 AD converter
45	AIN1	I	Analog input of channel-1 AD converter
46	$AV_{SS}1$	—	Analog GND for channel-1 AD converter
47	$AV_{SS}3$	—	Analog GND for channel-1 DA converter
48	AOUT1 (+)	O	Analog forward phase output of channel-1 DA converter

Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage (V_{DD}) . . . . . V_{SS}–0.5V to 7.0V
Input Voltage (V_1) . . . . . V_{SS} – 0.5V to V_{DD} + 0.5V
Output Voltage (V_0) . . . . . V_{SS} – 0.5V to V_{DD} + 0.5V
Operating Temperature (Topr) . . . . . -20°C to 75°C
Storage Temperature (Tstg . . . . . -55°C to 150°C

I/O Capacitance

	MIN	TYP	MAX
Input Pin (C_{IN})	—	—	9pF
Output Pin (C_{OUT})	—	—	11pF
Bidirectional Pin ($C_{I/O}$)	—	—	11 pF

Measurement conditions: $V_{DD} = V_1 = 0V$, f = 1MHz

Recommended Operating Conditions

	MIN	TYP	MAX
Supply Voltage (Note 1) (V_{DD})	4.5V	5.0V	5.5V
Ambient Temperature (T_A)	-20°C	—	+75°C
Sampling Frequency (Note 2) (F_S)	7kHz	—	33kHz

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. The analog power supplies for AD converters (Pins 17 and 44) must be turned on simultaneously with or before other poser supplies. turning on these power supplies after any other power supply may cause the device to fall into latch-up condition. this precaution, however, does not apply when turning off the power supplies.
2. Although the device can operate with F_S frequencies such as F_S = 44.1kHz or 48kHz, its analog characteristics deteriorate to extent. When used at only these F_S frequencies, the CXD255Q is recommended that is pin-compatible with the CXD2570Q.

Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	PART NUMBER OR GRADE MIN	TYP	MAX	UNITS	APPLICABLE PINS
DC Characteristics	$AV_{DD}1 = AV_{DD}2 = AV_{DD}3 = AV_{DD}4 = XV_{DD} = DV_{DD} = 5.0V \pm 10\%$, $AV_{SS}1 = AV_{SS}2 = AV_{SS}3 = AV_{SS}4 = XV_{SS} = DV_{SS} = 0V$, T_A = -20°C to 75°C						
Input Voltage	V_{IHC}		$0.7V_{DD}$	—	—	V	*1
	V_{ILC}		Ò	Ò	$0.3V_{DD}$		
	V_{IN}	Analog Input	V_{SS}	—	V_{DD}	V	*2
Output Voltage	V_{OH1}	I_{OH} = -2mA	V_{DD} -0.5	—	V_{DD}	V	*3
	V_{OL1}	I_{OL} = 4mA	0	—	0.4		
	V_{OH2}	I_{OH} = -4mA	V_{DD} -0.5	—	V_{DD}	V	*4
	V_{OL2}	I_{OL} = 4mA	0	—	0.4		
	V_{OH3}	I_{OH} = -12mA	$V_{DD}/2$	—	V_{DD}	V	*5
	V_{OL3}	I_{OL} = 16mA	0	—	$V_{DD}/2$		
	V_{OH4}	I_{OH} = -2mA	V_{DD} -0.8	—	V_{DD}	V	*6
	V_{OL4}	I_{OL} = 4mA	0	—	0.4		
Input Leak Current 1	I_{LI1}		-10	—	10	µA	*7
Input Leak Current 2	I_{LI2}		-40	—	40	µA	*8
Input Leak Current 3	I_{LI3}		-20	-50	-12-	µA	*9
Input Leak Current 4	I_{LI4}		20	50	120	µA	*10
Output Leak Current	I_{LZ}		-40	—	40	µA	*11
Feedback Resistance	R_{FB}	$V_{IN} = V_{SS}$ or V_{DD}	250K	1M	‘2.5M	Ω	*12
Supply Current	I_{DD}	(Note 3)	—	43	60	mA	
AC Characteristics	$AV_{DD}1 = AV_{DD}2 = AV_{DD}3 = AV_{DD}4 = XV_{DD} = DV_{DD} = 5.0V \pm 10\%$, $AV_{SS}1 = AV_{SS}2 = AV_{SS}3 = AV_{SS}4 = XV_{SS} = DV_{SS} = 0V$, T_A = -20°C to 75°C						
SIN Setup Time	tsus		10	—	—	ns	
SIN Hold Time	ths		15	—	—	ns	
LRCK Setup Time	tsul	Slave mode	10	—	—	ns	
LRCK Hold Time	thl	Slave mode	15	—	—	ns	
LRCK Delay Time	tdl	Master mode CL = 130pF	-40	—	30	ns	

Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	PART NUMBER OR GRADE			UNITS	APPLICABLE PINS
			MIN	TYP	MAX		
SOUT Delay Time	tds	CL = 60pF	9	—	65	ns	
SOUT Data Recovery Time	tzd		7	—	42	ns	
SOUT Data Erase Time	tdz		6	—	40	ns	
XTLI Pulse Width for Low Period	twl	FS = 16kHz, 256Fs (XSL0 = XSL1 = XSL2 = Low	40	—	200	ns	

NOTES:

3. This includes current consumption at load resistance (RL = 3.9Ω). Fs = 16kHz
   *1 All input pins except AIN1 and AIN2, and when bidirectional pins (BCK and LRCK) are input mode.
   *2 AIN1, AIN2
   *3 XCLK, XMCK2, SOUT
   *4 AOUT1 (+), AOUT1 (-), AOUT2 (+), AOUT2 (-), UCLK
   *5 XTLO
   *6 When bidirectional pins (BCK and LRCK) are output mode
   *7 All input pins except AIN1 and AIN2
   *8 When directional pins (BCK and LRCK) are input mode
   *9 MS, WO, CLR
   *10 TEST
   *11 SOUT, AOUT1 (+), AOUT1 (-), AOUT2 (+), AOUT2 (-), UCLK
   *12 Resistance between XTLO and XTLI

Analog Characteristics

$AV_{DD}1 = AV_{DD}2 = AV_{DD}3 = AV_{DD}4 = XV_{DD} = DV_{DD} = 5.0V \pm 10\%$, $AV_{SS}1 = AV_{SS}2 = AV_{SS}3 = AV_{SS}4 = XV_{SS} = DV_{SS} = 0V$, $T_A = 25^oC$

ITEM	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ADC + DAC Connection Overall Characteristics. Measured under the following conditions unless otherwise specified. Input waveform = 1kHz sine wave, 1.4Vrms (= 0dB), R_{IN} = 16kΩ XTAI = 16.384MHz (= 1024Fs, Fs = 16kHz) CLR = MS = WO = open (= 5V) SOUT and SIN directly coupled.					
S/N Ratio	8kHz LPF	74	80	—	dB
THD + N	8kHz LPF	—	0.015	0.03	%
Dynamic Range	1kHz, -60dB 8kHz LPF	74	80	—	dB
Channel Separation	1kHz, 0dB	—	97	—	dB
Gain Difference Between Channels		—	0.1	—	dB
Gain	RL = 3.9kW	-3	0	+3	dB
Input Level	R_{IN} = 0Ω	—	0.1	—	Vrms
	R_{IN} = 16Ω	—	1.4	—	Vrms
DC Offset (ADC Output)		—	030F	—	Hex
ADC Input Impedance		—	1.2		kΩ
DAC characteristics in a single unit. Measured under the following conditions unless otherwise specified. Input data = 1kHz sine wave, full scale (= 0dB) XTAI = 16.384MHz (= 1024Fs, Fs = 16kHz CLR = WO = open (= 5V), MS = GND					
S/N Ratio	8kHz LPF	84	90	—	dB
THD + N	8kHz LPF, -3dB	—	0.009	0.03	%
Dynamic Range	1kHz, -60dB 8kHz LPF	82	88	—	dB

Analog Characteristics $AV_{DD}1 = AV_{DD}2 = AV_{DD}3 = AV_{DD}4 = XV_{DD} = DV_{DD} = 5.0V \pm 10\%$, $AV_{SS}1 = AV_{SS}2 = AV_{SS}3 = AV_{SS}4 = XV_{SS} = DV_{SS} = 0V$, $T_A = 25^oC$ **(Continued)**

ITEM	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Channel Separation	1kHz, 0dB	—	100	—	dB
Gain Difference Between Channels		—	0.05	—	dB
Output Level	R_L = 3.9kW	1.80	1.93	2.10	Vrms

Description of Functions

1. Serial data interface

[Related pins] LRCK, BCK, SOUT, SIN, MASL, MLSL

The serial data format is common for both SIN (DA converter input) and SOUT (AD converter output), consisting of two channels per sampling serial data represented by 2's complement. Each channel is divided into 32-bit slots, of which 16 bits are handled as data.

MASL is used to select whether the 16 bits of valid data is placed in the first or the last half of the 32-bit slots.

Similarly, MLSL is used to select whether the serial data is arranged at MSB first of LSB first.

MASL	
High	Frontward truncation
Low	Rearward truncation

MLSL	
High	MSB first
Low	LSB first

2. Master mode/slave mode

[Related pins] MS, LRCK, BCK

When using the CXD2570Q in multiple units or in a pair with DA converter such as the CXD2558M, one of these CXD2570Qs should be in the master mode to serve as the source of clocks LRCK and BCK.

The other ICs including CXD2570Qs are used in the slave mode, with their clocks LRCK and BCK supplied by the master CXD2570Q.

MS	MODE	LRCK AND BCK I/O
High	Master mode	Output
Low	Slave mode	Input

3. Crystal oscillator frequency selection (FS = 16kHz to 48kHz)

[Related pins] XTLI, XTLO, XSL0, XSL1, XSL2, UCLK, XCLK

By setting a combination of XSL0 and XSL1, with XSL2 fixed low, the frequency of the external crystal oscillator connected to XTLI and XTLO can be selected. In this case, XCLK outputs a clock whose frequency is always 256 times Fs, and UCLK outputs a clock that is half the crystal oscillator frequency.

When supplying the master clock from some other external source, not a crystal oscillator, use XTLI for this clock input and leave XTLO open.

XSL2	XSL1	XSL0	CRYSTAL OSCILLATOR FREQUENCY	XCLK	UCLK
L	L	L	256Fs	256Fs	128Fs
L	L	H	512Fs	256Fs	256Fs
L	H	L	768Fs	256Fs	384Fs
L	H	H	1024Fs	256Fs	512Fs

*The CXD2555Q, which has the same pin configuration with this IC is recommended when using only Fs = 32kHz to 48kHz.

4. Crystal oscillator frequency selection (FS = 8kHz to 16kHz)

[Related pins] XTLI, XTLO, XSL0, XSL1, XSL2, UCLK, XCLK

With XSL2 fixed High, the device can be operated with low-Fs frequencies. In this case, the frequency of the crystal oscillator can be selected by setting a combination of XSL0 and XSL1 accordingly.

XSL2	XSL1	XSL0	CRYSTAL OSCILLATOR FREQUENCY*	XCLK	UCLK
H	L	L	512Fs	512Fs	256Fs
H	L	H	—	—	—
H	H	L	1024Fs	512Fs	512Fs
H	H	H	—	—	—

5. A/D converter input level

Any desired input level V_{IN} (m . 0.1Vrms) can be selected by adjusting R_{IN} to generate the full-scale output of the AD converter.

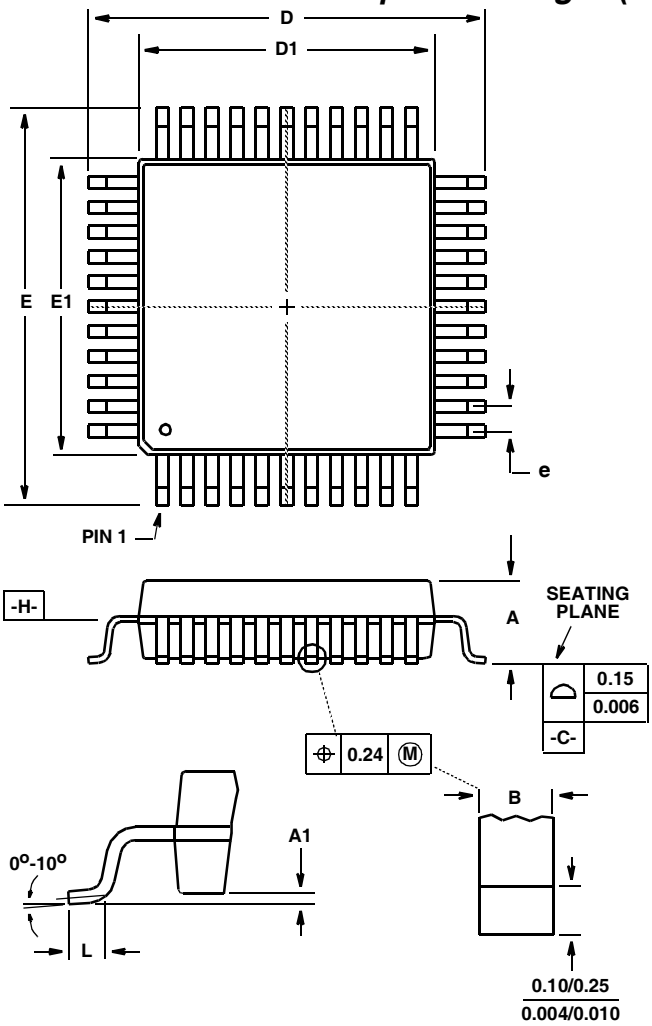
V_{IN} generation of full-scale output varies with the products, and calculate the V_{IN} maximum level (approximately -3dB below the full-scale) using the following equation to input the signal.

(1) Fs = 16kHz to 48kHz (XSL2 = Low)
$R_{IN} = 1230 \cdot V_{IN}$ [Vrms] -1200 (Ω)
(2) Fs = 8 to 16kHz (XSL2 = High)
$R_{IN} = 26600 \cdot V_{IN}$ [Vrms] -1200 (Ω)

6. D/A converter output level

To change the D/A converter output level, adjust R15, R17, R30 and R32 in Application Circuit on page.

Metric Plastic Quad Flatpack Packages (MQFP)



Q48.12x12-S

48 LEAD METRIC PLASTIC QUAD FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.081	0.100	2.05	2.55	-
A1	0.000	0.011	0.00	0.30	-
B	0.008	0.017	0.20	0.45	5
D	0.587	0.618	14.90	15.70	2
D1	0.469	0.488	11.90	12.40	3, 4
E	0.587	0.618	14.90	15.70	2
E1	0.469	0.488	11.90	12.40	3, 4
L	0.028	0.043	0.70	1.10	-
N	48		48		6
e	0.032 BSC		0.80 BSC		-

Rev. 0 2/96

NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. Dimensions D and E to be determined at seating plane -C-.
3. Dimensions D1 and E1 to be determined at datum plane -H-.
4. Dimensions D1 and E1 do not include mold protrusion.
5. Dimension B does not include dambar protrusion.
6. “N” is the number of terminal positions.