

# DSP56858

## Preliminary Technical Data

### DSP56858 16-bit Digital Signal Processor

- 120 MIPS at 120MHz
- 40K x 16-bit Program SRAM
- 24K x 16-bit Data SRAM
- 1K x 16-bit Boot ROM
- Access up to 2M words of program memory or 8M data memory
- Chip Select Logic for glue-less interface to ROM and SRAM
- Six (6) independent channels of DMA
- Two (2) Enhanced Synchronous Serial Interfaces (ESSI)
- Two (2) Serial Communication Interfaces (SCI)
- Serial Port Interface (SPI)
- 8-bit Parallel Host Interface
- General Purpose 16-bit Quad Timer
- JTAG/Enhanced On-Chip Emulation (OnCE™) for unobtrusive, real-time debugging
- Computer Operating Properly (COP)/Watchdog Timer
- Time-of -Day (TOD)
- 144 LQFP and 144 MAPBGA packages
- Up to 47 GPIO

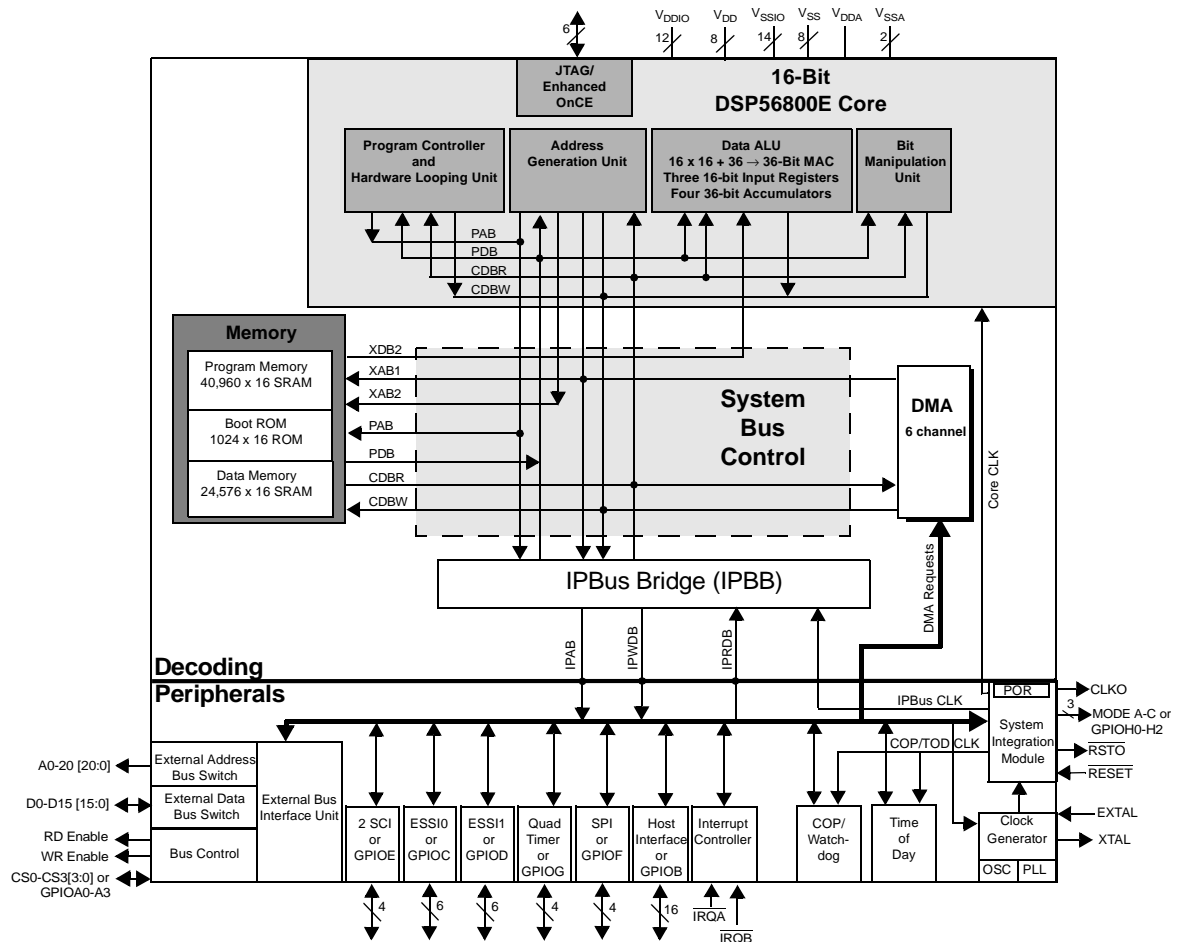


Figure 1. DSP56858 Block Diagram

# Part 1 Overview

## 1.1 DSP56858 Features

### 1.1.1 Digital Signal Processing Core

- Efficient 16-bit DSP engine with dual Harvard architecture
- 120 Million Instructions Per Second (MIPS) at 120MHz core frequency
- Single-cycle  $16 \times 16$ -bit parallel Multiplier-Accumulator (MAC)
- Four (4) 36-bit accumulators including extension bits
- 16-bit bidirectional shifter
- Parallel instruction set with unique DSP addressing modes
- Hardware DO and REP loops
- Three (3) internal address buses and one (1) external address bus
- Four (4) internal data buses and one (1) external data bus
- Instruction set supports both DSP and controller functions
- Four (4) hardware interrupt levels
- Five (5) software interrupt levels
- Controller-style addressing modes and instructions for compact code
- Efficient C-Compiler and local variable support
- Software subroutine and interrupt stack with depth limited only by memory
- JTAG/Enhanced OnCE debug programming interface

### 1.1.2 Memory

- Harvard architecture permits up to three (3) simultaneous accesses to program and data memory
- On-Chip Memory
  - $40K \times 16$ -bit Program RAM
  - $24K \times 16$ -bit Data RAM
  - $1K \times 16$ -bit Boot ROM
- Off-Chip Memory Expansion (EMI)
  - Access up to 2M words of program or 8M data memory (using chip selects)
  - Chip Select Logic for glue-less interface to ROM and SRAM

### 1.1.3 DSP56858 Peripheral Circuit Features

- General Purpose 16-bit Quad Timer\*
- Two Serial Communication Interfaces (SCI)\*
- Serial Peripheral Interface (SPI) Port\*
- Two (2) Enhanced Synchronous Serial Interface (ESSI) modules\*
- Computer Operating Properly (COP)/Watchdog Timer

- JTAG/Enhanced On-Chip Emulation (EOnCE) for unobtrusive, real-time debugging
- Six (6) independent channels of DMA
- 8-bit Parallel Host Interface\*
- Time-of-Day (TOD)
- Up to 47 GPIO

\* Each peripheral I/O can be used alternately as a GPIO if not needed

### 1.1.4 Energy Information

- Fabricated in high-density CMOS with 3.3V, TTL-compatible digital inputs
- Wait and Stop modes available

## 1.2 DSP56858 Description

The DSP56858 is a member of the DSP56800E core-based family of Digital Signal Processors (DSPs). This device combines the processing power of a DSP and the functionality of a microcontroller with a flexible set of peripherals on a single chip to create an extremely cost-effective solution. The low cost, flexibility, and compact program code make this device well-suited for many applications. The DSP56858 includes peripherals that are especially useful for teledatacom devices; Internet appliances; portable devices; TAD; voice recognition; hands-free devices; and general purpose applications.

The DSP56800E core is based on a Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The microprocessor-style programming model and optimized instruction set allow straightforward generation of efficient, compact code for both DSP and MCU applications. The instruction set is also highly efficient for C Compilers, enabling rapid development of optimized control applications.

The DSP56858 supports program execution from either internal or external memories. Two data operands can be accessed from the on-chip Data RAM per instruction cycle. The DSP56858 also provides two external dedicated interrupt lines, and up to 47 General Purpose Input/Output (GPIO) lines, depending on peripheral configuration.

The DSP56858 DSP controller includes 40K words of Program RAM, 24K words of Data RAM and 1K of Boot RAM. It also supports program execution from external memory.

This DSP controller also provides a full set of standard programmable peripherals that include an 8-bit Parallel Host Interface, two Enhanced Synchronous Serial Interfaces (ESSI), one Serial Peripheral Interface (SPI), two Serial Communications Interfaces (SCI), and one Quad Timer. The Host Interface, Quad Timer, SSI, SPI, SCI I/O and four chip selects can be used as General Purpose Input/Outputs when its primary function is not required.

## 1.3 “Best in Class” Development Environment

The SDK (Software Development Kit) provides fully debugged peripheral drivers, libraries and interfaces that allow a programmer to create his own unique C application code independent of component architecture. The CodeWarrior Integrated Development Environment is a sophisticated tool for code navigation, compiling, and debugging. A complete set of evaluation modules (EVMs) and development system cards will support concurrent engineering. Together, the SDK, CodeWarrior, and EVMs create a complete, scalable tools solution for easy, fast and efficient development.

## 1.4 Product Documentation

The four documents listed in [Table 1](#) are required for a complete description of and proper design with the DSP56858. Documentation is available from local Motorola distributors, Motorola semiconductor sales offices, Motorola Literature Distribution Centers, or online at [www.motorola.com/semiconductors/](http://www.motorola.com/semiconductors/).

**Table 1. DSP56858 Chip Documentation**

Topic	Description	Order Number
DSP56800E Reference Manual	Detailed description of the DSP56800E architecture, 16-bit DSP core processor and the instruction set	DSP56800ERM/D
DSP56858 User's Manual	Detailed description of memory, peripherals, and interfaces of the DSP56858	DSP5685xUM/D
DSP56858 Technical Data Sheet	Electrical and timing specifications, pin descriptions, and package descriptions (this document)	DSP56858/D
DSP56858 Product Brief	Summary description and block diagram of the DSP56858 core, memory, peripherals and interfaces.	DSP56858PB/D

## 1.5 Data Sheet Conventions

This data sheet uses the following conventions:

$\overline{\text{OVERBAR}}$  This is used to indicate a signal that is active when pulled low. For example, the  $\overline{\text{RESET}}$  pin is active when low.

“asserted” A high true (active high) signal is high or a low true (active low) signal is low.

“deasserted” A high true (active high) signal is low or a low true (active low) signal is high.

Examples:	Signal/Symbol	Logic State	Signal State	Voltage <sup>1</sup>
	$\overline{\text{PIN}}$	True	Asserted	$V_{IL}/V_{OL}$
	$\overline{\text{PIN}}$	False	Deasserted	$V_{IH}/V_{OH}$
	PIN	True	Asserted	$V_{IH}/V_{OH}$
	PIN	False	Deasserted	$V_{IL}/V_{OL}$

1. Values for  $V_{IL}$ ,  $V_{OL}$ ,  $V_{IH}$ , and  $V_{OH}$  are defined by individual product specifications.

## Part 2 Signal/Connection Descriptions

### 2.1 Introduction

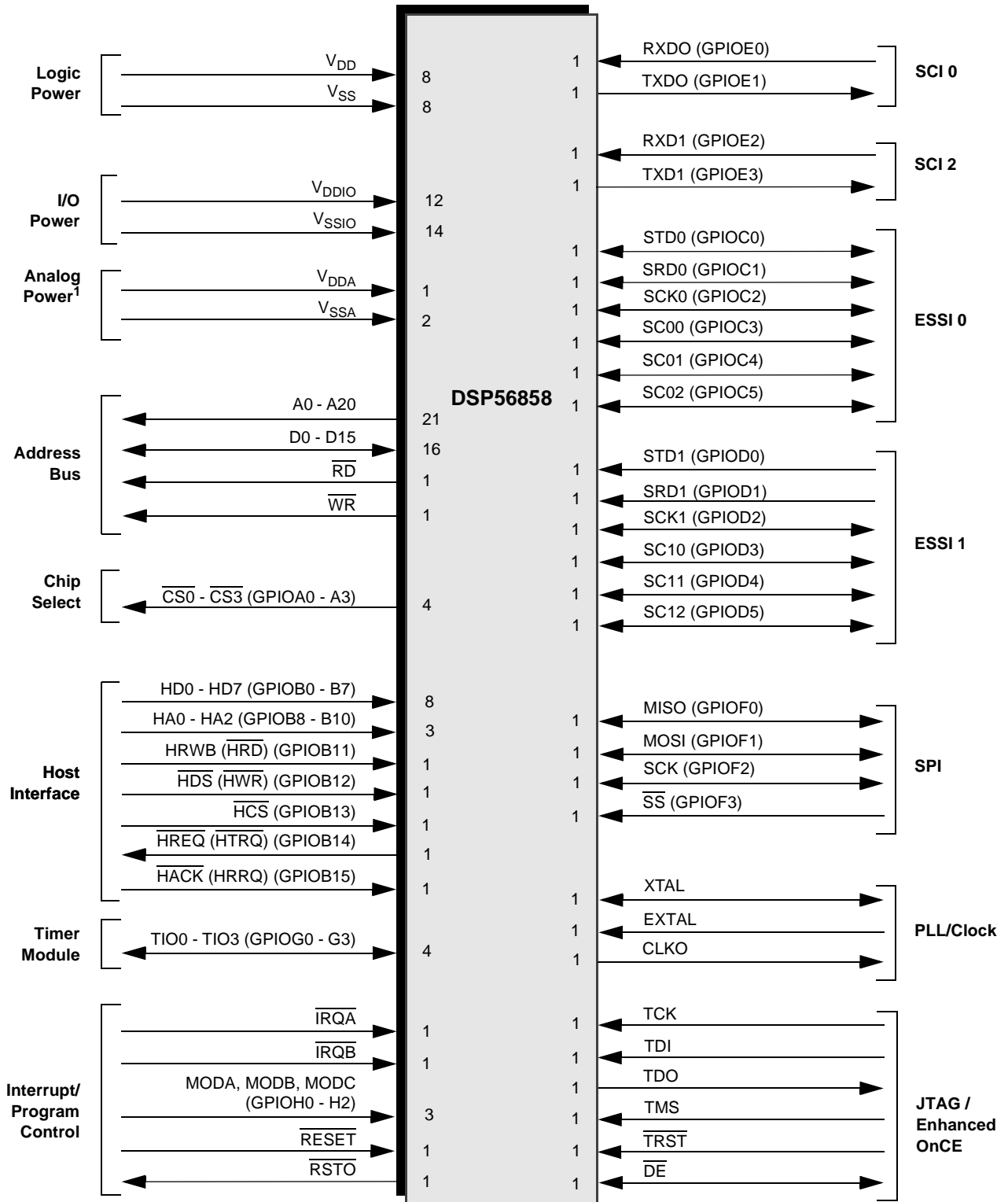
The input and output signals of the DSP56858 are organized into functional groups, as shown in **Table 2** and as illustrated in **Figure 2**. In **Table 3** each table row describes the package pin and the signal or signals present.

**Table 2. DSP56858 Functional Group Pin Allocations**

Functional Group	Number of Pins
Power ( $V_{DD}$ , $V_{DDIO}$ , or $V_{DDA}$ )	(8, 12, 1) <sup>1</sup>
Ground ( $V_{SS}$ , $V_{SSIO}$ , or $V_{SSA}$ )	(8, 14, 2) <sup>1</sup>
PLL and Clock	3
External Bus Signals	39
External Chip Select*	4
Interrupt and Program Control	7 <sup>2</sup>
Host Interface (HI)*	16 <sup>3</sup>
Enhanced Synchronous Serial Interface (ESSI0) Port*	6
Enhanced Synchronous Serial Interface (ESSI1) Port*	6
Serial Communications Interface (SCI0) Ports*	2
Serial Communications Interface (SCI1) Ports*	2
Serial Peripheral Interface (SPI) Port*	4
Quad Timer Module Port*	4
JTAG/On-Chip Emulation (OnCE)	6

\*Alternately, GPIO pins

1.  $V_{DD} = V_{DD\ CORE}$ ,  $V_{SS} = V_{SS\ CORE}$ ,  $V_{DDIO} = V_{DD\ IO}$ ,  $V_{SSIO} = V_{SS\ IO}$ ,  $V_{DDA} = V_{DD\ ANA}$ ,  $V_{SSA} = V_{SS\ ANA}$
2. MODA, MODB and MODC can be used as GPIO after the bootstrap process has completed.
3. The following Host Interface signals are multiplexed: HRWB to  $\overline{HRD}$ , HDS to  $\overline{HWR}$ , HREQ to  $\overline{HTRQ}$  and HACK to HRRQ.



**Figure 2. DSP56858 Signals Identified by Functional Group<sup>2</sup>**

1. Specifically for PLL, OSC, and POR.

2. Alternate pin functions are shown in parentheses. Pin direction/type is represented as the preferred functionality. GPIO may provide bidirectional use of any pin.

## Part 3 Signals and Package Information

All digital inputs have a weak internal pull-up circuit associated with them. These pull-up circuits are enabled by default. Exceptions:

1. When a pin has GPIO functionality, the pull-up may be disabled under software control.
2. MODE A, MODE B and MODE C pins have no pull-up.
3. TCK has a weak pull-down circuit always active.
4. Bidirectional I/O pullups automatically disable when the output is enabled.

This table is presented consistently with the *Signals Identified by Functional Group* figure.

1. **BOLD** entries in the *Type* column represents the state of the pin just out of reset.
2. Ouput(Z) means an output in a High-Z condition.

**Table 3. DSP56858 Signal and Package Information for the 144-pin LQFP and MAPBGA**

Signal Name	BGA Pin No.	LQFP Pin No.	Type	Description
V <sub>DD</sub>	E1	14	V <sub>DD</sub>	<b>Logic Power (V<sub>DD</sub>)</b> —These pins provide power to the internal structures of the chip, and should all be attached to V <sub>DD</sub> .
V <sub>DD</sub>	M6	36		
V <sub>DD</sub>	F12	52		
V <sub>DD</sub>	A9	72		
V <sub>DD</sub>	M2	87		
V <sub>DD</sub>	J12	88		
V <sub>DD</sub>	E12	109		
V <sub>DD</sub>	A12	125		
V <sub>SS</sub>	G1	15	V <sub>SS</sub>	<b>Logic Power–Ground (V<sub>SS</sub>)</b> —These pins provide grounding for the internal structures of the chip and should all be attached to V <sub>SS</sub> .
V <sub>SS</sub>	L6	16		
V <sub>SS</sub>	D12	53		
V <sub>SS</sub>	A7	54		
V <sub>SS</sub>	F1	71		
V <sub>SS</sub>	M7	89		
V <sub>SS</sub>	K12	126		
V <sub>SS</sub>	A8	127		

**Table 3. DSP56858 Signal and Package Information for the 144-pin LQFP and MAPBGA**

Signal Name	BGA Pin No.	LQFP Pin No.	Type	Description
V <sub>DDIO</sub>	B1	5	V <sub>DDIO</sub>	<b>I/O Power (V<sub>DDIO</sub>)</b> —These pins provide power for all I/O and ESD structures of the chip and should all be attached to V <sub>DDIO</sub> (3.3V).
V <sub>DDIO</sub>	H1	6		
V <sub>DDIO</sub>	M3	20		
V <sub>DDIO</sub>	M8	45		
V <sub>DDIO</sub>	M11	61		
V <sub>DDIO</sub>	H12	67		
V <sub>DDIO</sub>	C12	68		
V <sub>DDIO</sub>	A11	80		
V <sub>DDIO</sub>	A5	105		
V <sub>DDIO</sub>	A3	113		
V <sub>DDIO</sub>	C1	129		
V <sub>DDIO</sub>	M10	139		
V <sub>SSIO</sub>	D1	7	V <sub>SSIO</sub>	<b>I/O Power–Ground (V<sub>SSIO</sub>)</b> —These pins provide grounding for all I/O and ESD structures of the chip and should all be attached to V <sub>SS</sub> .
V <sub>SSIO</sub>	J1	21		
V <sub>SSIO</sub>	M5	46		
V <sub>SSIO</sub>	M9	47		
V <sub>SSIO</sub>	L12	62		
V <sub>SSIO</sub>	G12	69		
V <sub>SSIO</sub>	B12	70		
V <sub>SSIO</sub>	A10	82		
V <sub>SSIO</sub>	A4	106		
V <sub>SSIO</sub>	A1	115		
V <sub>SSIO</sub>	A2	128		
V <sub>SSIO</sub>	M4	130		
V <sub>SSIO</sub>	M12	140		
V <sub>SSIO</sub>	A6	141		
V <sub>DDA</sub>	K1	24	V <sub>DDA</sub>	<b>Analog Power (V<sub>DDA</sub>)</b> —These pins supply an analog power source.
V <sub>SSA</sub>	M1	25	V <sub>SSA</sub>	<b>Analog Ground (V<sub>SSA</sub>)</b> —This pin supplies an analog ground.
V <sub>SSA</sub>	L1	26		



**Table 3. DSP56858 Signal and Package Information for the 144-pin LQFP and MAPBGA**

Signal Name	BGA Pin No.	LQFP Pin No.	Type	Description
A0	E5	10	Output(Z)	<b>Address Bus (A0-A20)</b> —These signals specify a word address for external program or data memory access.
A1	E4	11		
A2	E3	12		
A3	E2	13		
A4	J2	29		
A5	H3	30		
A6	G4	31		
A7	H4	32		
A8	G5	48		
A9	L5	49		
A10	J6	50		
A11	K6	51		
A12	J8	63		
A13	K8	64		
A14	L9	65		
A15	K9	66		
A16	K10	75		
A17	K11	76		
A18	J9	77		
A19	J10	78		
A20	J11	79		

**Table 3. DSP56858 Signal and Package Information for the 144-pin LQFP and MAPBGA**

Signal Name	BGA Pin No.	LQFP Pin No.	Type	Description
D0	H7	81	<b>Input/Output(Z)</b>	<b>Data Bus (D0-D15)</b> —These pins provide the bidirectional data for external program or data memory accesses.
D1	G7	94		
D2	F9	95		
D3	F10	96		
D4	F11	97		
D5	E10	98		
D6	D7	120		
D7	B7	121		
D8	E7	122		
D9	F8	123		
D10	F7	124		
D11	D5	137		
D12	B4	138		
D13	C4	142		
D14	F6	143		
D15	B3	144		
$\overline{RD}$	D3	8	Output	<b>Read Enable (<math>\overline{RD}</math>)</b> — is asserted during external memory read cycles.  This signal is pulled high during reset.
$\overline{WR}$	D4	9	Output	<b>Write Enable (<math>\overline{WR}</math>)</b> —is asserted during external memory write cycles.  This signal is pulled high during reset.
$\overline{CS0}$ GPIOA0	H8	83	<b>Output</b>  <b>Input/Output</b>	<b>External Chip Select (<math>\overline{CS0}</math>)</b> —This pin is used as a dedicated GPIO.  <b>Port A GPIO (0)</b> —This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
$\overline{CS1}$ GPIOA1	H9	84	<b>Output</b>  <b>Input/Output</b>	<b>External Chip Select (<math>\overline{CS1}</math>)</b> —This pin is used as a dedicated GPIO.  <b>Port A GPIO (1)</b> —This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
$\overline{CS2}$ GPIOA2	H11	85	<b>Output</b>  <b>Input/Output</b>	<b>External Chip Select (<math>\overline{CS2}</math>)</b> —This pin is used as a dedicated GPIO.  <b>Port A GPIO (2)</b> —This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.

**Table 3. DSP56858 Signal and Package Information for the 144-pin LQFP and MAPBGA**

Signal Name	BGA Pin No.	LQFP Pin No.	Type	Description
$\overline{\text{CS3}}$ GPIOA3	H10	86	Output  Input/Output	<b>External Chip Select (<math>\overline{\text{CS3}}</math>)</b> —This pin is used as a dedicated GPIO.  <b>Port A GPIO (3)</b> —This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
HD0 GPIOB0	J3	33	Input  Input/Output	<b>Host Address (HD0)</b> —This input provides data selection for HI registers.  This pin is disconnected internally during reset.  <b>Port B GPIO (0)</b> —This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
HD1 GPIOB1	K2	34	Input  Input/Output	<b>Host Address (HD1)</b> —This input provides data selection for HI registers.  This pin is disconnected internally during reset.  <b>Port B GPIO (1)</b> —This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
HD2 GPIOB2	L2	35	Input  Input/Output	<b>Host Address (HD2)</b> —This input provides data selection for HI registers.  This pin is disconnected internally during reset.  <b>Port B GPIO (2)</b> —This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
HD3 GPIOB3	J4	40	Input  Input/Output	<b>Host Address (HD3)</b> —This input provides data selection for HI registers.  This pin is disconnected internally during reset.  <b>Port B GPIO (3)</b> —This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
HD4 GPIOB4	L4	41	Input  Input/Output	<b>Host Address (HD4)</b> —This input provides data selection for HI registers.  This pin is disconnected internally during reset.  <b>Port B GPIO (4)</b> —This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
HD5 GPIOB5	J5	42	Input  Input/Output	<b>Host Address (HD5)</b> —This input provides data selection for HI registers.  This pin is disconnected internally during reset.  <b>Port B GPIO (5)</b> —This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.

**Table 3. DSP56858 Signal and Package Information for the 144-pin LQFP and MAPBGA**

Signal Name	BGA Pin No.	LQFP Pin No.	Type	Description
HD6	K5	43	Input	<b>Host Address (HD6)</b> —This input provides data selection for HI registers.  This pin is disconnected internally during reset.
GPIOB6			Input/Output	<b>Port B GPIO (6)</b> —This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
HD7	H5	44	Input	<b>Host Address (HD7)</b> —This input provides data selection for HI registers.  This pin is disconnected internally during reset.
GPIOB7			Input/Output	<b>Port B GPIO (7)</b> —This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
HA0	G10	90	Input	<b>Host Address (HA0)</b> —These inputs provide the address selection for HI registers.  These pins are disconnected internally during reset.
GPIOB8			Input/Output	<b>Port B GPIO (8)</b> —These pins are General Purpose I/O (GPIO) pins when not configured for host port usage.
HA1	G11	91	Input	<b>Host Address (HA0)</b> —These inputs provide the address selection for HI registers.  These pins are disconnected internally during reset.
GPIOB9			Input/Output	<b>Port B GPIO (9)</b> —These pins are General Purpose I/O (GPIO) pins when not configured for host port usage.
HA2	G9	92	Input	<b>Host Address (HA0)</b> —These inputs provide the address selection for HI registers.  These pins are disconnected internally during reset.
GPIOB10			Input/Output	<b>Port B GPIO (10)</b> —These pins are General Purpose I/O (GPIO) pins when not configured for host port usage.
HRWB	G8	93	Input	<b>Host Read/Write (HRWB)</b> —When the HI08 is programmed to interface to a single-data-strobe host bus and the HI function is selected, this signal is the Read/Write input .  These pins are disconnected internally during reset.
$\overline{\text{HRD}}$			Input	<b>Host Read Data (<math>\overline{\text{HRD}}</math>)</b> —This signal is the Read Data input when the HI08 is programmed to interface to a double-data-strobe host bus and the HI function is selected.
GPIOB11			Input/Output	<b>Port B GPIO (11)</b> —This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.

**Table 3. DSP56858 Signal and Package Information for the 144-pin LQFP and MAPBGA**

Signal Name	BGA Pin No.	LQFP Pin No.	Type	Description
$\overline{\text{HDS}}$	C8	116	Input	<b>Host Data Strobe (<math>\overline{\text{HDS}}</math>)</b> —When the HI08 is programmed to interface to a single-data-strobe host bus and the HI function is selected, this input enables a data transfer on the HI when HCS is asserted.  These pins are disconnected internally during reset.
$\overline{\text{HWR}}$			Input	<b>Host Write Enable (<math>\overline{\text{HWR}}</math>)</b> —This signal is the Write Data input when the HI08 is programmed to interface to a double-data-strobe host bus and the HI function is selected.
GPIOB12			Input/Output	<b>Port B GPIO (12)</b> —This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
$\overline{\text{HCS}}$	D8	117	Input	<b>Host Chip Select (<math>\overline{\text{HCS}}</math>)</b> —This input is the chip select input for the Host Interface.  These pins are disconnected internally during reset.
GPIOB13			Input/Output	<b>Port B GPIO (13)</b> —This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
$\overline{\text{HREQ}}$	B8	118	Open Drain Output	<b>Host Request (<math>\overline{\text{HREQ}}</math>)</b> —When the HI08 is programmed for HRMS=0 functionality (typically used on a single-data-strobe bus), this open drain output is used by the HI to request service from the host processor. The HREQ may be connected to an interrupt request pin of a host processor, a transfer request of a DMA controller, or a control input of external circuitry.  These pins are disconnected internally during reset.
$\overline{\text{HTRQ}}$			Open Drain Output	<b>Transmit Host Request (<math>\overline{\text{HTRQ}}</math>)</b> —This signal is the Transmit Host Request output when the HI08 is programmed for HRMS=1 functionality and is typically used on a double-data-strobe bus.
GPIOB14			Input/Output	<b>Port B GPIO (14)</b> —This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.

**Table 3. DSP56858 Signal and Package Information for the 144-pin LQFP and MAPBGA**

Signal Name	BGA Pin No.	LQFP Pin No.	Type	Description
$\overline{\text{HACK}}$	C7	119	Input	<b>Host Acknowledge (HACK)</b> —When the HI08 is programmed for HRMS=0 functionality (typically used on a single-data-strobe bus), this input has two functions: (1) provide a Host Acknowledge signal for DMA transfers or (2) to control handshaking and provide a Host Interrupt Acknowledge compatible with the MC68000 family processors.  These pins are disconnected internally during reset.
HRRQ			Open Drain Output	<b>Receive Host Request (HRRQ)</b> —This signal is the Receive Host Request output when the HI08 is programmed for HRMS=1 functionality and is typically used on a double-data-strobe bus.
GPIOB15			Input/Output	<b>Port B GPIO (15)</b> —This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
TIO0	B9	114	Input/Output	<b>Timer Input/Outputs (TIO0)</b> —This pin can be independently configured to be either a timer input source or an output flag.
GPIOG0			Input/Output	<b>Port G GPIOG0</b> —This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as an input or output pin.
TIO1	C9	112	Input/Output	<b>Timer Input/Outputs (TIO1)</b> —This pin can be independently configured to be either a timer input source or an output flag.
GPIOG1			Input/Output	<b>Port G GPIO (1)</b> —This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as an input or output pin.
TIO2	D9	111	Input/Output	<b>Timer Input/Outputs (TIO2)</b> —This pin can be independently configured to be either a timer input source or an output flag.
GPIOG2			Input/Output	<b>Port G GPIO (2)</b> —This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as an input or output pin.
TIO3	B10	110	Input/Output	<b>Timer Input/Outputs (TIO3)</b> —This pin can be independently configured to be either a timer input source or an output flag.
GPIOG3			Input/Output	<b>Port G GPIO (3)</b> —This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as an input or output pin.
$\overline{\text{IRQA}}$	G2	22	Input	<b>External Interrupt Request A and B</b> —The $\overline{\text{IRQA}}$ and $\overline{\text{IRQB}}$ inputs are asynchronous external interrupt requests that indicate that an external device is requesting service. A Schmitt trigger input is used for noise immunity. They can be programmed to be level-sensitive or negative-edge-triggered. If level-sensitive triggering is selected, an external pull-up resistor is required for Wired-OR operation.
$\overline{\text{IRQB}}$	F5	23		

**Table 3. DSP56858 Signal and Package Information for the 144-pin LQFP and MAPBGA**

Signal Name	BGA Pin No.	LQFP Pin No.	Type	Description
MODE A GPIOH0	F4	17	Input  Input/Output	<b>Mode Select (MODE A)</b> —During the bootstrap process MODE A selects one of the eight bootstrap modes.  <b>Port H GPIO (0)</b> —This pin is a General Purpose I/O (GPIO) pin after the bootstrap process has completed.
MODE B GPIOH1	F3	18	Input  Input/Output	<b>Mode Select (MODE B)</b> —During the bootstrap process MODE A selects one of the eight bootstrap modes.  <b>Port H GPIO (1)</b> —This pin is a General Purpose I/O (GPIO) pin after the bootstrap process has completed.
MODE C GPIOH2	F2	19	Input  Input/Output	<b>Mode Select (MODE C)</b> —During the bootstrap process MODE A selects one of the eight bootstrap modes.  <b>Port H GPIO (2)</b> —This pin is a General Purpose I/O (GPIO) pin after the bootstrap process has completed.
$\overline{\text{RESET}}$	K4	39	Input	<b>Reset (RESET)</b> —This input is a direct hardware reset on the processor. When $\overline{\text{RESET}}$ is asserted low, the DSP is initialized and placed in the Reset state. A Schmitt trigger input is used for noise immunity. When the $\overline{\text{RESET}}$ pin is deasserted, the initial chip operating mode is latched from the MODE A, MODE B, and MODE C pins.  To ensure complete hardware reset, $\overline{\text{RESET}}$ and $\overline{\text{TRST}}$ should be asserted together. The only exception occurs in a debugging environment when a hardware DSP reset is required and it is necessary not to reset the JTAG/Enhanced OnCE module. In this case, assert $\overline{\text{RESET}}$ , but do not assert $\overline{\text{TRST}}$ .
$\overline{\text{RSTO}}$	K3	38	Output	<b>Reset Output (RSTO)</b> —This output is asserted on any reset condition (external reset, low voltage, software, or COP).
RXD0 GPIOE0	L10	73	Input  Input/Output	<b>Serial Receive Data 0 (RXD0)</b> —This input receives byte-oriented serial data and transfers it to the SCI 0 receive shift register.  <b>Port E GPIO (0)</b> —This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin.
TXD0 GPIOE1	L11	74	Output(Z)  Input/Output	<b>Serial Transmit Data 0 (TXD0)</b> —This signal transmits data from the SCI 0 transmit data register.  <b>Port E GPIO (1)</b> —This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin.
RXD1 GPIOE2	B11	107	Input  Input/Output	<b>Serial Receive Data 1 (RXD1)</b> —This input receives byte-oriented serial data and transfers it to the SCI 1 receive shift register.  <b>Port E GPIO (2)</b> —This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin.

**Table 3. DSP56858 Signal and Package Information for the 144-pin LQFP and MAPBGA**

Signal Name	BGA Pin No.	LQFP Pin No.	Type	Description
TXD1	C10	108	<b>Output(Z)</b>	<b>Serial Transmit Data 1 (TXD1)</b> —This signal transmits data from the SCI 1 transmit data register.
GPIOE3			Input/Output	<b>Port E GPIO (3)</b> —This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin.
STD0	B6	131	<b>Output</b>	<b>ESSI Transmit Data (STD0)</b> —This output pin transmits serial data from the ESSI Transmitter Shift Register.
GPIOC0			Input/Output	<b>Port C GPIO (0)</b> —This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.
SRD0	C6	132	<b>Input</b>	<b>ESSI Receive Data (SRD0)</b> —This input pin receives serial data and transfers the data to the ESSI Receive Shift Register.
GPIOC1			Input/Output	<b>Port C GPIO (1)</b> —This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.
SCK0	C5	133	<b>Input/Output</b>	<b>ESSI Serial Clock (SCK0)</b> —This bidirectional pin provides the serial bit rate clock for the transmit section of the ESSI. The clock signal can be continuous or gated and can be used by both the transmitter and receiver in synchronous mode.
GPIOC2			Input/Output	<b>Port C GPIO (2)</b> —This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.
SC00	D6	134	<b>Input/Output</b>	<b>ESSI Serial Control Pin 0 (SC00)</b> —The function of this pin is determined by the selection of either synchronous or asynchronous mode. For asynchronous mode, this pin will be used for the receive clock I/O. For synchronous mode, this pin is used either for transmitter1 output or for serial I/O flag 0.
GPIOC3			Input/Output	<b>Port C GPIO (3)</b> —This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.
SC01	B5	135	<b>Input/Output</b>	<b>ESSI Serial Control Pin 1 (SC01)</b> —The function of this pin is determined by the selection of either synchronous or asynchronous mode. For asynchronous mode, this pin is the receiver frame sync I/O. For synchronous mode, this pin is used either for transmitter2 output or for serial I/O flag 1.
GPIOC4			Input/Output	<b>Port C GPIO (4)</b> —This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.
SC02	E6	136	<b>Input/Output</b>	<b>ESSI Serial Control Pin 2 (SC02)</b> —This pin is used for frame sync I/O. SC02 is the frame sync for both the transmitter and receiver in synchronous mode and for the transmitter only in asynchronous mode. When configured as an output, this pin is the internally generated frame sync signal. When configured as an input, this pin receives an external frame sync signal for the transmitter (and the receiver in synchronous operation).
GPIOC5			Input or Output	<b>Port C GPIO (5)</b> —This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.



**Table 3. DSP56858 Signal and Package Information for the 144-pin LQFP and MAPBGA**

Signal Name	BGA Pin No.	LQFP Pin No.	Type	Description
STD1	E8	99	Output	<b>ESSI Transmit Data (STD1)</b> —This output pin transmits serial data from the ESSI Transmitter Shift Register.
GPIOD0			Input/Output	<b>Port D GPIO (0)</b> —This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.
SRD1	E11	100	Input	<b>ESSI Receive Data (SRD1)</b> —This input pin receives serial data and transfers the data to the ESSI Receive Shift Register.
GPIOD1			Input/Output	<b>Port D GPIO (1)</b> —This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.
SCK1	E9	101	Input/Output	<b>ESSI Serial Clock (SCK1)</b> —This bidirectional pin provides the serial bit rate clock for the transmit section of the ESSI. The clock signal can be continuous or gated and can be used by both the transmitter and receiver in synchronous mode.
GPIOD2			Input/Output	<b>Port D GPIO (2)</b> —This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.
SC10	D10	102	Input/Output	<b>ESSI Serial Control Pin 0 (SC10)</b> —The function of this pin is determined by the selection of either synchronous or asynchronous mode. For asynchronous mode, this pin will be used for the receive clock I/O. For synchronous mode, this pin is used either for transmitter1 output or for serial I/O flag 0.
GPIOD3			Input/Output	<b>Port D GPIO (3)</b> —This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.
SC11	D11	103	Input/Output	<b>ESSI Serial Control Pin 1 (SC11)</b> —The function of this pin is determined by the selection of either synchronous or asynchronous mode. For asynchronous mode, this pin is the receiver frame sync I/O. For synchronous mode, this pin is used either for transmitter2 output or for serial I/O flag 1.
GPIOD4			Input/Output	<b>Port D GPIO (4)</b> —This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.
SC12	C11	104	Input/Output	<b>ESSI Serial Control Pin 2 (SC12)</b> —This pin is used for frame sync I/O. SC02 is the frame sync for both the transmitter and receiver in synchronous mode and for the transmitter only in asynchronous mode. When configured as an output, this pin is the internally generated frame sync signal. When configured as an input, this pin receives an external frame sync signal for the transmitter (and the receiver in synchronous operation).
GPIOC5			Input/Output	<b>Port D GPIO (5)</b> —This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.

**Table 3. DSP56858 Signal and Package Information for the 144-pin LQFP and MAPBGA**

Signal Name	BGA Pin No.	LQFP Pin No.	Type	Description
MISO	B2	1	Input/Output	<b>SPI Master In/Slave Out (MISO)</b> —This serial data pin is an input to a master device and an output from a slave device. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected. The driver on this pin can be configured as an open-drain driver by the SPI's Wired-OR mode (WOM) bit when this pin is configured for SPI operation.
GPIOF0			Input/Output	<b>Port F GPIO (0)</b> —This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin.
MOSI	C3	2	Input/Output (Z)	<b>SPI Master Out/Slave In (MOSI)</b> —This serial data pin is an output from a master device and an input to a slave device. The master device places data on the MOSI line a half-cycle before the clock edge that the slave device uses to latch the data. The driver on this pin can be configured as an open-drain driver by the SPI's WOM bit when this pin is configured for SPI operation.
GPIOF1			Input/Output	<b>Port F GPIO (1)</b> —This pin is a General Purpose I/O (GPIO) pin that can be individually programmed as input or output pin.
SCK	C2	3	Input/Output	<b>SPI Serial Clock (SCK)</b> —This bidirectional pin provides a serial bit rate clock for the SPI. This gated clock signal is an input to a slave device and is generated as an output by a master device. Slave devices ignore the SCK signal unless the $\overline{SS}$ pin is active low. In both master and slave SPI devices, data is shifted on one edge of the SCK signal and is sampled on the opposite edge where data is stable. The driver on this pin can be configured as an open-drain driver by the SPI's WOM bit when this pin is configured for SPI operation. When using Wired-OR mode, the user must provide an external pull-up device.
GPIOF2			Input/Output	<b>Port F GPIO (2)</b> —This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin.
$\overline{SS}$	D2	4	Input	<b>SPI Slave Select (<math>\overline{SS}</math>)</b> —This input pin selects a slave device before a master device can exchange data with the slave device. $\overline{SS}$ must be low before data transactions and must stay low for the duration of the transaction. The $\overline{SS}$ line of the master must be held high.
GPIOF3			Input/Output	<b>Port F GPIO (3)</b> —This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin.
XTAL	H2	27	Input/Output	<b>Crystal Oscillator Output (XTAL)</b> —This output connects the internal crystal oscillator output to an external crystal. If an external clock source other than a crystal oscillator is used, XTAL must be used as the input.

**Table 3. DSP56858 Signal and Package Information for the 144-pin LQFP and MAPBGA**

Signal Name	BGA Pin No.	LQFP Pin No.	Type	Description
EXTAL	G3	28	Input	<b>External Crystal Oscillator Input (EXTAL)</b> —This input should be connected to an external crystal. If an external clock source other than a crystal oscillator is used, EXTAL must be tied off. See <a href="#">Section 4.5.2</a>
CLKO	L3	37	Output	<b>Clock Output (CLKO)</b> —This pin outputs a buffered clock signal. When enabled, this signal is the system clock divided by four.
TCK	L8	60	Input	<b>Test Clock Input (TCK)</b> —This input pin provides a gated clock to synchronize the test logic and to shift serial data to the JTAG/OnCE port. The pin is connected internally to a pull-down resistor.
TDI	K7	58	Input	<b>Test Data Input (TDI)</b> —This input pin provides a serial input data stream to the JTAG/OnCE port. It is sampled on the rising edge of TCK and has an on-chip pull-up resistor.
TDO	G6	57	Output (Z)	<b>Test Data Output (TDO)</b> —This tri-statable output pin provides a serial output data stream from the JTAG/Enhanced OnCE port. It is driven in the Shift-IR and Shift-DR controller states, and changes on the falling edge of TCK.
TMS	J7	59	Input	<b>Test Mode Select Input (TMS)</b> —This input pin is used to sequence the JTAG TAP controller's state machine. It is sampled on the rising edge of TCK and has an on-chip pull-up resistor.
$\overline{\text{TRST}}$	L7	56	Input	<b>Test Reset (<math>\overline{\text{TRST}}</math>)</b> —As an input, a low signal on this pin provides a reset signal to the JTAG TAP controller. To ensure complete hardware reset, $\overline{\text{TRST}}$ should be asserted whenever $\overline{\text{RESET}}$ is asserted. The only exception occurs in a debugging environment, since the Enhanced OnCE/JTAG module is under the control of the debugger. In this case it is not necessary to assert $\overline{\text{TRST}}$ when asserting $\overline{\text{RESET}}$ . Outside of a debugging environment $\overline{\text{RESET}}$ should be permanently asserted by grounding the signal, thus disabling the Enhanced OnCE/JTAG module on the DSP.
$\overline{\text{DE}}$	H6	55	Input/Output	<b>Debug Event (<math>\overline{\text{DE}}</math>)</b> —This is an open-drain, bidirectional, active low signal. As an input, it is a means of entering debug mode of operation from an external command controller. As an output, it is a means of acknowledging that the chip has entered debug mode.  This pin is connected internally to a weak pull-up resistor.

## Part 4 Specifications

### 4.1 General Characteristics

The DSP56858 is fabricated in high-density CMOS with 5-volt tolerant TTL-compatible digital inputs. The term “5-volt tolerant” refers to the capability of an I/O pin, built on a 3.3V compatible process technology, to withstand a voltage up to 5.5V without damaging the device. Many systems have a mixture of devices designed for 3.3V and 5V power supplies. In such systems, a bus may carry both 3.3V and 5V-compatible I/O voltage levels (a standard 3.3V I/O is designed to receive a maximum voltage of  $3.3V \pm 10\%$  during normal operation without causing damage). This 5V tolerant capability therefore offers the power savings of 3.3V I/O levels while being able to receive 5V levels without being damaged.

Absolute maximum ratings given in [Table 4](#) are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond these ratings may affect device reliability or cause permanent damage to the device.

The DSP56858 DC/AC electrical specifications are preliminary and are from design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. Finalized specifications will be published after complete characterization and device qualifications have been completed.

#### CAUTION

**This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.**

**Table 4. Absolute Maximum Ratings**

Characteristic	Symbol	Min	Max	Unit
Supply voltage, core	$V_{DD}^1$	$V_{SS} - 0.3$	$V_{SS} + 2.0$	V
Supply voltage, IO Supply voltage, analog	$V_{DDIO}^2$ $V_{DDIO}^2$	$V_{SSIO} - 0.3$ $V_{SSA} - 0.3$	$V_{SSIO} + 4.0$ $V_{DDA} + 4.0$	V
Digital input voltages Analog input voltages (XTAL, EXTAL)	$V_{IN}$ $V_{INA}$	$V_{SSIO} - 0.3$ $V_{SSA} - 0.3$	$V_{SSIO} + 5.5$ $V_{DDA} + 0.3$	V
Current drain per pin excluding $V_{DD}$ , GND	I	—	8	mA
Junction temperature	$T_J$	-40	120	°C
Storage temperature range	$T_{STG}$	-55	150	°C

1.  $V_{DD}$  must not exceed  $V_{DDIO}$
2.  $V_{DDIO}$  and  $V_{DDA}$  must not differ by more than 0.5V

**Table 5. Recommended Operating Conditions**

Characteristic	Symbol	Min	Max	Unit
Supply voltage for Logic Power	$V_{DD}$	1.62	1.98	V
Supply voltage for I/O Power	$V_{DDIO}$	3.0	3.6	V
Supply voltage for Analog Power	$V_{DDA}$	3.0	3.6	V
Ambient operating temperature	$T_A$	-40	85	°C
PLL clock frequency <sup>1</sup>	$f_{pll}$	—	240	MHz
Operating Frequency <sup>2</sup>	$f_{op}$	—	120	MHz
Frequency of peripheral bus	$f_{ipb}$	—	60	MHz
Frequency of external clock	$f_{clk}$	—	240	MHz
Frequency of oscillator	$f_{osc}$	2	4	MHz
Frequency of clock via XTAL	$f_{xtal}$	—	240	MHz
Frequency of clock via EXTAL	$f_{extal}$	2	4	MHz

1. Assumes clock source is direct clock to EXTAL or crystal oscillator running 2-4MHz. PLL must be enabled, locked, and selected. The actual frequency depends on the source clock frequency and programming of the CGM module.

2. Master clock is derived from on of the following four sources:

$f_{clk} = f_{xtal}$  when the source clock is the direct clock to EXTAL

$f_{clk} = f_{pll}$  when PLL is selected

$f_{clk} = f_{osc}$  when the source clock is the crystal oscillator and PLL is not selected

$f_{clk} = f_{extal}$  when the source clock is the direct clock to EXTAL and PLL is not selected

**Table 6. Thermal Characteristics<sup>1</sup>**

Characteristic	Symbol	Value		Unit
		144-pin LQFP	144 MAPBGA	
Thermal resistance junction-to-ambient (estimated)	$\theta_{JA}$	42.9	36.1	°C/W
I/O pin power dissipation	$P_{I/O}$	User Determined		W
Power dissipation	$P_D$	$P_D = (I_{DD} \times V_{DD}) + P_{I/O}$		W
Maximum allowed $P_D$	$P_{DMAX}$	$(T_J - T_A) / \theta_{JA}$		°C

1. See [Section 6.1](#) for more detail.

## 4.2 DC Electrical Characteristics

**Table 7. DC Electrical Characteristics**

Operating Conditions:  $V_{SS} = V_{SSIO} = V_{SSA} = 0\text{ V}$ ,  $V_{DD} = 1.62\text{--}1.98\text{ V}$ ,  $V_{DDIO} = V_{DDA} = 3.0\text{--}3.6\text{ V}$ ,  $T_A = -40^\circ\text{ to }+120^\circ\text{ C}$ ,  $C_L \leq 50\text{ pF}$ ,  $f_{op} = 120\text{ MHz}$

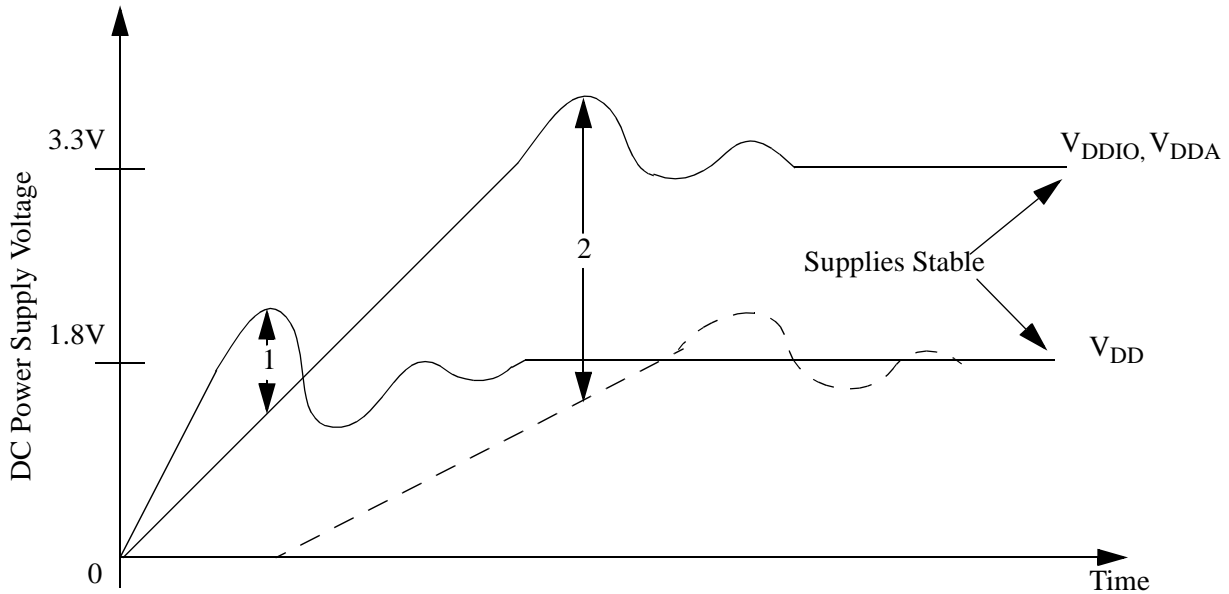
Characteristic	Symbol	Min	Typ	Max	Unit
Input high voltage (XTAL/EXTAL)	$V_{IHC}$	$V_{DDA} - 0.8$	$V_{DDA}$	$V_{DDA} + 0.3$	V
Input low voltage (XTAL/EXTAL)	$V_{ILC}$	-0.3	—	0.5	V
Input high voltage	$V_{IH}$	2.0	—	5.5	V
Input low voltage	$V_{IL}$	-0.3	—	0.8	V
Input current low (pullups disabled)	$I_{IL}$	-1	—	1	$\mu\text{A}$
Input current high (pullups disabled)	$I_{IH}$	-1	—	1	$\mu\text{A}$
Output tri-state current low	$I_{OZL}$	-10	—	10	$\mu\text{A}$
Output tri-state current high	$I_{OZH}$	-10	—	10	$\mu\text{A}$
Output High Voltage	$V_{OH}$	$V_{DD} - 0.7$	—	—	V
Output Low Voltage	$V_{OL}$	—	—	0.4	V
Output High Current	$I_{OH}$	8	—	16	mA
Output Low Current	$I_{OL}$	8	—	16	mA
Input capacitance	$C_{IN}$	—	8	—	pF
Output capacitance	$C_{OUT}$	—	12	—	pF
$V_{DD}$ supply current @ nominal voltage and 25 °C Run <sup>1</sup> Deep Stop <sup>2</sup> Light Stop <sup>3</sup>	$I_{DD}^4$	— — —	70 100 2.6	— — —	mA $\mu\text{A}$ mA
$V_{DDIO}$ supply current @ nominal voltage and 25 °C Run <sup>5</sup>	$I_{DDIO}$	—	40	—	mA
$V_{DDA}$ supply current @ nominal voltage and 25 °C Deep Stop <sup>2</sup>	$I_{DDA}$	—	60	—	$\mu\text{A}$
Low Voltage Interrupt <sup>6</sup>	$V_{EI}$	—	2.5	2.85	V
Low Voltage Interrupt Recovery Hysteresis	$V_{EIH}$	—	50	—	mV
Power on Reset <sup>7</sup>	POR	—	1.5	2.0	V

1. Run (operating)  $I_{DD}$  measured using external square wave clock source ( $f_{osc} = 4\text{ MHz}$ ) into XTAL. All inputs 0.2V from rail; no DC loads; outputs unloaded. All ports configured as inputs; measured with all modules enabled. PLL set to 240MHz out. Running Core, performing 50% NOP and 50% FIR. Clock at 120 MHz.

2. Deep Stop Mode - Operation frequency = 4 MHz, PLL set to 4 MHz, crystal oscillator and time of day module operating.
3. Light Stop Mode - Operation frequency = 120 MHz, PLL set to 240 MHz, crystal oscillator and time of day module operating.
4.  $I_{DD}$  includes current for core logic, internal memories, and all internal peripheral logic circuitry.
5. Running core and performing external memory access. Clock at 120 MHz.
6. When  $V_{DD}$  drops below  $V_{EI}$  max value, an interrupt is generated.
7. Power-on reset occurs whenever the digital supply drops below 1.8V. While power is ramping up, this signal remains active for as long as the internal 2.5V is below 1.8V no matter how long the ramp up rate is. The internally regulated voltage is typically 100 mV less than  $V_{DD}$  during ramp up until 2.5V is reached, at which time it self-regulates.

### 4.3 Supply Voltage Sequencing and Separation Cautions

Figure 3 shows two situations to avoid in sequencing the  $V_{DD}$  and  $V_{DDIO}$ ,  $V_{DDA}$  supplies.



- Notes:**
1.  $V_{DD}$  rising before  $V_{DDIO}$ ,  $V_{DDA}$
  2.  $V_{DDIO}$ ,  $V_{DDA}$  rising much faster than  $V_{DD}$

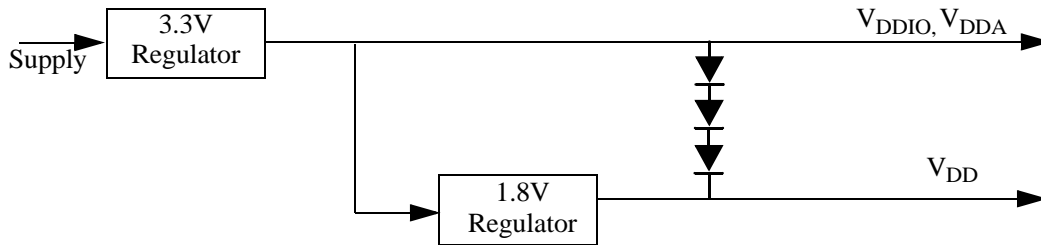
**Figure 3. Supply Voltage Sequencing and Separation Cautions**

$V_{DD}$  should not be allowed to rise early (1). This is usually avoided by running the regulator for the  $V_{DD}$  supply (1.8V) from the voltage generated by the 3.3V  $V_{DDIO}$  supply, see Figure 4. This keeps  $V_{DD}$  from rising faster than  $V_{DDIO}$ .

$V_{DD}$  should not rise so late that a large voltage difference is allowed between the two supplies (2). Typically this situation is avoided by using external discrete diodes in series between supplies, as shown in Figure 4. The series diodes forward bias when the difference between  $V_{DDIO}$  and  $V_{DD}$  reaches approximately 2.1, causing  $V_{DD}$  to rise as  $V_{DDIO}$  ramps up. When the  $V_{DD}$  regulator begins proper operation, the difference between supplies will typically be 0.8V and conduction through the diode chain reduces to essentially leakage current. During supply sequencing, the following general relationship should be adhered to:

$$V_{DDIO} \geq V_{DD} \geq (V_{DDIO} - 2.1V)$$

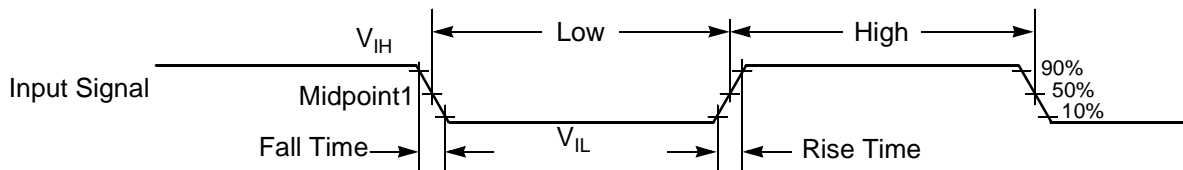
In practice,  $V_{DDA}$  is typically connected directly to  $V_{DDIO}$  with some filtering.



**Figure 4. Example Circuit to Control Supply Sequencing**

## 4.4 AC Electrical Characteristics

Timing waveforms in [Section 4.3](#) are tested with a  $V_{IL}$  maximum of 0.8V and a  $V_{IH}$  minimum of 2.0V for all pins except XTAL, which is tested using the input levels in [Section 4.2](#). In [Figure 5](#) the levels of  $V_{IH}$  and  $V_{IL}$  for an input signal are shown.

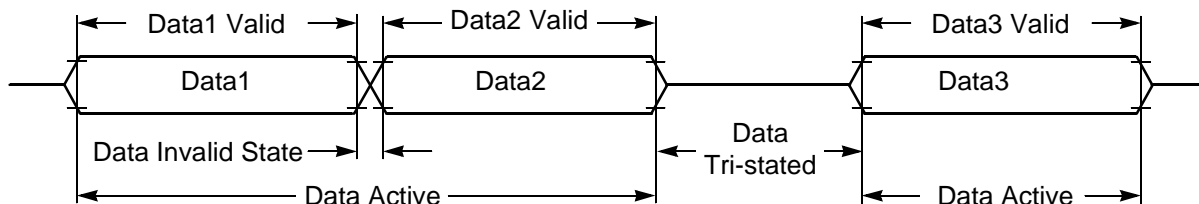


Note: The midpoint is  $V_{IL} + (V_{IH} - V_{IL})/2$ .

**Figure 5. Input Signal Measurement References**

[Figure 6](#) shows the definitions of the following signal states:

- Active state, when a bus or signal is driven, and enters a low impedance state
- Tri-stated, when a bus or signal is placed in a high impedance state
- Data Valid state, when a signal level has reached  $V_{OL}$  or  $V_{OH}$
- Data Invalid state, when a signal level is in transition between  $V_{OL}$  and  $V_{OH}$



**Figure 6. Signal States**



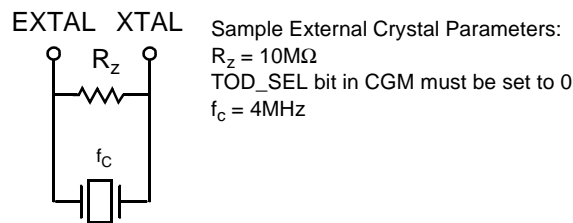
## 4.5 External Clock Operation

The DSP56858 system clock can be derived from a crystal or an external system clock signal. To generate a reference frequency using the internal oscillator, a reference crystal must be connected between the EXTAL and XTAL pins.

### 4.5.1 Crystal Oscillator

The internal oscillator is designed to interface with a parallel-resonant crystal resonator in the frequency range specified for the external crystal in [Table 9](#). In [Figure 7](#) a typical crystal oscillator circuit is shown. Follow the crystal supplier's recommendations when selecting a crystal, because crystal parameters determine the component values required to provide maximum stability and reliable start-up. The crystal and associated components should be mounted as close as possible to the EXTAL and XTAL pins to minimize output distortion and start-up stabilization time.

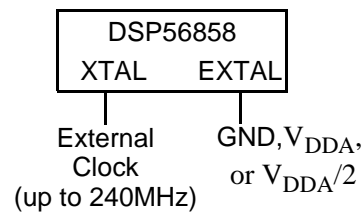
**Crystal Frequency = 2–4MHz (optimized for 4MHz)**



**Figure 7. Crystal Oscillator**

### 4.5.2 High Speed External Clock Source (> 4MHz)

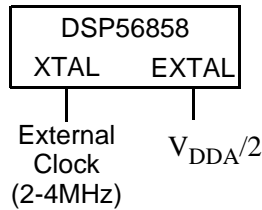
The recommended method of connecting an external clock is given in [Figure 8](#). The external clock source is connected to XTAL and the EXTAL pin is held at ground,  $V_{DDA}$ , or  $V_{DDA}/2$ . The TOD\_SEL bit in CGM must be set to 0.



**Figure 8. Connecting a High Speed External Clock Signal using XTAL**

### 4.5.3 Low Speed External Clock Source (2-4MHz)

The recommended method of connecting an external clock is given in [Figure 9](#). The external clock source is connected to XTAL and the EXTAL pin is held at  $V_{DDA}/2$ . The TOD\_SEL bit in CGM must be set to 0.



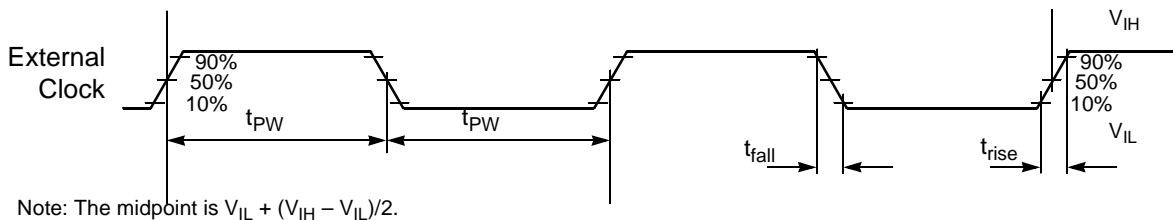
**Figure 9. Connecting a Low Speed External Clock Signal using XTAL**

**Table 8. External Clock Operation Timing Requirements<sup>4</sup>**

Operating Conditions:  $V_{SS} = V_{SSIO} = V_{SSA} = 0\text{ V}$ ,  $V_{DD} = 1.62\text{--}1.98\text{ V}$ ,  $V_{DDIO} = V_{DDA} = 3.0\text{--}3.6\text{ V}$ ,  $T_A = -40^\circ\text{ to }+120^\circ\text{ C}$ ,  $C_L \leq 50\text{ pF}$ ,  $f_{op} = 120\text{ MHz}$

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency of operation (external clock driver) <sup>1</sup>	$f_{osc}$	0	—	240	MHz
Clock Pulse Width <sup>4</sup>	$t_{PW}$	6.25	—	—	ns
External clock input rise time <sup>2, 4</sup>	$t_{rise}$	—	—	TBD	ns
External clock input fall time <sup>3, 4</sup>	$t_{fall}$	—	—	TBD	ns

1. See [Figure 8](#) for details on using the recommended connection of an external clock driver.
2. External clock input rise time is measured from 10% to 90%.
3. External clock input fall time is measured from 90% to 10%.
4. Parameters listed are guaranteed by design.



**Figure 10. External Clock Timing**

**Table 9. PLL Timing**

Operating Conditions:  $V_{SS} = V_{SSIO} = V_{SSA} = 0\text{ V}$ ,  $V_{DD} = 1.62\text{--}1.98\text{ V}$ ,  $V_{DDIO} = V_{DDA} = 3.0\text{--}3.6\text{ V}$ ,  $T_A = -40^\circ\text{ to }+120^\circ\text{ C}$ ,  $C_L \leq 50\text{ pF}$ ,  $f_{op} = 120\text{ MHz}$

Characteristic	Symbol	Min	Typ	Max	Unit
External reference crystal frequency for the PLL <sup>1</sup>	$f_{osc}$	2	4	4	MHz
PLL output frequency	$f_{clk}$	40	—	240	MHz
PLL stabilization time <sup>2</sup>	$t_{plls}$	—	1	10	ms

1. An externally supplied reference clock should be as free as possible from any phase jitter for the PLL to work correctly. The PLL is optimized for 4MHz input crystal.
2. This is the minimum time required after the PLL setup is changed to ensure reliable operation.

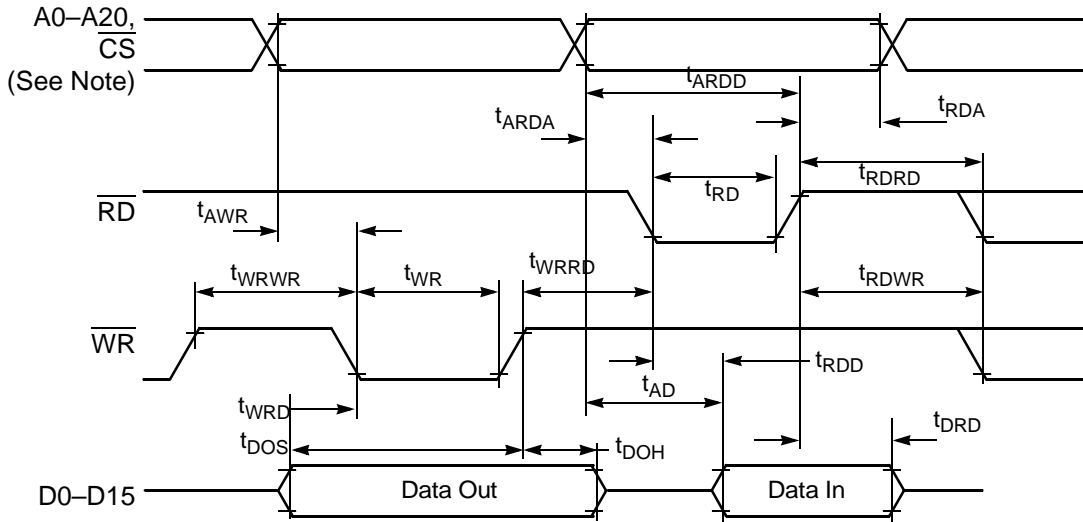
## 4.6 External Memory Interface Timing

**Table 10. External Memory Interface Timing 1, 2**

Operating Conditions:  $V_{SS} = V_{SSIO} = V_{SSA} = 0\text{ V}$ ,  $V_{DD} = 1.62\text{--}1.98\text{ V}$ ,  $V_{DDIO} = V_{DDA} = 3.0\text{--}3.6\text{ V}$ ,  $T_A = -40^\circ\text{ to }+120^\circ\text{C}$ ,  $C_L \leq 50\text{ pF}$ ,  $f_{op} = 120\text{ MHz}$ ,  $T_{OP} = 8.3$ ,  $F_{IPB} = 60\text{ MHz}$ ,  $T_{IPB} = 16.6$

Characteristic	Symbol	Typical Min	Typical Max	Unit
Address Valid to $\overline{WR}$ Asserted	$t_{AWR}$	4.36	—	ns
$\overline{WR}$ Width Asserted Wait states $\geq 1$	$t_{WR}$	$(T_{IPB} * WS) - .81$	—	ns
D0–D15 Out Valid to $\overline{WR}$ Asserted	$t_{WRD}$	4.57	—	ns
Data Out Hold Time from $\overline{WR}$ Deasserted	$t_{DOH}$	5.37	—	ns
Data Out Set Up Time to $\overline{WR}$ Deasserted Wait states $\geq 1$	$t_{DOS}$	$(T_{IPB} * WS) + 4.76$	—	ns
$\overline{RD}$ Deasserted to Address Not Valid	$t_{RDA}$	12.65	—	ns
Address Valid to $\overline{RD}$ Deasserted Wait states $\geq 1$	$t_{ARDD}$	$(T_{IPB} * WS) - 2.28$	—	ns
Input Data Hold to $\overline{RD}$ Deasserted	$t_{DRD}$	0	—	ns
$\overline{RD}$ Assertion Width Wait states $\geq 1$	$t_{RD}$	$(T_{IPB} * WS) - 1.58$	—	ns
Address Valid to Input Data Valid Wait states $\geq 1$	$t_{AD}$	—	$(T_{IPB} * WS) - 21.76$	ns
Address Valid to $\overline{RD}$ Asserted	$t_{ARDA}$	-1.70	—	ns
$\overline{RD}$ Asserted to Input Data Valid Wait states $\geq 1$	$t_{RDD}$	—	$(T_{IPB} * WS) - 21.06$	ns
$\overline{WR}$ Deasserted to $\overline{RD}$ Asserted	$t_{WRRD}^4$	$T_{OP}$	—	ns
$\overline{RD}$ Deasserted to $\overline{RD}$ Asserted	$t_{RDRD}^4$	$T_{OP} \times 2$	—	ns
$\overline{WR}$ Deasserted to $\overline{WR}$ Asserted	$t_{WRWR}^4$	$T_{OP} \times 2$	—	ns
$\overline{RD}$ Deasserted to $\overline{WR}$ Asserted	$t_{RDWR}^4$	$T_{OP} \times 3$	—	ns

1. Timing is both wait state and frequency dependent. In the formulas listed, WS = the number of wait states (min. 1) and  $T_{op}$  = System Clock Period.
2. Parameters listed are guaranteed by design.
3. EMI operates at  $f_{ipb}$  rate. Wait states are in terms of  $f_{ipb}$  periods.
4. Shows separation of R/W enables in system cycles ( $T_{op}$ ) in data space using consecutive one-word assembly language instructions.



Note: During read-modify-write instructions and internal instructions, the address lines do not change state.

**Figure 11. External Memory Interface Timing**

## 4.7 Reset, Stop, Wait, Mode Select, and Interrupt Timing

**Table 11. Reset, Stop, Wait, Mode Select, and Interrupt Timing<sup>1, 2</sup>**

Operating Conditions:  $V_{SS} = V_{SSIO} = V_{SSA} = 0\text{ V}$ ,  $V_{DD} = 1.62\text{--}1.98\text{ V}$ ,  $V_{DDIO} = V_{DDA} = 3.0\text{--}3.6\text{ V}$ ,  $T_A = -40^\circ\text{ to }+120^\circ\text{ C}$ ,  $C_L \leq 50\text{ pF}$ ,  $f_{op} = 120\text{ MHz}$

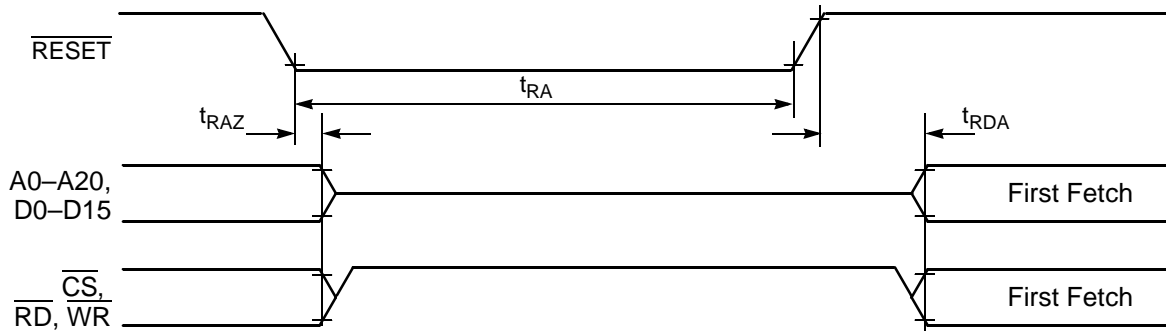
Characteristic	Symbol	Typical Min	Typical Max	Unit	See Figure
$\overline{\text{RESET}}$ Assertion to Address, Data and Control Signals High Impedance	$t_{\text{RAZ}}$	—	11	ns	Figure 12
Minimum $\overline{\text{RESET}}$ Assertion Duration <sup>3</sup>	$t_{\text{RA}}$	30	—	ns	Figure 12
$\overline{\text{RESET}}$ Deassertion to First External Address Output	$t_{\text{RDA}}$	—	120T	ns	Figure 12
Edge-sensitive Interrupt Request Width	$t_{\text{IRW}}$	1T + 3	—	ns	Figure 13
$\overline{\text{IRQA}}$ , $\overline{\text{IRQB}}$ Assertion to External Data Memory Access Out Valid, caused by first instruction execution in the interrupt service routine	$t_{\text{IDM}}$	—	18T	ns	Figure 14
$\overline{\text{IRQA}}$ , $\overline{\text{IRQB}}$ Assertion to General Purpose Output Valid, caused by first instruction execution in the interrupt service routine	$t_{\text{IG}}$	—	18T	ns	Figure 14
$\overline{\text{IRQA}}$ Low to First Valid Interrupt Vector Address Out recovery from Wait State <sup>4</sup>	$t_{\text{IRI}}$	—	13T	ns	Figure 15
$\overline{\text{IRQA}}$ Width Assertion to Recover from Stop State <sup>5</sup>	$t_{\text{IW}}$				
Fast <sup>6</sup>		4T	—	ns	Figure 16
Normal <sup>7, 8</sup>		8ET	—	ns	

**Table 11. Reset, Stop, Wait, Mode Select, and Interrupt Timing<sup>1, 2</sup>**

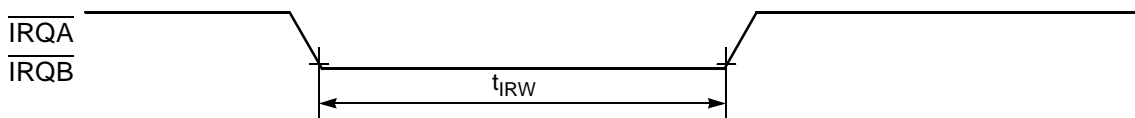
Operating Conditions:  $V_{SS} = V_{SSIO} = V_{SSA} = 0V$ ,  $V_{DD} = 1.62\text{--}1.98V$ ,  $V_{DDIO} = V_{DDA} = 3.0\text{--}3.6V$ ,  $T_A = -40^\circ$  to  $+120^\circ\text{C}$ ,  $C_L \leq 50\text{pF}$ ,  $f_{op} = 120\text{MHz}$

Characteristic	Symbol	Typical Min	Typical Max	Unit	See Figure
Delay from $\overline{\text{IRQA}}$ Assertion to Fetch of first instruction (exiting Stop) Fast <sup>5</sup> Normal <sup>6,7</sup>	$t_{IF}$	— —	13T 25ET	ns ns	Figure 16
$\overline{\text{RSTO}}$ pulse width <sup>7</sup> normal operation internal reset mode	$t_{RSTO}$	128ET 8ET	— —	— —	Figure 17

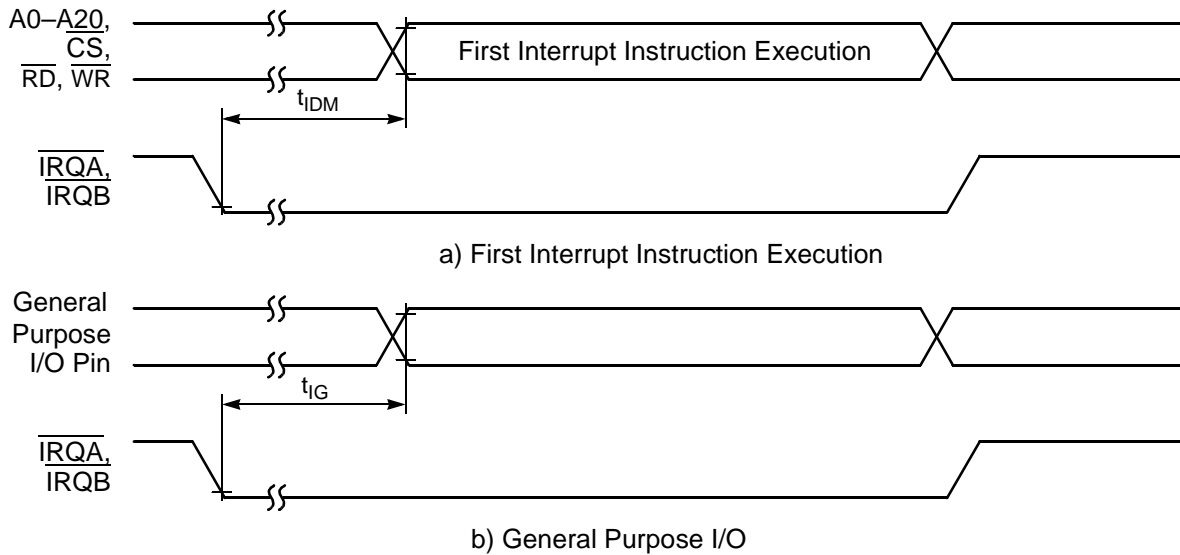
1. In the formulas, T = clock cycle. For  $f_{op} = 120\text{MHz}$  operation and  $f_{ipb} = 60\text{MHz}$ ,  $T = 8.33\text{ns}$ .
2. Parameters listed are guaranteed by design.
3. At reset, the PLL is disabled and bypassed. The part is then put into Run mode and  $t_{clk}$  assumes the period of the source clock,  $t_{xtal}$ ,  $t_{extal}$  or  $t_{osc}$ .
4. The minimum is specified for the duration of an edge-sensitive IRQA interrupt required to recover from the Wait state. This is not the minimum required so that the IRQA interrupt is accepted.
5. This interrupt instruction fetch is visible on the pins only in Mode 3.
6. Fast stop mode:  
Fast stop recovery applies when fast stop mode recovery is requested (OMR bit 6 is set to 1). The PLL and the master clock are unaffected by stop mode entry. Recovery takes one less cycle and  $t_{clk}$  will continue with the same value it had before stop mode was entered.
7. Normal stop mode:  
As a power saving feature, normal stop mode disables and bypasses the PLL. Stop mode will then shut down the master clock, recovery will take an extra cycle (to restart the clock), and  $t_{clk}$  will resume at the input clock source rate.
8. ET = External Clock period; for an external crystal frequency of 4MHz, ET=250ns.



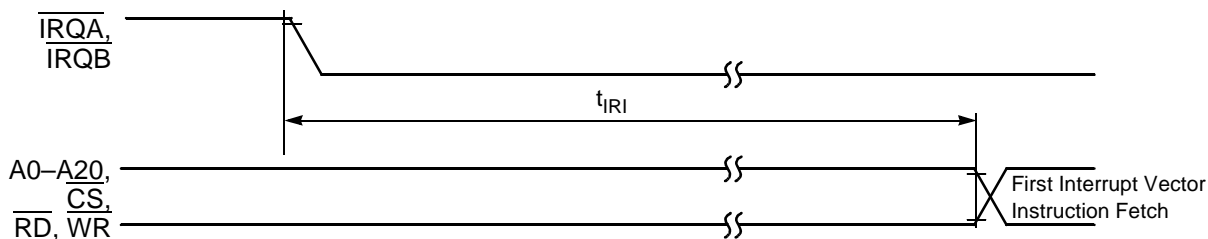
**Figure 12. Asynchronous Reset Timing**



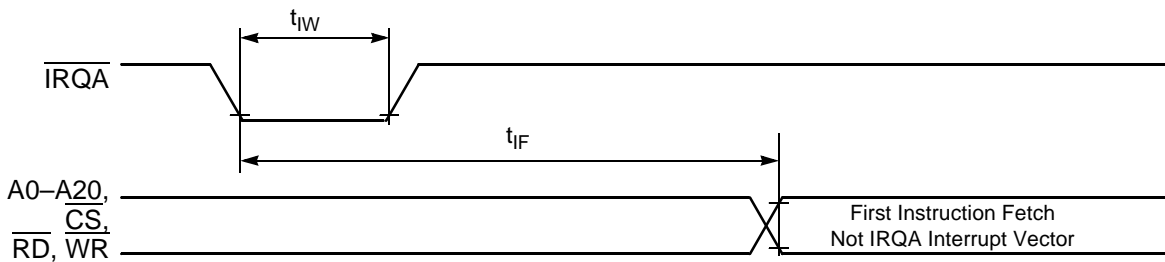
**Figure 13. External Interrupt Timing (Negative-Edge-Sensitive)**



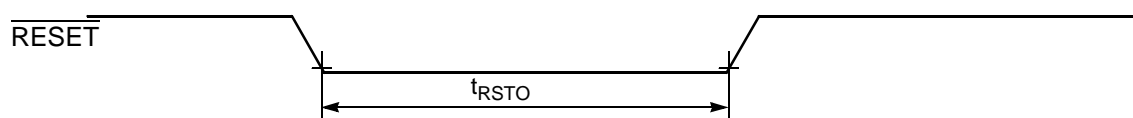
**Figure 14. External Level-Sensitive Interrupt Timing**



**Figure 15. Interrupt from Wait State Timing**



**Figure 16. Recovery from Stop State Using Asynchronous Interrupt Timing**



**Figure 17. Reset Output Timing**

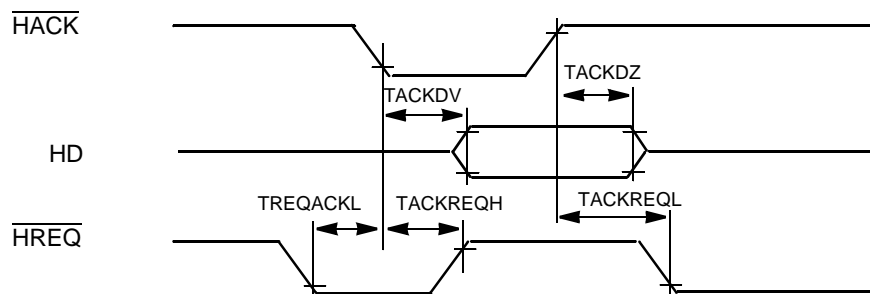
## 4.8 Host Interface Port

**Table 12. Host Interface Port Timing<sup>1</sup>**

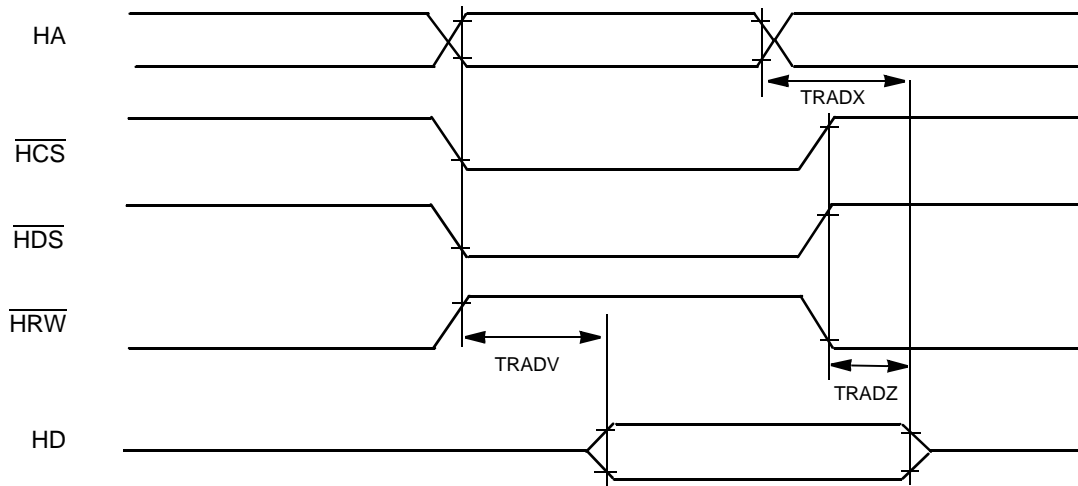
Operating Conditions:  $V_{SS} = V_{SSIO} = V_{SSA} = 0\text{ V}$ ,  $V_{DD} = 1.62\text{--}1.98\text{ V}$ ,  $V_{DDIO} = V_{DDA} = 3.0\text{--}3.6\text{ V}$ ,  $T_A = -40^\circ\text{ to }+120^\circ\text{ C}$ ,  $C_L \leq 50\text{ pF}$ ,  $f_{op} = 120\text{ MHz}$

Characteristic	Symbol	Min	Max	Unit	See Figure
Access time	TACKDV	—	13	ns	Figure 18
Disable time	TACKDZ	3	—	ns	Figure 18
Time to disassert	TACKREQH	3.5	9	ns	Figure 18 Figure 21
Lead time	TREQACKL	0	—	ns	Figure 18 Figure 21
Access time	TRADV	—	13	ns	Figure 19 Figure 20
Disable time	TRADX	5	—	ns	Figure 19 Figure 20
Disable time	TRADZ	3	—	ns	Figure 19 Figure 20
Setup time	TDACKS	3	—	ns	Figure 21
Hold time	TACKDH	1	—	ns	Figure 21
Setup time	TADSS	3	—	ns	Figure 22 Figure 23
Hold time	TDSAH	1	—	ns	Figure 22 Figure 23
Pulse width	TWDS	5	—	ns	Figure 22 Figure 23
Time to re-assert 1. After second write in 16-bit mode 2. After first write in 16-bit mode or after write in 8-bit mode	TACKREQL	4T + 5 5	5T + 9 13	ns ns	Figure 18, Figure 21

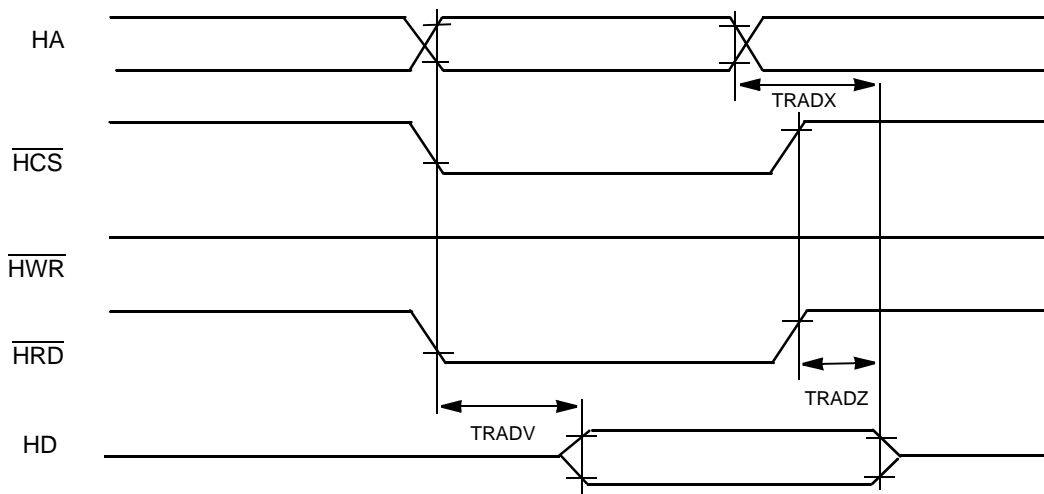
1. The formulas:  $T = \text{clock cycle}$ ,  $f_{ipb} = 60\text{ MHz}$ ,  $T = 16.7\text{ ns}$ .



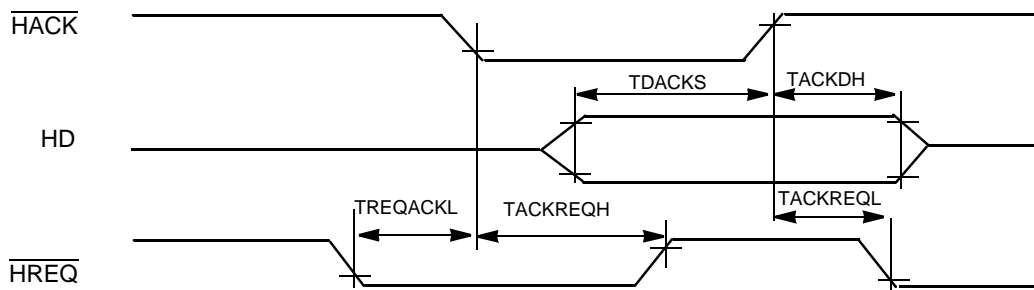
**Figure 18. DSP-to-Host DMA Read Mode**



**Figure 19. Single Strobe Read Mode**



**Figure 20. Dual Strobe Read Mode**



**Figure 21. Host-to-DSP DMA Write Mode**



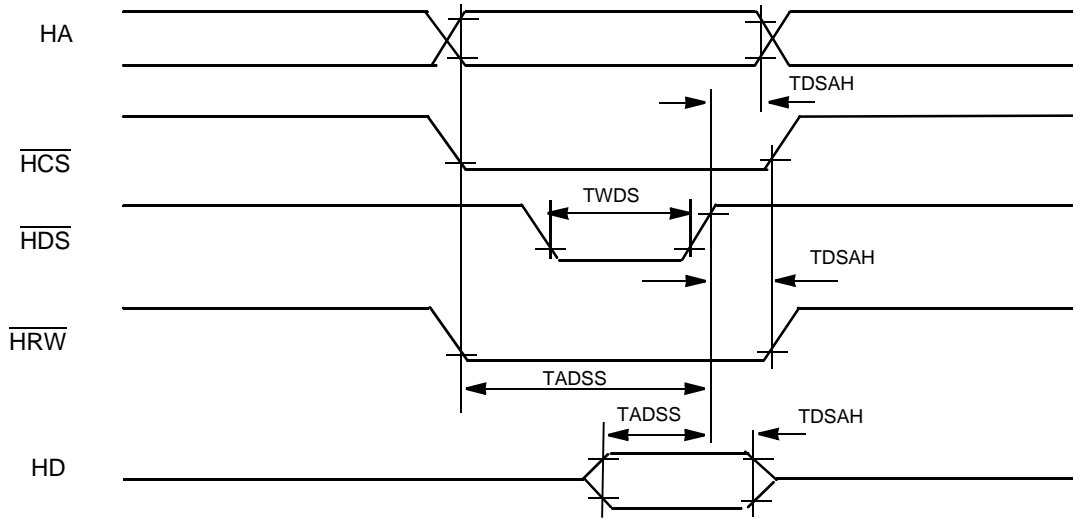


Figure 22. Single Strobe Write Mode

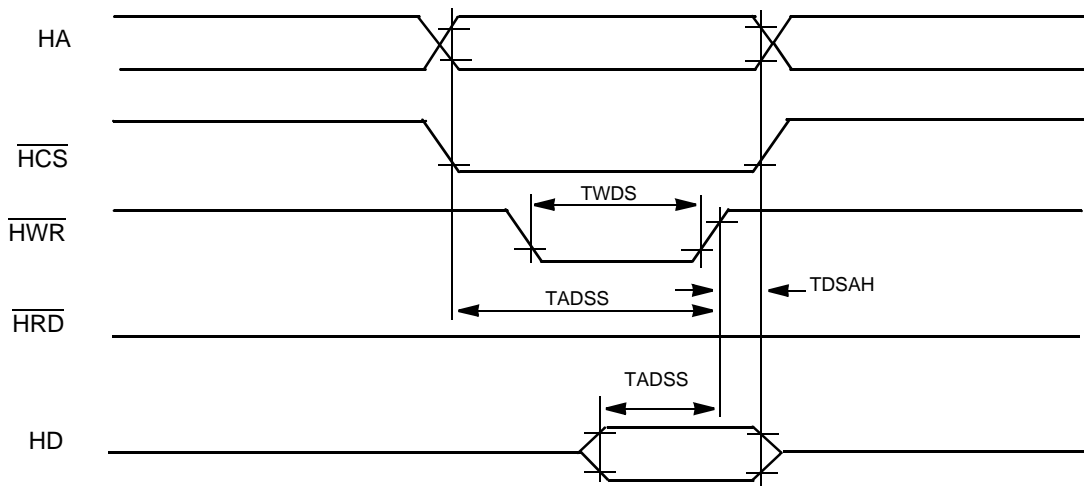


Figure 23. Dual Strobe Write Mode

## 4.9 Serial Peripheral Interface (SPI) Timing

**Table 13. SPI Timing <sup>1</sup>**

Operating Conditions:  $V_{SS} = V_{SSIO} = V_{SSA} = 0\text{ V}$ ,  $V_{DD} = 1.62\text{--}1.98\text{ V}$ ,  $V_{DDIO} = V_{DDA} = 3.0\text{--}3.6\text{ V}$ ,  $T_A = -40^\circ\text{ to }+120^\circ\text{ C}$ ,  $C_L \leq 50\text{ pF}$ ,  $f_{op} = 120\text{ MHz}$

Characteristic	Symbol	Min	Max	Unit	See Figure
Cycle time Master Slave	$t_C$	25 25	— —	ns ns	Figures 24, 25, 26, 27
Enable lead time Master Slave	$t_{ELD}$	— 12.5	— —	ns ns	Figure 27
Enable lag time Master Slave	$t_{ELG}$	— 12.5	— —	ns ns	Figure 27
Clock (SCLK) high time Master Slave	$t_{CH}$	9 12.5	— —	ns ns	Figures 24, 25, 26, 27
Clock (SCLK) low time Master Slave	$t_{CL}$	12 12.5	— —	ns ns	Figure 27
Data set-up time required for inputs Master Slave	$t_{DS}$	10 2	— —	ns ns	Figures 24, 25, 26, 27
Data hold time required for inputs Master Slave	$t_{DH}$	0 2	— —	ns ns	Figures 24, 25, 26, 27
Access time (time to data active from high-impedance state) Slave	$t_A$	5	15	ns ns	Figure 27
Disable time (hold time to high-impedance state) Slave	$t_D$	2	9	ns ns	Figure 27
Data valid for outputs Master Slave (after enable edge)	$t_{DV}$	— —	2 14	ns ns	Figures 24, 25, 26, 27
Data invalid Master Slave	$t_{DI}$	0 0	— —	ns ns	Figures 24, 25, 26, 27
Rise time Master Slave	$t_R$	— —	11.5 10.0	ns ns	Figures 24, 25, 26, 27
Fall time Master Slave	$t_F$	— —	9.7 9.0	ns ns	Figures 24, 25, 26, 27

1. Parameters listed are guaranteed by design.

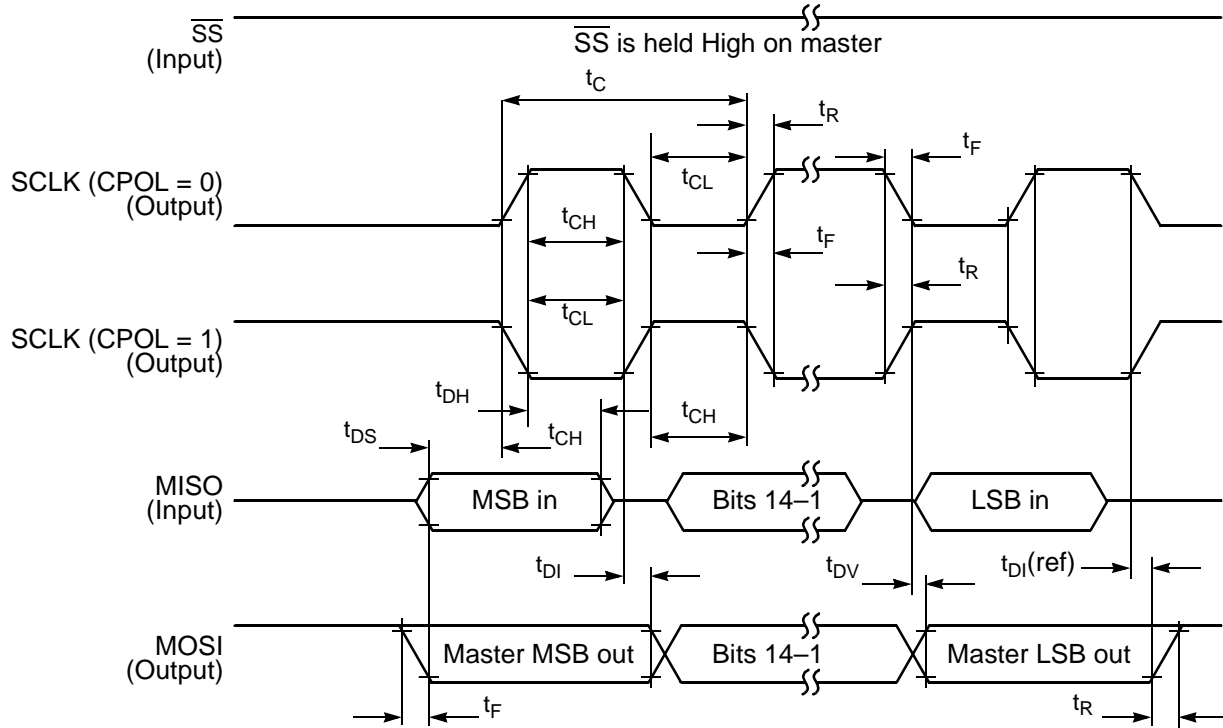


Figure 24. SPI Master Timing (CPHA = 0)

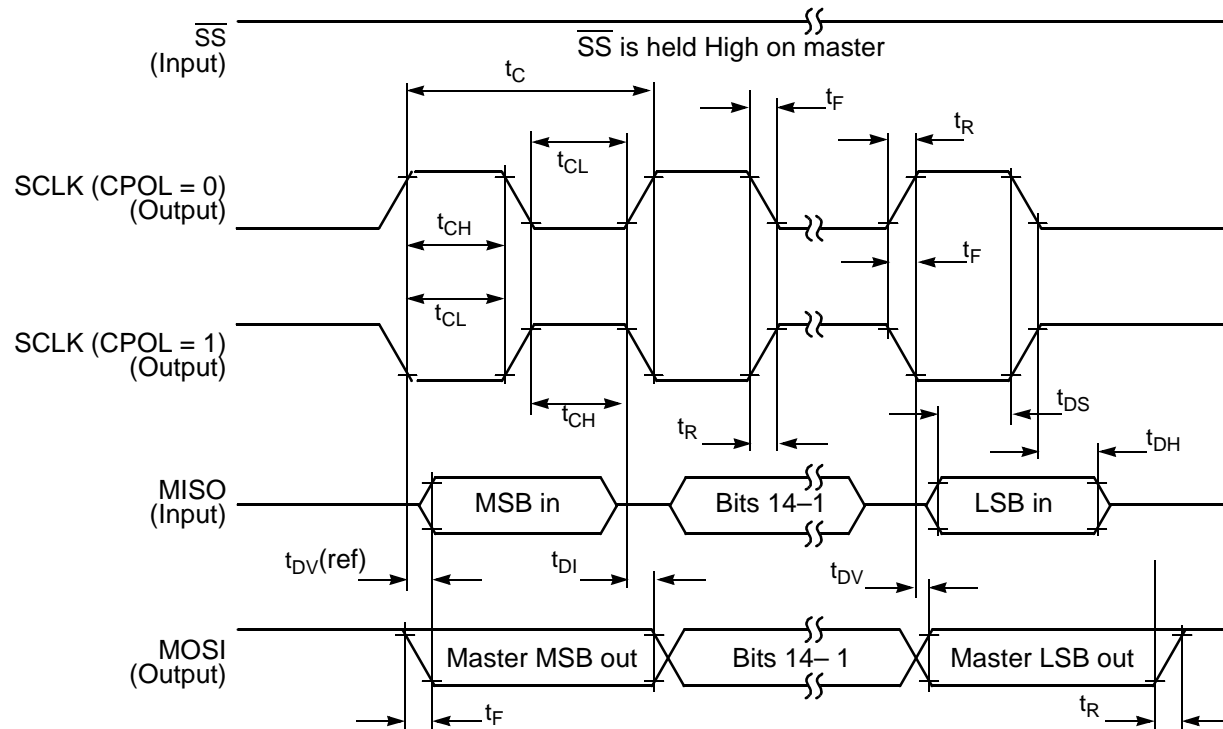


Figure 25. SPI Master Timing (CPHA = 1)

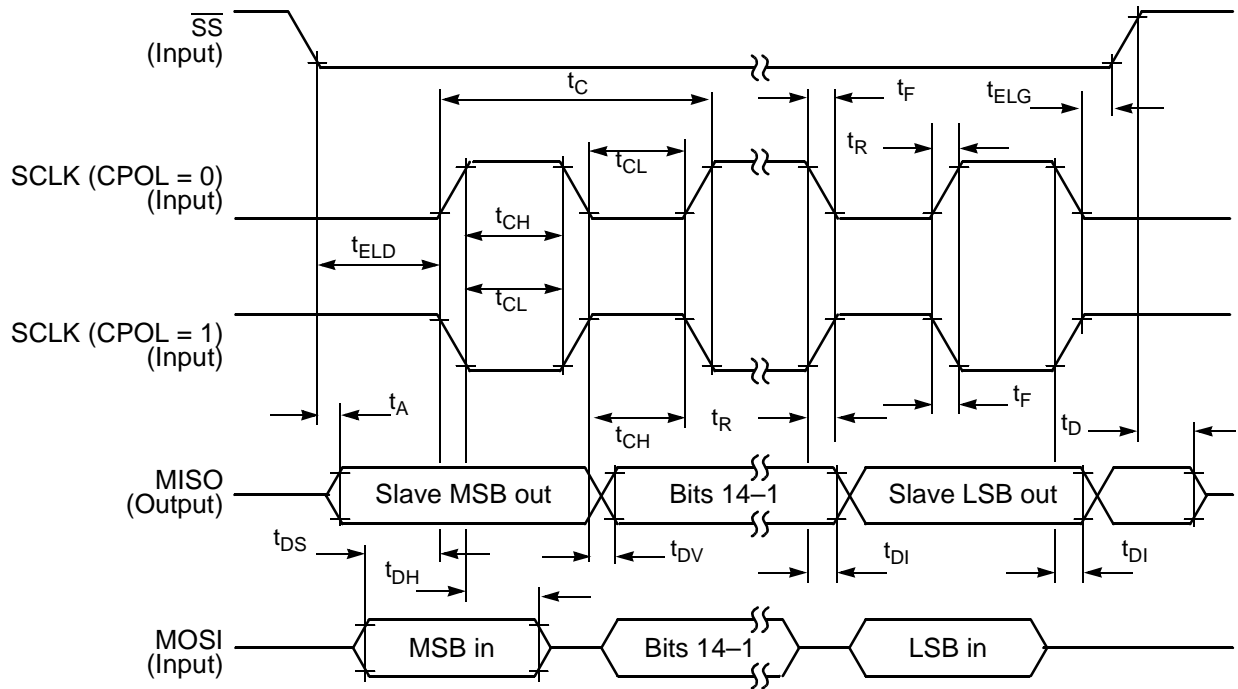


Figure 26. SPI Slave Timing (CPHA = 0)

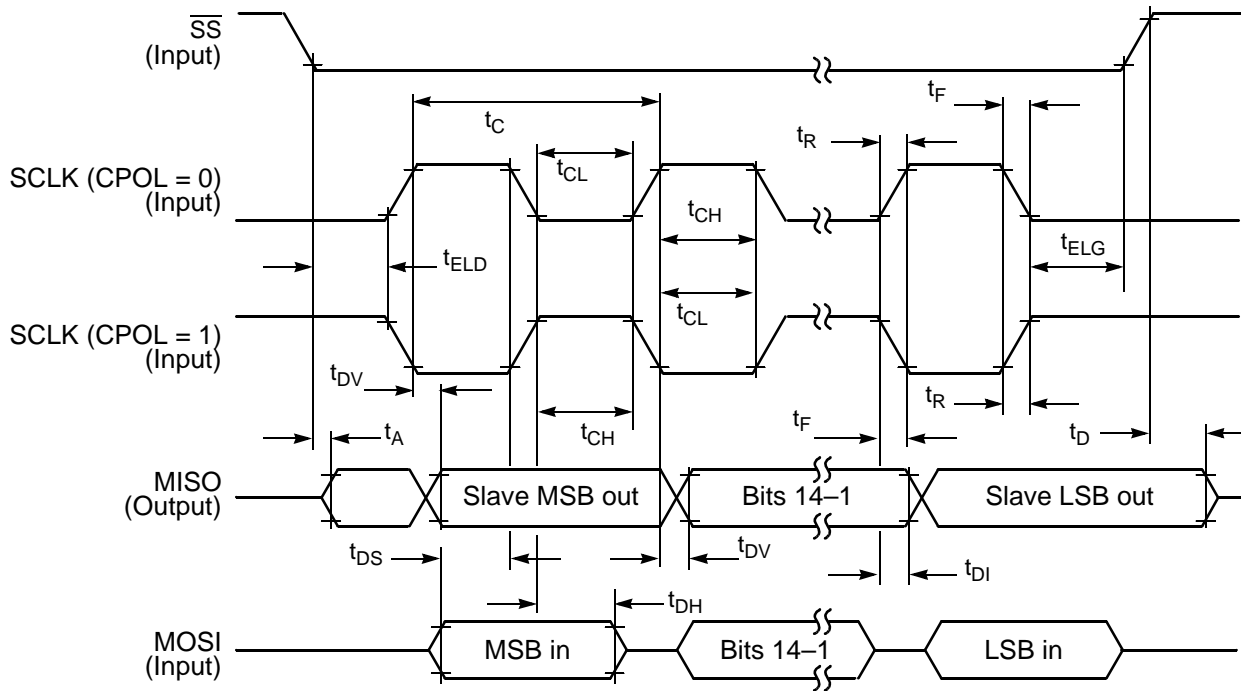


Figure 27. SPI Slave Timing (CPHA = 1)

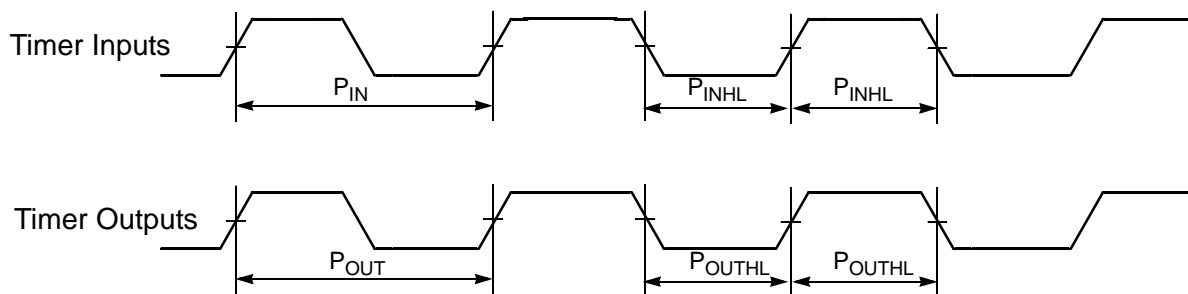
## 4.10 Quad Timer Timing

**Table 14. Quad Timer Timing<sup>1, 2</sup>**

Operating Conditions:  $V_{SS} = V_{SSIO} = V_{SSA} = 0\text{ V}$ ,  $V_{DD} = 1.62\text{--}1.98\text{ V}$ ,  $V_{DDIO} = V_{DDA} = 3.0\text{--}3.6\text{ V}$ ,  $T_A = -40^\circ\text{ to }+120^\circ\text{ C}$ ,  $C_L \leq 50\text{ pF}$ ,  $f_{op} = 120\text{ MHz}$

Characteristic	Symbol	Min	Max	Unit
Timer input period	$P_{IN}$	$2T + 3$	—	ns
Timer input high/low period	$P_{INHL}$	$1T + 3$	—	ns
Timer output period	$P_{OUT}$	$2T - 3$	—	ns
Timer output high/low period	$P_{OUTHL}$	$1T - 3$	—	ns

1. In the formulas listed,  $T$  = clock cycle. For  $f_{op} = 120\text{ MHz}$  operation and  $f_{ipb} = 60\text{ MHz}$ ,  $T = 8.33\text{ ns}$ .
2. Parameters listed are guaranteed by design.



**Figure 28. Timer Timing**

## Enhanced Synchronous Serial Interface (ESSI) Timing

**Table 15. ESSI Master Mode<sup>1</sup> Switching Characteristics**

Operating Conditions:  $V_{SS} = V_{SSIO} = V_{SSA} = 0\text{ V}$ ,  $V_{DD} = 1.62\text{--}1.98\text{ V}$ ,  $V_{DDIO} = V_{DDA} = 3.0\text{--}3.6\text{ V}$ ,  $T_A = -40^\circ\text{ to }+120^\circ\text{ C}$ ,  $C_L \leq 50\text{ pF}$ ,  $f_{op} = 120\text{ MHz}$

Parameter	Symbol	Min	Typ	Max	Units
SCK frequency	$f_s$	—	—	$15^2$	MHz
SCK period <sup>3</sup>	$t_{SCKW}$	66.7	—	—	ns
SCK high time	$t_{SCKH}$	33.4 <sup>4</sup>	—	—	ns
SCK low time	$t_{SCKL}$	33.4 <sup>4</sup>	—	—	ns
Output clock rise/fall time	—	—	4	—	ns
Delay from SCK high to SC2 (bl) high - Master <sup>5</sup>	$t_{TFSBHM}$	-1.0	—	1.0	ns
Delay from SCK high to SC2 (wl) high - Master <sup>5</sup>	$t_{TFSWHM}$	-1.0	—	1.0	ns
Delay from SC0 high to SC1 (bl) high - Master <sup>5</sup>	$t_{RFSBHM}$	-1.0	—	1.0	ns
Delay from SC0 high to SC1 (wl) high - Master <sup>5</sup>	$t_{RFSWHM}$	-1.0	—	1.0	ns
Delay from SCK high to SC2 (bl) low - Master <sup>5</sup>	$t_{TFSBLM}$	-1.0	—	1.0	ns

**Table 15. ESSI Master Mode<sup>1</sup> Switching Characteristics(Continued)**

Operating Conditions:  $V_{SS} = V_{SSIO} = V_{SSA} = 0V$ ,  $V_{DD} = 1.62-1.98V$ ,  $V_{DDIO} = V_{DDA} = 3.0-3.6V$ ,  $T_A = -40^\circ$  to  $+120^\circ C$ ,  $C_L \leq 50pF$ ,  $f_{op} = 120MHz$

Parameter	Symbol	Min	Typ	Max	Units
Delay from SCK high to SC2 (wl) low - Master <sup>5</sup>	$t_{TFSWLM}$	-1.0	—	1.0	ns
Delay from SC0 high to SC1 (bl) low - Master <sup>5</sup>	$t_{RFSBLM}$	-1.0	—	1.0	ns
Delay from SC0 high to SC1 (wl) low - Master <sup>5</sup>	$t_{RFSWLM}$	-1.0	—	1.0	ns
SCK high to STD enable from high impedance - Master	$t_{TXEM}$	-0.1	—	2	ns
SCK high to STD valid - Master	$t_{TXVM}$	-0.1	—	2	ns
SCK high to STD not valid - Master	$t_{TXNVM}$	-0.1	—	—	ns
SCK high to STD high impedance - Master	$t_{TXHIM}$	-4	—	0	ns
SRD Setup time before SC0 low - Master	$t_{SM}$	4	—	—	ns
SRD Hold time after SC0 low - Master	$t_{HM}$	4	—	—	ns
<b>Synchronous Operation (in addition to standard internal clock parameters)</b>					
SRD Setup time before SCK low - Master	$t_{TSM}$	4	—	—	ns
SRD Hold time after SCK low - Master	$t_{THM}$	4	—	—	ns

1. Master mode is internally generated clocks and frame syncs
2. Max clock frequency is  $IP\_clk/4 = 60MHz / 4 = 15MHz$  for an 120MHz part.
3. All the timings for the ESSI are given for a non-inverted serial clock polarity (TSCKP=0 in SCR2 and RSCKP=0 in SCSR) and a non-inverted frame sync (TFSI=0 in SCR2 and RFSI=0 in SCSR). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal SCK/SC0 and/or the frame sync SC2/SC1 in the tables and in the figures.
4. 50 percent duty cycle
5. bl = bit length; wl = word length

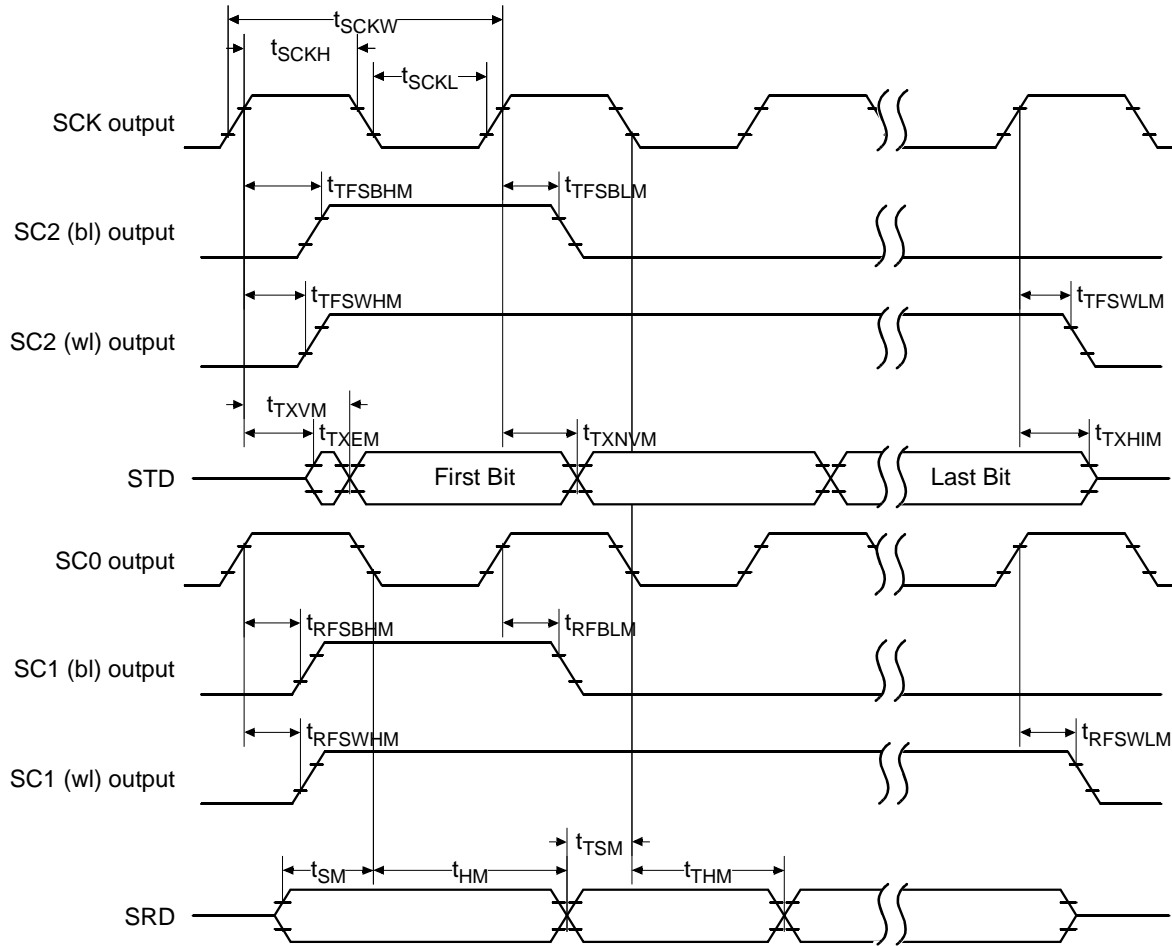


Figure 29. Master Mode Timing Diagram

Table 16: ESSI Slave Mode<sup>1</sup> Switching Characteristics

Operating Conditions:  $V_{SS} = V_{SSIO} = V_{SSA} = 0\text{ V}$ ,  $V_{DD} = 1.62\text{--}1.98\text{ V}$ ,  $V_{DDIO} = V_{DDA} = 3.0\text{--}3.6\text{ V}$ ,  $T_A = -40^\circ\text{ to }+120^\circ\text{ C}$ ,  $C_L \leq 50\text{ pF}$ ,  $f_{op} = 120\text{ MHz}$

Parameter	Symbol	Min	Typ	Max	Units
SCK frequency	$f_s$	—	—	$15^2$	MHz
SCK period <sup>3</sup>	$t_{SCKW}$	66.7	—	—	ns
SCK high time	$t_{SCKH}$	$33.4^4$	—	—	ns
SCK low time	$t_{SCKL}$	$33.4^4$	—	—	ns
Output clock rise/fall time	—	—	4	—	ns
Delay from SCK high to SC2 (bl) high - Slave <sup>5</sup>	$t_{TFSBHS}$	-1	—	29	ns
Delay from SCK high to SC2 (wl) high - Slave <sup>5</sup>	$t_{TFSWHS}$	-1	—	29	ns
Delay from SC0 high to SC1 (bl) high - Slave <sup>5</sup>	$t_{RFSBHS}$	-1	—	29	ns

**Table 16: ESSI Slave Mode<sup>1</sup> Switching Characteristics(Continued)**Operating Conditions:  $V_{SS} = V_{SSIO} = V_{SSA} = 0V$ ,  $V_{DD} = 1.62-1.98V$ ,  $V_{DDIO} = V_{DDA} = 3.0-3.6V$ ,  $T_A = -40^\circ$  to  $+120^\circ C$ ,  $C_L \leq 50pF$ ,  $f_{op} = 120MHz$ 

Parameter	Symbol	Min	Typ	Max	Units
Delay from SC0 high to SC1 (wl) high - Slave <sup>5</sup>	$t_{RFSWHS}$	-1	—	29	ns
Delay from SCK high to SC2 (bl) low - Slave <sup>5</sup>	$t_{TFSBLS}$	-29	—	29	ns
Delay from SCK high to SC2 (wl) low - Slave <sup>5</sup>	$t_{TFSWLS}$	-29	—	29	ns
Delay from SC0 high to SC1 (bl) low - Slave <sup>5</sup>	$t_{RFSBLS}$	-29	—	29	ns
Delay from SC0 high to SC1 (wl) low - Slave <sup>5</sup>	$t_{RFSWLS}$	-29	—	29	ns
SCK high to STD enable from high impedance - Slave	$t_{TXES}$	—	—	15	ns
SCK high to STD valid - Slave	$t_{TXVS}$	4	—	15	ns
SC2 high to STD enable from high impedance (first bit) - Slave	$t_{FTXES}$	4	—	15	ns
SC2 high to STD valid (first bit) - Slave	$t_{FTXVS}$	4	—	15	ns
SCK high to STD not valid - Slave	$t_{TXNVS}$	4	—	15	ns
SCK high to STD high impedance - Slave	$t_{TXHIS}$	4	—	15	ns
SRD Setup time before SC0 low - Slave	$t_{SS}$	4	—	—	ns
SRD Hold time after SC0 low - Slave	$t_{HS}$	4	—	—	ns
<b>Synchronous Operation (in addition to standard external clock parameters)</b>					
SRD Setup time before SCK low - Slave	$t_{TSS}$	4	—	—	ns
SRD Hold time after SCK low - Slave	$t_{THS}$	4	—	—	ns

1. Slave mode is externally generated clocks and frame syncs
2. Max clock frequency is  $IP\_clk/4 = 60MHz / 4 = 15MHz$  for a 120MHz part.
3. All the timings for the ESSI are given for a non-inverted serial clock polarity ( $TSCKP=0$  in SCR2 and  $RSCKP=0$  in SCSR) and a non-inverted frame sync ( $TFSI=0$  in SCR2 and  $RFSI=0$  in SCSR). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal SCK/SC0 and/or the frame sync SC2/SC1 in the tables and in the figures.
4. 50 percent duty cycle
5. bl = bit length; wl = word length



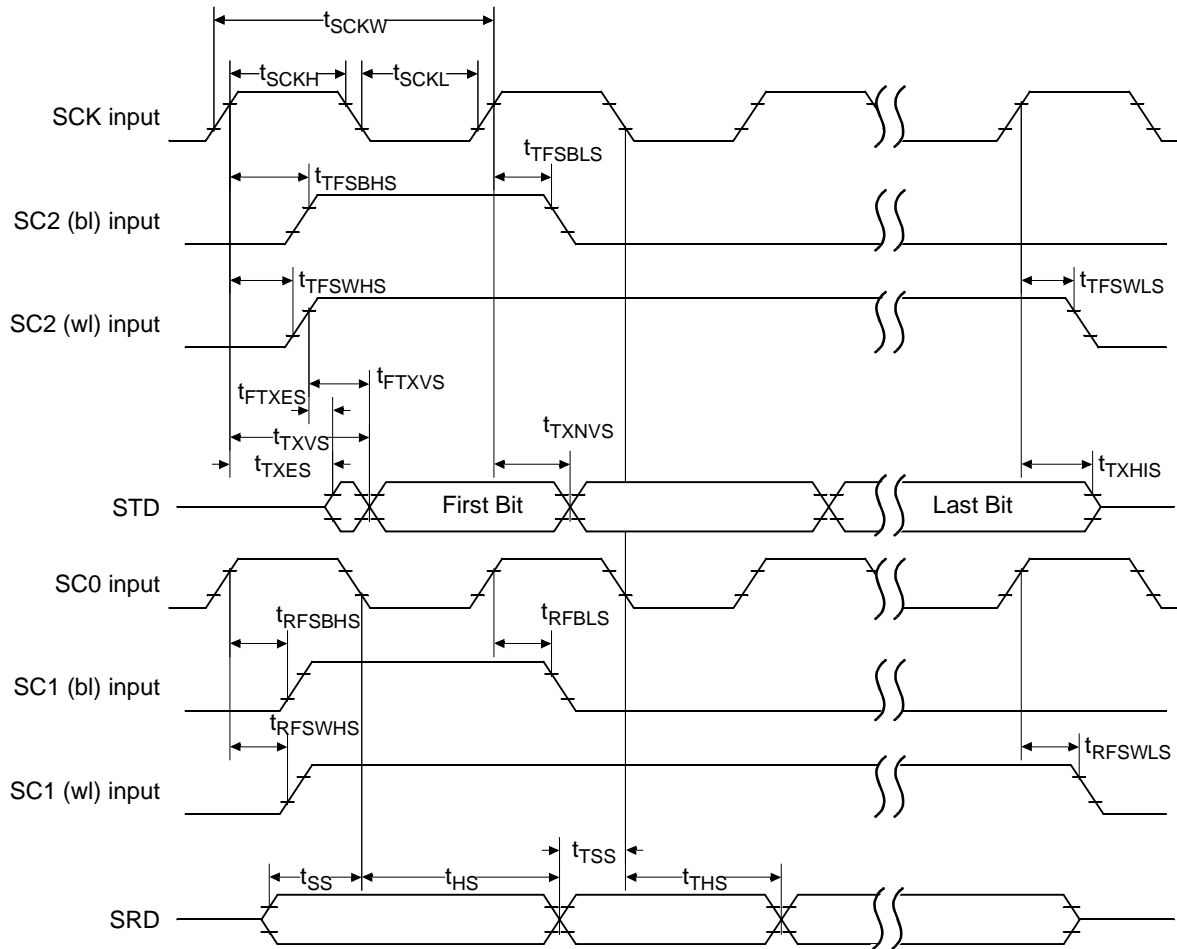


Figure 30. Slave Mode Clock Timing

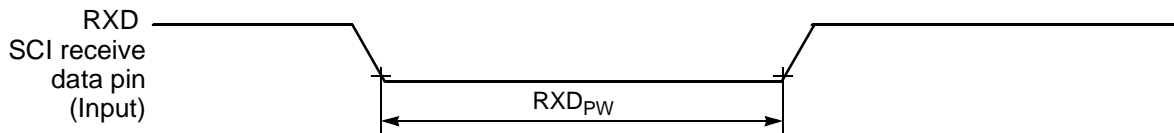
## 4.11 Serial Communication Interface (SCI) Timing

Table 17. SCI Timing<sup>4</sup>

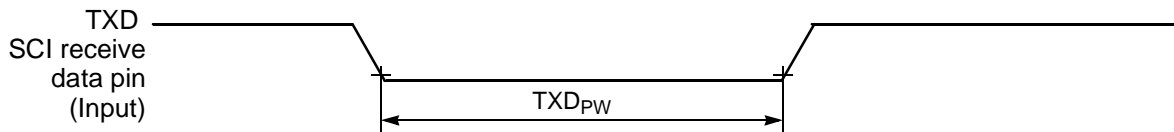
Operating Conditions:  $V_{SS} = V_{SSIO} = V_{SSA} = 0\text{ V}$ ,  $V_{DD} = 1.62\text{--}1.98\text{ V}$ ,  $V_{DDIO} = V_{DDA} = 3.0\text{--}3.6\text{ V}$ ,  $T_A = -40^\circ\text{ to }+120^\circ\text{ C}$ ,  $C_L \leq 50\text{ pF}$ ,  $f_{op} = 120\text{ MHz}$

Characteristic	Symbol	Min	Max	Unit
Baud Rate <sup>1</sup>	BR	—	$(f_{MAX})/(32)$	Mbps
RXD <sup>2</sup> Pulse Width	$RXD_{PW}$	$0.965/BR$	$1.04/BR$	ns
TXD <sup>3</sup> Pulse Width	$TXD_{PW}$	$0.965/BR$	$1.04/BR$	ns

- $f_{MAX}$  is the frequency of operation of the system clock in MHz.
- The RXD pin in SCI0 is named RXD0 and the RXD pin in SCI1 is named RXD1.
- The TXD pin in SCI0 is named TXD0 and the TXD pin in SCI1 is named TXD1.
- Parameters listed are guaranteed by design.



**Figure 31. RXD Pulse Width**



**Figure 32. TXD Pulse Width**

## 4.12 JTAG Timing

**Table 18. JTAG Timing<sup>1, 3</sup>**

Operating Conditions:  $V_{SS} = V_{SSIO} = V_{SSA} = 0\text{ V}$ ,  $V_{DD} = 1.62\text{--}1.98\text{ V}$ ,  $V_{DDIO} = V_{DDA} = 3.0\text{--}3.6\text{ V}$ ,  $T_A = -40^\circ\text{ to }+120^\circ\text{ C}$ ,  $C_L \leq 50\text{ pF}$ ,  $f_{op} = 120\text{ MHz}$

Characteristic	Symbol	Min	Max	Unit
TCK frequency of operation <sup>2</sup>	$f_{OP}$	DC	30	MHz
TCK cycle time	$t_{CY}$	33.3	—	ns
TCK clock pulse width	$t_{PW}$	16.6	—	ns
TMS, TDI data setup time	$t_{DS}$	3	—	ns
TMS, TDI data hold time	$t_{DH}$	3	—	ns
TCK low to TDO data valid	$t_{DV}$	—	12	ns
TCK low to TDO tri-state	$t_{TS}$	—	10	ns
$\overline{\text{TRST}}$ assertion time	$t_{TRST}$	35	—	ns
$\overline{\text{DE}}$ assertion time	$t_{DE}$	4T	—	ns

1. Timing is both wait state and frequency dependent. For the values listed, T = clock cycle. For 120MHz operation, T = 8.33ns.
2. TCK frequency of operation must be less than 1/4 the processor rate.
3. Parameters listed are guaranteed by design.

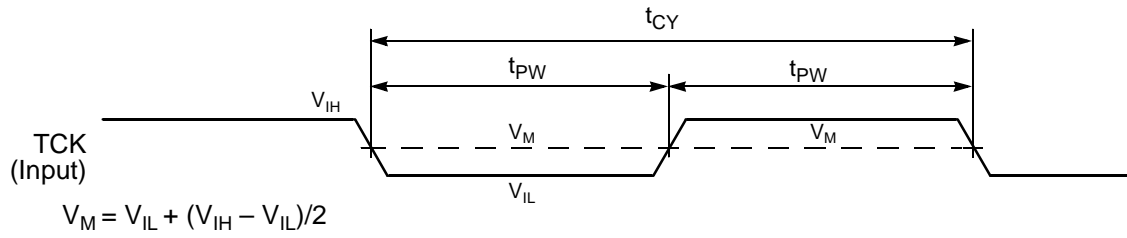


Figure 33. Test Clock Input Timing Diagram

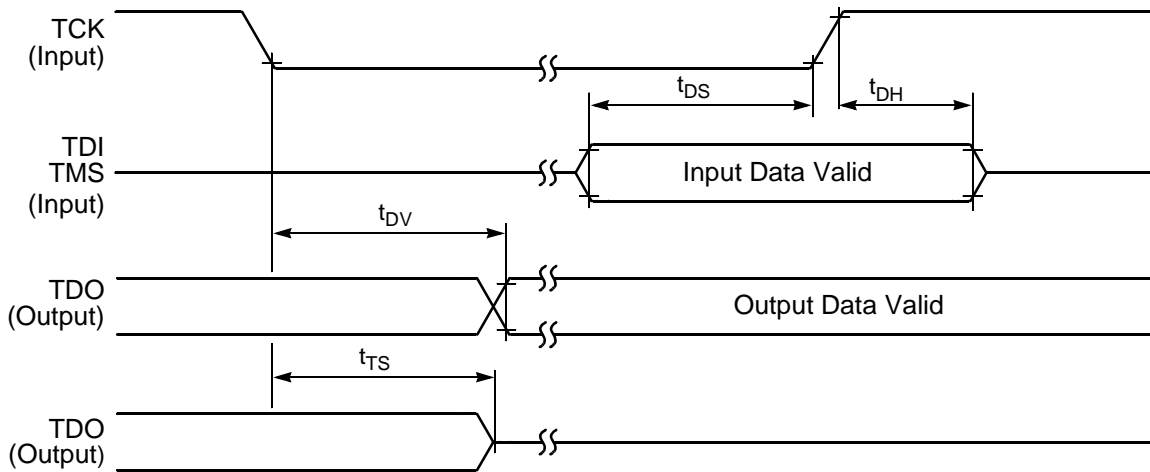


Figure 34. Test Access Port Timing Diagram



Figure 35.  $\overline{\text{TRST}}$  Timing Diagram



Figure 36. Enhanced OnCE—Debug Event

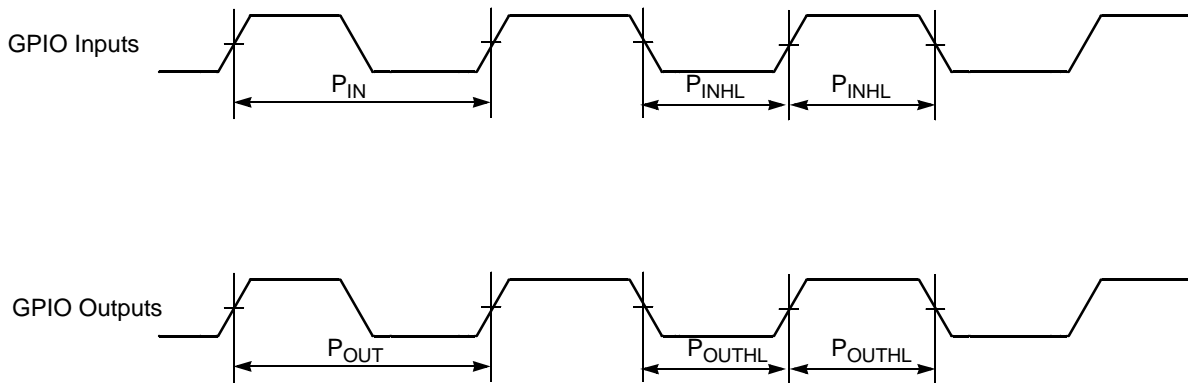
## 4.13 GPIO Timing

**Table 19. GPIO Timing<sup>1, 2</sup>**

Operating Conditions:  $V_{SS} = V_{SSIO} = V_{SSA} = 0\text{ V}$ ,  $V_{DD} = 1.62\text{--}1.98\text{ V}$ ,  $V_{DDIO} = V_{DDA} = 3.0\text{--}3.6\text{ V}$ ,  $T_A = -40^\circ\text{ to }+120^\circ\text{ C}$ ,  $C_L \leq 50\text{ pF}$ ,  $f_{op} = 120\text{ MHz}$

Characteristic	Symbol	Min	Max	Unit
GPIO input period	$P_{IN}$	$2T + 3$	—	ns
GPIO input high/low period	$P_{INHL}$	$1T + 3$	—	ns
GPIO output period	$P_{OUT}$	$2T - 3$	—	ns
GPIO output high/low period	$P_{OUTHL}$	$1T - 3$	—	ns

1. In the formulas listed,  $T$  = clock cycle. For  $f_{op} = 120\text{ MHz}$  operation and  $f_{ipb} = 60\text{ MHz}$ ,  $T = 8.33\text{ ns}$
2. Parameters listed are guaranteed by design.



**Figure 37. GPIO Timing**

## Part 5 Packaging

### 5.1 Package and Pin-Out Information DSP56853

This section contains package and pin-out information for the 144-pin LQFP configuration of the DSP56858.

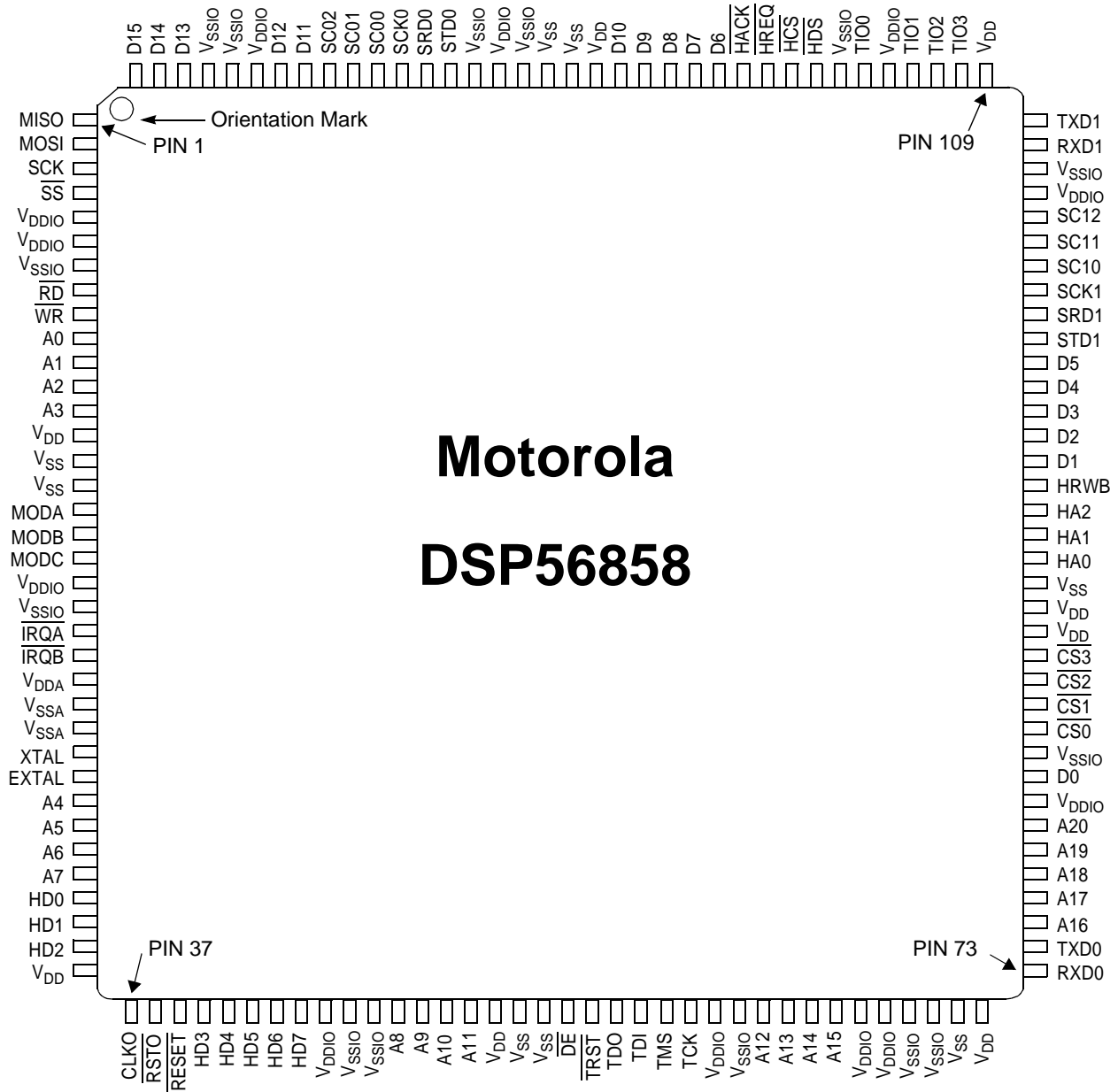


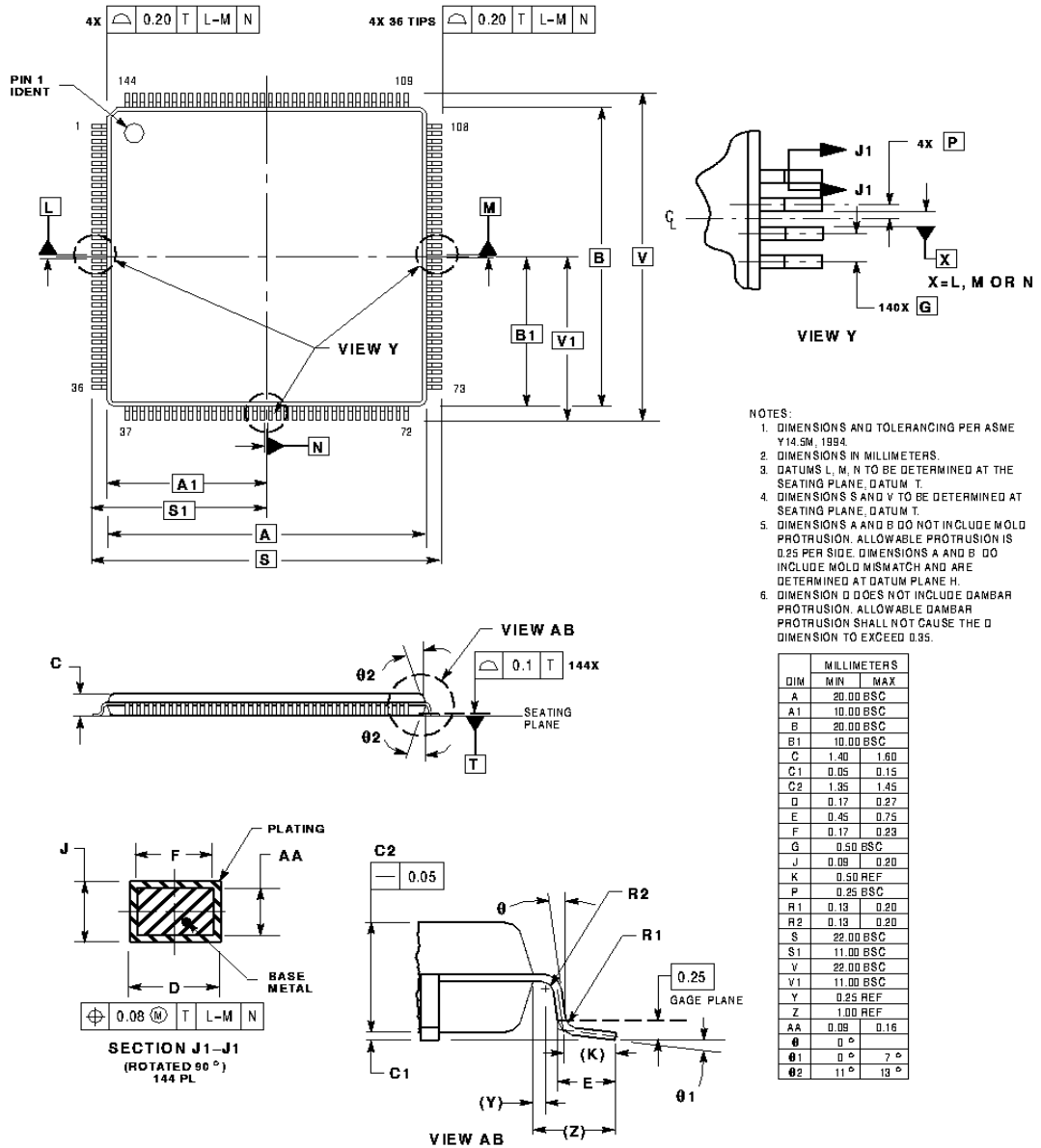
Figure 38. Top View, DSP56858 144-pin LQFP Package

**Table 20. DSP56858 Pin Identification by Pin Number**

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
1	MISO	37	CLKO	73	RXD0	109	V <sub>DD</sub>
2	MOSI	38	$\overline{\text{RSTO}}$	74	TXD0	110	TIO3
3	SCK	39	$\overline{\text{RESET}}$	75	A16	111	TIO2
4	$\overline{\text{SS}}$	40	HD3	76	A17	112	TIO1
5	V <sub>DDIO</sub>	41	HD4	77	A18	113	V <sub>DDIO</sub>
6	V <sub>DDIO</sub>	42	HD5	78	A19	114	TIO0
7	V <sub>SSIO</sub>	43	HD6	79	A20	115	V <sub>SSIO</sub>
8	$\overline{\text{RD}}$	44	HD7	80	V <sub>DDIO</sub>	116	$\overline{\text{HDS}}$
9	$\overline{\text{WR}}$	45	V <sub>DDIO</sub>	81	D0	117	$\overline{\text{HCS}}$
10	A0	46	V <sub>SSIO</sub>	82	V <sub>SSIO</sub>	118	$\overline{\text{HREQ}}$
11	A1	47	V <sub>SSIO</sub>	83	$\overline{\text{CS0}}$	119	$\overline{\text{HACK}}$
12	A2	48	A8	84	$\overline{\text{CS1}}$	120	D6
13	A3	49	A9	85	$\overline{\text{CS2}}$	121	D7
14	V <sub>DD</sub>	50	A10	86	$\overline{\text{CS3}}$	122	D8
15	V <sub>SS</sub>	51	A11	87	V <sub>DD</sub>	123	D9
16	V <sub>SS</sub>	52	V <sub>DD</sub>	88	V <sub>DD</sub>	124	D10
17	MODA	53	V <sub>SS</sub>	89	V <sub>SS</sub>	125	V <sub>DD</sub>
18	MODB	54	V <sub>SS</sub>	90	HA0	126	V <sub>SS</sub>
19	MODC	55	$\overline{\text{DE}}$	91	HA1	127	V <sub>SS</sub>
20	V <sub>DDIO</sub>	56	$\overline{\text{TRST}}$	92	HA2	128	V <sub>SSIO</sub>
21	V <sub>SSIO</sub>	57	TDO	93	HRWB	129	V <sub>DDIO</sub>
22	$\overline{\text{IRQA}}$	58	TDI	94	D1	130	V <sub>SSIO</sub>
23	$\overline{\text{IRQB}}$	59	TMS	95	D2	131	STD0
24	V <sub>DDA</sub>	60	TCK	96	D3	132	SRD0
25	V <sub>SSA</sub>	61	V <sub>DDIO</sub>	97	D4	133	SCK0

**Table 20. DSP56858 Pin Identification by Pin Number**

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
26	V <sub>SSA</sub>	62	V <sub>SSIO</sub>	98	D5	134	SC00
27	XTAL	63	A12	99	STD1	135	SC01
28	EXTAL	64	A13	100	SRD1	136	SC02
29	A4	65	A14	101	SCK1	137	D11
30	A5	66	A15	102	SC10	138	D12
31	A6	67	V <sub>DDIO</sub>	103	SC11	139	V <sub>DDIO</sub>
32	A7	68	V <sub>DDIO</sub>	104	SC12	140	V <sub>SSIO</sub>
33	HD0	69	V <sub>SSIO</sub>	105	V <sub>DDIO</sub>	141	V <sub>SSIO</sub>
34	HD1	70	V <sub>SSIO</sub>	106	V <sub>SSIO</sub>	142	D13
35	HD2	71	V <sub>SS</sub>	107	RXD1	143	D14
36	V <sub>DD</sub>	72	V <sub>DD</sub>	108	TXD1	144	D15



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ISSUE C

Figure 39. 144-pin LQFP Mechanical Information



This section contains package and pin-out information for the 144-pin MAPBGA configuration of the DSP56858.

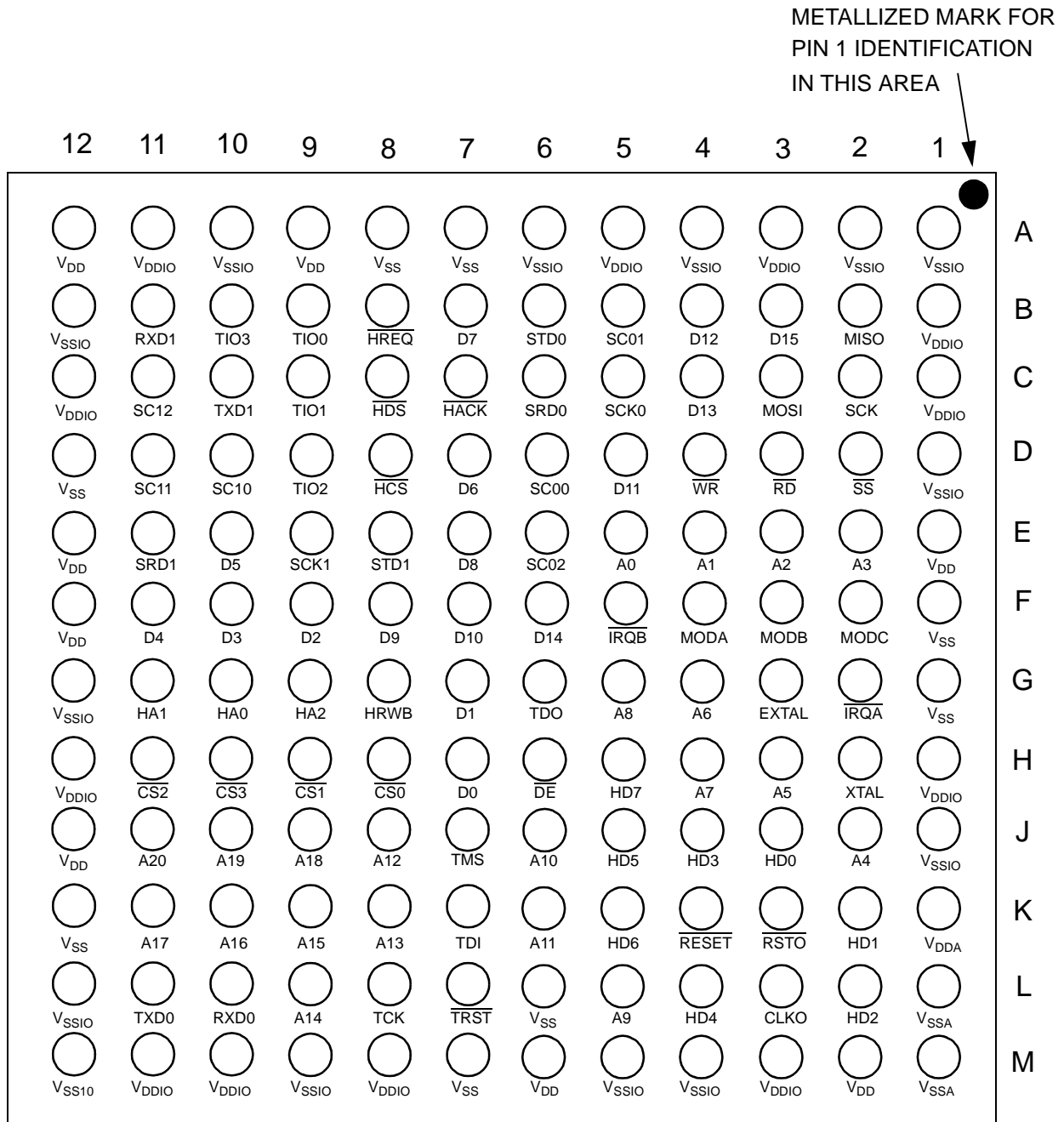


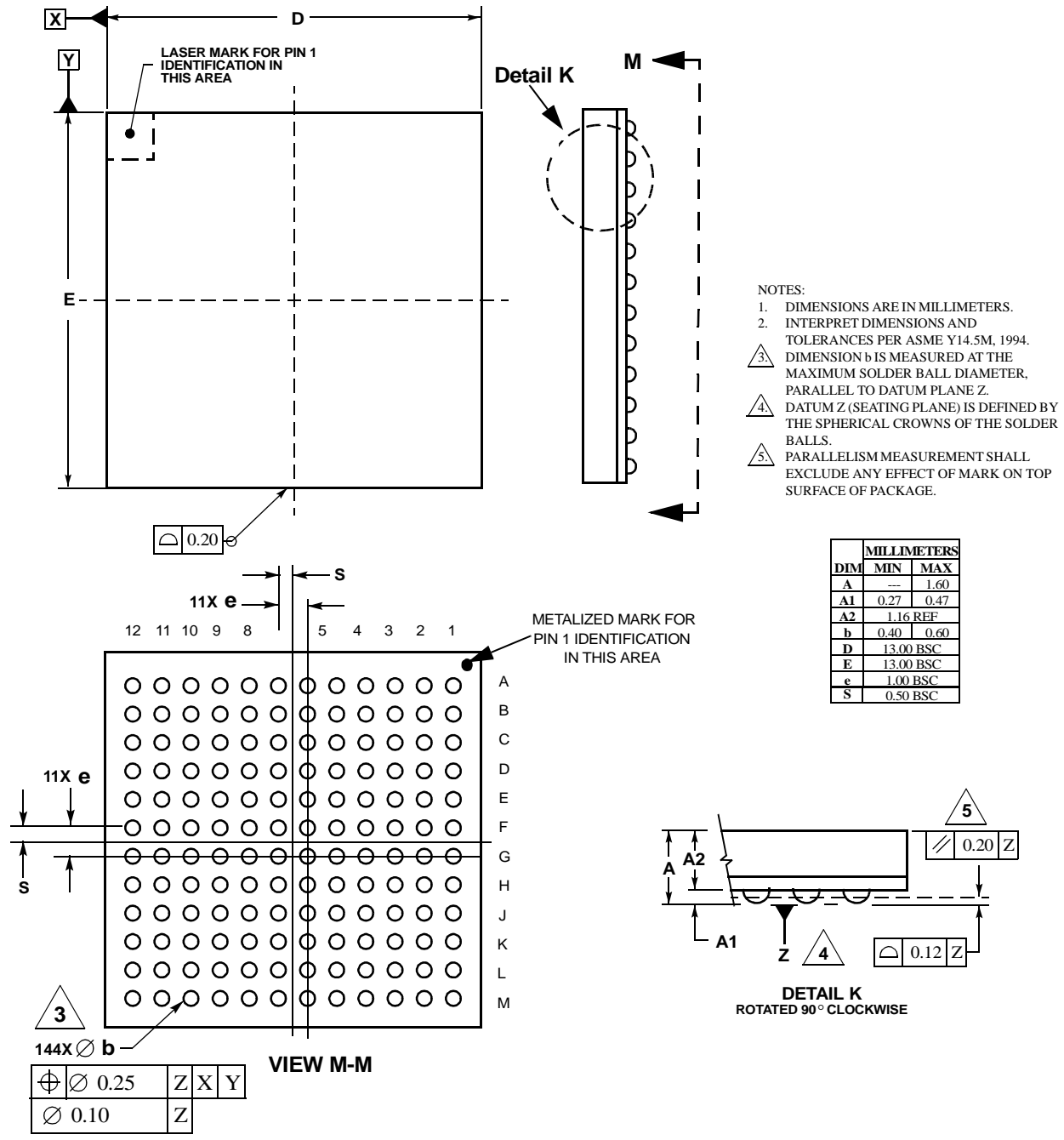
Figure 40. Bottom-View, DSP56858 144-pin MAPBGA Package

**Table 21. DSP56858 Pin Identification by Pin Number**

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
E5	A0	F7	D10	D8	$\overline{\text{HCS}}$	A5	V <sub>DDIO</sub>
E4	A1	D5	D11	J3	HD0	A3	V <sub>DDIO</sub>
E3	A2	B4	D12	K2	HD1	C1	V <sub>DDIO</sub>
E2	A3	C4	D13	L2	HD2	M10	V <sub>DDIO</sub>
J2	A4	F6	D14	J4	HD3	D3	$\overline{\text{RD}}$
H3	A5	B3	D15	L4	HD4	K4	$\overline{\text{RESET}}$
G4	A6	H6	$\overline{\text{DE}}$	J5	HD5	K3	$\overline{\text{RSTO}}$
H4	A7	G3	EXTAL	K5	HD6	L10	RXD0
G5	A8	M1	V <sub>SSA</sub>	H5	HD7	B11	RXD1
L5	A9	L1	V <sub>SSA</sub>	C8	$\overline{\text{HDS}}$	D6	SC00
J6	A10	G1	V <sub>SS</sub>	B8	$\overline{\text{HREQ}}$	B5	SC01
K6	A11	L6	V <sub>SS</sub>	G8	HRWB	E6	SC02
J8	A12	D12	V <sub>SS</sub>	G2	$\overline{\text{IRQA}}$	D10	SC10
K8	A13	A7	V <sub>SS</sub>	F5	$\overline{\text{IRQB}}$	D11	SC11
L9	A14	F1	V <sub>SS</sub>	B2	MISO	C11	SC12
K9	A15	M7	V <sub>SS</sub>	F4	MODA	C5	SCK0
K10	A16	K12	V <sub>SS</sub>	F3	MODB	E9	SCK1
K11	A17	A8	V <sub>SS</sub>	F2	MODC	C2	SCK
J9	A18	D1	V <sub>SSIO</sub>	C3	MOSI	C6	SRD0
J10	A19	J1	V <sub>SSIO</sub>	K1	V <sub>DDA</sub>	E11	SRD1
J11	A20	M5	V <sub>SSIO</sub>	E1	V <sub>DD</sub>	D2	$\overline{\text{SS}}$
L3	CLKO	M9	V <sub>SSIO</sub>	M6	V <sub>DD</sub>	B6	STD0
H8	$\overline{\text{CS0}}$	L12	V <sub>SSIO</sub>	F12	V <sub>DD</sub>	E8	STD1
H9	$\overline{\text{CS1}}$	G12	V <sub>SSIO</sub>	A9	V <sub>DD</sub>	L8	TCK
H11	$\overline{\text{CS2}}$	B12	V <sub>SSIO</sub>	M2	V <sub>DD</sub>	K7	TDI
H10	$\overline{\text{CS3}}$	A10	V <sub>SSIO</sub>	J12	V <sub>DD</sub>	G6	TDO

Table 21. DSP56858 Pin Identification by Pin Number

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
H7	D0	A4	V <sub>SSIO</sub>	E12	V <sub>DD</sub>	B9	TIO0
G7	D1	A1	V <sub>SSIO</sub>	A12	V <sub>DD</sub>	C9	TIO1
F9	D2	A2	V <sub>SSIO</sub>	B1	V <sub>DDIO</sub>	D9	TIO2
F10	D3	M4	V <sub>SSIO</sub>	H1	V <sub>DDIO</sub>	B10	TIO3
F11	D4	M12	V <sub>SSIO</sub>	M3	V <sub>DDIO</sub>	J7	TMS
E10	D5	A6	V <sub>SSIO</sub>	M8	V <sub>DDIO</sub>	L7	$\overline{\text{TRST}}$
D7	D6	G10	HA0	M11	V <sub>DDIO</sub>	L11	TXD0
B7	D7	G11	HA1	H12	V <sub>DDIO</sub>	C10	TXD1
E7	D8	G9	HA2	C12	V <sub>DDIO</sub>	D4	$\overline{\text{WR}}$
F8	D9	C7	$\overline{\text{HACK}}$	A11	V <sub>DDIO</sub>	H2	XTAL



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Figure 41. 144-pin MAPBGA Mechanical Information

## Part 6 Design Considerations

### 6.1 Thermal Design Considerations

An estimation of the chip junction temperature,  $T_J$ , in °C can be obtained from the equation:

$$\text{Equation 1: } T_J = T_A + (P_D \times R_{\theta JA})$$

Where:

$T_A$  = ambient temperature °C

$R_{\theta JA}$  = package junction-to-ambient thermal resistance °C/W

$P_D$  = power dissipation in package

Historically, thermal resistance has been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$\text{Equation 2: } R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

Where:

$R_{\theta JA}$  = package junction-to-ambient thermal resistance °C/W

$R_{\theta JC}$  = package junction-to-case thermal resistance °C/W

$R_{\theta CA}$  = package case-to-ambient thermal resistance °C/W

$R_{\theta JC}$  is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance,  $R_{\theta CA}$ . For example, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on the Printed Circuit Board (PCB), or otherwise change the thermal dissipation capability of the area surrounding the device on the PCB. This model is most useful for ceramic packages with heat sinks; some 90% of the heat flow is dissipated through the case to the heat sink and out to the ambient environment. For ceramic packages, in situations where the heat flow is split between a path to the case and an alternate path through the PCB, analysis of the device thermal performance may need the additional modeling capability of a system level thermal simulation tool.

The thermal performance of plastic packages is more dependent on the temperature of the PCB to which the package is mounted. Again, if the estimations obtained from  $R_{\theta JA}$  do not satisfactorily answer whether the thermal performance is adequate, a system level model may be appropriate.

A complicating factor is the existence of three common definitions for determining the junction-to-case thermal resistance in plastic packages:

- Measure the thermal resistance from the junction to the outside surface of the package (case) closest to the chip mounting area when that surface has a proper heat sink. This is done to minimize temperature variation across the surface.
- Measure the thermal resistance from the junction to where the leads are attached to the case. This definition is approximately equal to a junction to board thermal resistance.
- Use the value obtained by the equation  $(T_J - T_T)/P_D$  where  $T_T$  is the temperature of the package case determined by a thermocouple.

As noted above, the junction-to-case thermal resistances quoted in this data sheet are determined using the first definition. From a practical standpoint, that value is also suitable for determining the junction temperature from a case thermocouple reading in forced convection environments. In natural convection, using the junction-to-case thermal resistance to estimate junction temperature from a thermocouple reading

on the case of the package will estimate a junction temperature slightly hotter than actual. Hence, the new thermal metric, Thermal Characterization Parameter, or  $\Psi_{JT}$ , has been defined to be  $(T_J - T_T)/P_D$ . This value gives a better estimate of the junction temperature in natural convection when using the surface temperature of the package. Remember that surface temperature readings of packages are subject to significant errors caused by inadequate attachment of the sensor to the surface and to errors caused by heat loss to the sensor. The recommended technique is to attach a 40-gauge thermocouple wire and bead to the top center of the package with thermally conductive epoxy.

## 6.2 Electrical Design Considerations

### CAUTION

**This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.**

Use the following list of considerations to assure correct DSP operation:

- Provide a low-impedance path from the board power supply to each  $V_{DD}$  pin on the DSP, and from the board ground to each  $V_{SS}$  (GND) pin.
- The minimum bypass requirement is to place six 0.01–0.1  $\mu\text{F}$  capacitors positioned as close as possible to the package supply pins. The recommended bypass configuration is to place one bypass capacitor on each of the ten  $V_{DD}/V_{SS}$  pairs, including  $V_{DDA}/V_{SSA}$ .
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip  $V_{DD}$  and  $V_{SS}$  (GND) pins are less than 0.5 inch per capacitor lead.
- Use at least a four-layer Printed Circuit Board (PCB) with two inner layers for  $V_{DD}$  and GND.
- Bypass the  $V_{DD}$  and GND layers of the PCB with approximately 100  $\mu\text{F}$ , preferably with a high-grade capacitor such as a tantalum capacitor.
- Because the DSP output signals have fast rise and fall times, PCB trace lengths should be minimal.
- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the  $V_{DD}$  and GND circuits.
- All inputs must be terminated (i.e., not allowed to float) using CMOS levels.
- Take special care to minimize noise levels on the  $V_{DDA}$  and  $V_{SSA}$  pins.
- When using Wired-OR mode on the SPI or the  $\overline{\text{IRQx}}$  pins, the user must provide an external pull-up device.

- Designs that utilize the  $\overline{\text{TRST}}$  pin for JTAG port or Enhance OnCE module functionality (such as development or debugging systems) should allow a means to assert  $\overline{\text{TRST}}$  whenever  $\overline{\text{RESET}}$  is asserted, as well as a means to assert  $\overline{\text{TRST}}$  independently of  $\overline{\text{RESET}}$ . Designs that do not require debugging functionality, such as consumer products, should tie these pins together.
- The internal POR (Power on Reset) will reset the part at power on with  $\overline{\text{reset}}$  asserted or pulled high but requires that  $\overline{\text{TRST}}$  be asserted at power on.

## Part 7 Ordering Information

**Table 22** lists the pertinent information needed to place an order. Consult a Motorola Semiconductor sales office or authorized distributor to determine availability and to order parts.

**Table 22. DSP56858 Ordering Information**

Part	Supply Voltage	Package Type	Pin Count	Frequency (MHz)	Order Number
DSP56858	1.8V, 3.3V	Low-Profile Quad Flat Pack (LQFP)	144	120	DSP56858FV120
DSP56858	1.8V, 3.3V	MAP Ball Grid Array (MAPBGA)	144	120	DSP56858VF120

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