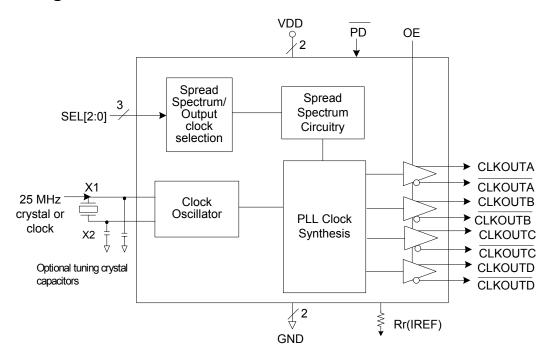## Description

The ICS557-05A is a spread-spectrum clock generator supporting PCI-Express requirements. The device is used in a PC or embedded systems to substantially reduce electro-magnetic interference (EMI). The device provides four differential (HCSL) spread spectrum, high-frequency outputs with spread spectrum capabilties. The device is pin configured for selecting spread spectrum and will take a 25 MHz crystal or clock input.

A 20-pin TSSOP package is employed to maximize board space utilization.
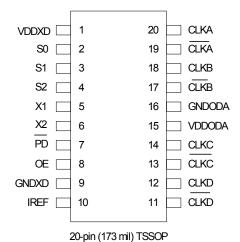
Features

- Packaged in 20-pin TSSOP
- Available in Pb (lead) free package
- Supports PCI-Express
- Four differential (HCSL) spread spectrum clock Outputs
- Spread spectrum for EMI reduction
- Uses external 25 MHz clock or crystal input
- Low output jitter design
- Output enable mode
- Power down pin turns off chip
- OE control tri-state outputs
- Spread selection via hardware pins
- Spread Bypass option available

Block Diagram

Integrated Circuit Systems, Inc. ● 525 Race Street, San Jose, CA 95126 ● tel (408) 297-1201 ● www.icst.com

Pin Assignment

```
           ┌──────────────┐
VDDXD ──┤ 1          20 ├── CLKA
   S0 ──┤ 2          19 ├── CLKA̅
   S1 ──┤ 3          18 ├── CLKB
   S2 ──┤ 4          17 ├── CLKB̅
   X1 ──┤ 5          16 ├── GNDODA
   X2 ──┤ 6          15 ├── VDDODA
   PD̅ ──┤ 7          14 ├── CLKC
   OE ──┤ 8          13 ├── CLKC̅
GNDXD ──┤ 9          12 ├── CLKD
 IREF ──┤ 10         11 ├── CLKD̅
           └──────────────┘
```

20-pin (173 mil) TSSOP

Spread Spectrum Selection Table

S2	S1	S0	Spread %	Spread Type	Output Frequency (MHz)
0	0	0	-0.5	Down	100
0	0	1	-1.0	Down	100
0	1	0	-1.5	Down	100
0	1	1	No Spread	Not Applicable	100
1	0	0	-0.5	Down	200
1	0	1	-1.0	Down	200
1	1	0	-1.5	Down	200
1	1	1	No Spread	Not Applicable	200

Pin Descriptions

Pin	Pin Name	Pin Type	Pin Description
1	VDDXD	Power	Connect to +3.3 V. Supply for oscillator and digital circuits.
2	S0	Input	Spread spectrum select pin #0. See table above. Internal pull-up resistor.
3	S1	Input	Spread spectrum select pin #1. See table above Internal pull-up resistor.
4	S2	Input	Spread spectrum select pin #2. See table above. Internal pull-up resistor.
5	X1	Input	Crystal connection. Connect to a fundamental mode crystal or clock input.
6	X2	Output	Crystal connection. Connect to a fundamental mode crystal or leave open.
7	$\overline{PD}$	Input	Powers down all PLL's and tri-states outputs when low. Internal pull-up resistor.
8	OE	Input	Provides output on, tri-states output (High = enable outputs; Low = disable outputs). Internal pull-up resistor.
9	GND	Power	Connect to ground. Supply for oscillator and digital circuits.
10	IREF	Output	Precision resistor attached to this pin is connected to the internal current reference.
11	$\overline{CLKD}$	Output	Selectable 100/200 MHz spread spectrum differential Compliment clock.
12	CLKD	Output	Selectable 100/200 MHz spread spectrum differential True clock.
13	$\overline{CLKC}$	Output	Selectable 100/200 MHz spread spectrum differential Compliment clock.
14	CLKC	Output	Selectable 100/200 MHz spread spectrum differential True clock.
15	VDDODA	Power	Connect to +3.3 V. Supply for output driver and analog circuits.
16	GND	Power	Connect to ground. Supply for output driver and analog circuits.
17	$\overline{CLKB}$	Output	Selectable 100/200 MHz spread spectrum differential Compliment clock.
18	CLKB	Output	Selectable 100/200 MHz spread spectrum differential True clock.
19	$\overline{CLKA}$	Output	Selectable 100/200 MHz spread spectrum differential Compliment clock.
20	CLKA	Output	Selectable 100/200 MHz spread spectrum differential True clock.

Application Information

Decoupling Capacitors

As with any high-performance mixed-signal IC, the ICS557-05A must be isolated from system power supply noise to perform optimally.

Decoupling capacitors of 0.01µF must be connected between each VDD and the PCB ground plane.

PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

Each 0.01µF decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between decoupling capacitor and VDD pin. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via. Distance of the ferrite bead and bulk decoupling from the device is less critical.

2) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers (the ferrite bead and bulk decoupling capacitor can be mounted on the back). Other signal traces should be routed away from the ICS557-05A.

This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

External Components

A minimum number of external components are required for proper operation. Decoupling capacitors of 0.01 µF should be connected between VDD and GND pairs (1,9 and 15,16) as close to the device as possible.

On chip capacitors- Crystal capacitors should be connected from pins X1 to ground and X2 to ground to optimize the initial accuracy. The value (in pf) of these crystal caps equal $(C_L-12)*2$ in this equation, C_L=crystal load capacitance in pf. For example, for a crystal with a 16 pF load cap, each external crystal cap would be 8 pF. [(16-12)x2]=8.

Current Reference Source R_r (Iref)

If board target trace impedance (Z) is 50Ω, then Rr = 475Ω (1%), providing IREF of 2.32 mA, output current (I_{OH}) is equal to 6*IREF.

Load Resistors R_L

Since the clock outputs are open source outputs, 50 ohm external resistors to ground are to be connected at each clock output.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS557-05A. These ratings are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD, VDDA	5.5 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature	0 to +70°C
Storage Temperature	-65 to +150°C
Junction Temperature	125°C
Soldering Temperature	260°C
ESD Protection (Input)	2000 V min. (HBM)

DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temperature 0 to +70°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Supply Voltage	V		3.135		3.465	
Input High Voltage[1]	V_{IH}		2.0		VDD +0.3	V
Input Low Voltage[1]	V_{IL}		VSS-0.3		0.8	V
Input Leakage Current[2]	I_{IL}	0 < Vin < VDD	-5		5	μA
Operating Supply Current	I_{DD}	50Ω, 2pF load@ 100MHz		105		mA
	I_{DDOE}	OE =Low		40		mA
	I_{DDPD}	No load, $\overline{PD}$ =Low		500		μA
Input Capacitance	C_{IN}	Input pin capacitance			7	pF
Output Capacitance	C_{OUT}	Output pin capacitance			6	pF
Pin Inductance	L_{PIN}				5	nH
Output Resistance	Rout	CLKOUT	3.0			kΩ

[1] Single edge is monotonic when transitioning through region.
[2] Inputs with pull-ups/-downs are not included.

AC Electrical Characteristics - CLKOUTA/CLKOUTB

Unless stated otherwise, **VDD=3.3 V ±5%**, Ambient Temperature 0 to +70°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency				25		MHz
Output Frequency			100		200	MHz
Output High Voltage[1,2]	V_{OH}		660	700	850	mV
Output Low Voltage[1,2]	V_{OL}		-150	0		mV
Crossing Point Voltage[1,2]		Absolute	250	350	550	mV
Crossing Point Voltage[1,2,4]		Variation over all edges			140	mV
Jitter, Cycle-to-Cycle[1,3]				60		ps
Modulation Frequency		Spread spectrum	30	31.5	33	kHz
Rise Time[1,2]	t_{OR}	From 0.175 V to 0.525 V	175	332	700	ps
Fall Time[1,2]	t_{OF}	From 0.525 V to 0.175 V	175	344	700	ps
Skew between outputs		At crossing point Voltage			50	ps
Duty Cycle[1,3]			45		55	%
Output Enable Time[5]		All outputs			10	us
Output Disable Time[5]		All outputs			10	us
Power-up Time	t_{STABLE}	From power-up VDD=3.3 V		3.0		ms
Spread Change Time	t_{SPREAD}	Settling period after spread change		3.0		ms

[1] Test setup is R_L=50 ohms with 2 pF, Rr = 475Ω (1%).
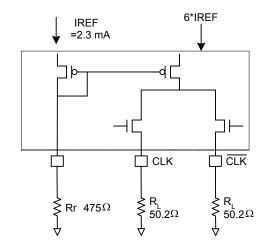
[2] Measurement taken from a single-ended waveform.

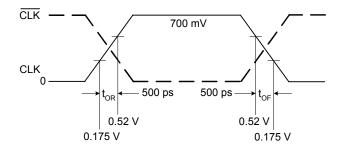[3] Measurement taken from a differential waveform.

[4] Measured at the crossing point where instantaneous voltages of both CLKOUT and $\overline{CLKOUT}$ are equal.

[5] CLKOUT pins are tri-stated when OE is low. asserted. CLKOUT is driven differential when OE is high unless its $\overline{PD}$= low.

Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		93		°C/W
	θ_{JA}	1 m/s air flow		78		°C/W
	θ_{JA}	3 m/s air flow		65		°C/W
Thermal Resistance Junction to Case	θ_{JC}			20		°C/W

HCSL Output Loads

IREF
=2.3 mA

6*IREF

CLK

$\overline{CLK}$

Rr 475Ω

R_L
50.2Ω

R_L
50.2Ω

$\overline{CLK}$

700 mV

CLK
0

t_{OR}

500 ps
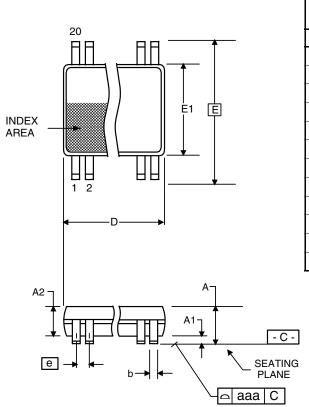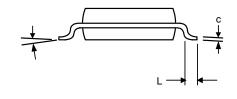
500 ps

t_{OF}

0.52 V

0.52 V

0.175 V

0.175 V

Package Outline and Package Dimensions (20-pin TSSOP, 173 mil Body)

Package dimensions are kept current with JEDEC Publication No. 95, MO-153

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A		1.20		0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.032	0.041
b	0.19	0.30	0.007	0.012
c	0.09	0.20	0.0035	0.008
D	6.40	6.60	0.252	0.260
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	0.169	0.177
e	0.65 Basic		0.0256 Basic	
L	0.45	0.75	0.018	0.030
α	0°	8°	0°	8°
aaa	--	0.10	--	0.004

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
ICS557G-05A	ICS557G-05A	Tubes	20-pin TSSOP	0 to +70°C
ICS557G-05ATR	ICS557G-05A	Tape and Reel	20-pin TSSOP	0 to +70°C
ICS557G-05ALF	557G-05ALF	Tubes	20-pin TSSOP	0 to +70°C
ICS557G-05ALFTR	557G-05ALF	Tape and Reel	20-pin TSSOP	0 to +70°C

Note: "LF" denotes Pb (lead) free package.

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