ICS557-07

2:1 MULTIPLEXER CHIP FOR PCI-E

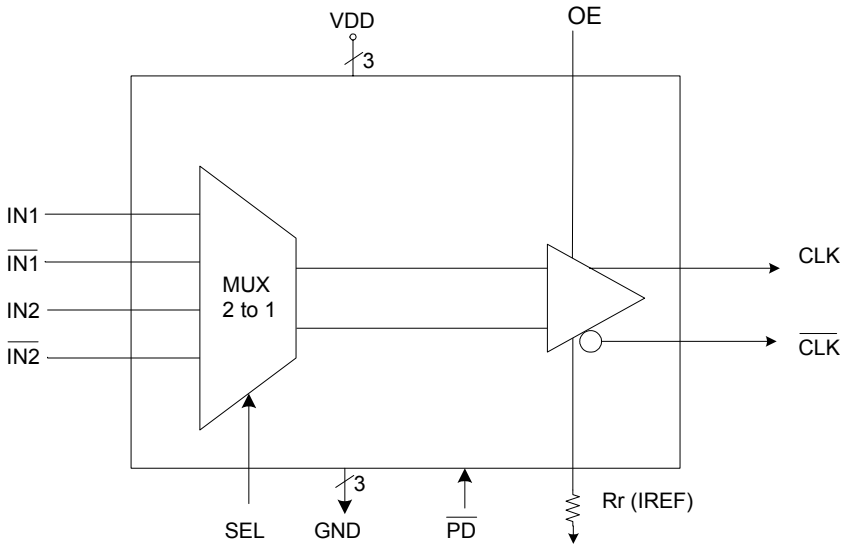
Description

The ICS557-07 is a 2:1 HCSL multiplexer chip that allows the user to select one of the two input pairs of HCSL (Host Clock Signal Level) or LVDS inputs and fans out to one pair of differential HCSL outputs. This chip is suited especially for PCI-Express applications, where there is a need to select the PCI-Express clock locally from the PCI-E card or from the motherboard.

Features

- Packaged in 16-pin TSSOP
- Available in Pb (lead) free package
- Operating voltage of 3.3 V
- Low power consumption
- Input differential clock of up to 200 MHz (can accept LVDS, HCSL)
- Output, one pair (HCSL, 0.7 V Current mode differential pair)
- Jitter 60 ps (peak-to-peak)
- Operating frequency of 80 MHz to 200 MHz

Block Diagram



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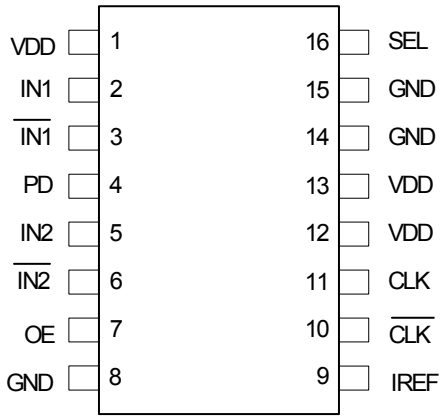
Pin Assignment



16-pin (173 mil) TSSOP

Select Table

SEL	Input Pair selected
0	IN2/ $\overline{IN2}$
1	IN1/ $\overline{IN1}$

Pin Descriptions

Pin	Pin Name	Pin Type	Pin Description
1	VDD	Power	Connect to +3.3 V. Supply voltage for Input clocks.
2	IN1	Input	HCSL/LVDS true input signal 1.
3	$\overline{IN1}$	Input	HCSL/LVDS complimentary input signal 1.
4	$\overline{PD}$	Input	Powers down the chip and tri-states outputs when low. Internal pull-up resistor.
5	IN2	Input	HCSL/LVDS true input signal 2.
6	$\overline{IN2}$	Input	HCSL/LVDS complimentary input signal 2.
7	OE	Input	Provides fast output on, tri-states output (High = enable outputs; Low = disable). Internal pull-up resistor.
8	GND	Power	Connect to ground.
9	Rr(IREF)	Output	Precision resistor attached to this pin is connected to the internal current reference.
10	$\overline{CLK}$	Output	HCSL differential complimentary clock .
11	CLK	Output	HCSL True clock.
12	VDD	Power	Connect to +3.3 V. Supply Voltage for output clocks.
13	VDD	Power	Connect to +3.3 V. Supply Voltage for output clocks.
14	GND	Power	Connect to ground.
15	GND	Power	Connect to ground.
16	SEL	Input	SEL=1 selects IN1/$\overline{IN1}$. SEL =0 selects IN2/ $\overline{IN2}$. Internal pull-up resistor.

Applications Information

External Components

A minimum number of external components are required for proper operation.

Decoupling Capacitors

Decoupling capacitors of 0.01 µF should be connected between VDD and the ground plane (pin 4) as close to the VDD pin as possible. Do not share ground vias between components. Route power from power source through the capacitor pad and then into ICS pin.

Crystal

A 25 MHz fundamental mode parallel resonant crystal with C_L = 16 pF should be used. This crystal must have less than 300 ppm of error across temperature in order for the ICS557-07 to meet PCI Express specifications.

Crystal Capacitors

Crystal capacitors are connected from pins X1 to ground and X2 to ground to optimize the accuracy of the output frequency.

C_L= Crystal's load capacitance in pF

Crystal Capacitors (pF) = (C_L- 8) * 2

For example, for a crystal with a 16 pF load cap, each external crystal cap would be 16 pF. (16-8)*2=16.

Current Source (Iref) Reference Resistor - R_R

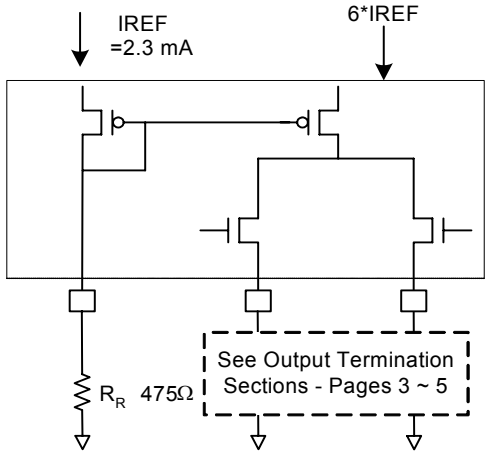
If board target trace impedance (Z) is 50Ω, then R_R = 475Ω (1%), providing IREF of 2.32 mA. The output current (I_{OH}) is equal to 6*IREF.

Output Termination

The PCI-Express differential clock outputs of the ICS557-07 are open source drivers and require an external series resistor and a resistor to ground. These resistor values and their allowable locations are shown in detail in the **PCI-Express Layout Guidelines** section.

The ICS557-07can also be configured for LVDS compatible voltage levels. See the **LVDS Compatible Layout Guidelines** section

Output Structures



General PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1. Each 0.01µF decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible.

2. No vias should be used between decoupling capacitor and VDD pin.

3. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via. Distance of the ferrite bead and bulk decoupling from the device is less critical.

4. An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers (any ferrite beads and bulk decoupling capacitors can be mounted on the back). Other signal traces should be routed away from the ICS557-07.This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS557-07. These ratings are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	5.5 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature	0 to +70°C
Storage Temperature	-65 to +150°C
Junction Temperature	125°C
Soldering Temperature	260°C
ESD Protection (Input)	2000 V min. (HBM)

DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temperature 0 to +70°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Supply Voltage	V		3.135		3.465	
Input High Voltage[1]	V_{IH}	OE, SEL, $\overline{PD}$	2.0		VDD +0.3	V
Input Low Voltage[1]	V_{IL}	OE, SEL, $\overline{PD}$	VDD-0.3		0.8	V
Input Leakage Current[2]	I_{IL}	0 < Vin < VDD	-5		5	µA
Operating Supply Current	I_{DD}	50Ω, 2 pF			40	mA
	I_{DDOE}	OE =Low			20	mA
	I_{DDPD}	No load, $\overline{PD}$ =Low			400	µA
Input Capacitance	C_{IN}	Input pin capacitance			7	pF
Output Capacitance	C_{OUT}	Output pin capacitance			6	pF
Pin Inductance	L_{PIN}				5	nH
Output Resistance	R_{OUT}	CLK, each output	3.0			kΩ
Pull-up Resistor	R_{PU}		110			kΩ

[1] Single edge is monotonic when transitioning through region.
[2] Inputs with pull-ups/-downs are not included.

AC Electrical Characteristics - CLKOUTA/CLKOUTB

Unless stated otherwise, **VDD=3.3 V ±5%**, Ambient Temperature 0 to +70°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency			80		200	MHz
Output Frequency			80		200	MHz
Input High Voltage[1,2]	V_{IH}	HCSL	660	700	850	mV
Input Low Voltage[1,2]	V_{IL}	HCSL	-150	0		mV
Differential Input Voltages	(V_{ID})	LVDS	250	350	450	mV
Input Offset Voltage	(V_{IS})	LVDS	1.125	1.25	1.375	V
Output High Voltage[1,2]	V_{OH}	HCSL	660	700	850	mV
Output Low Voltage[1,2]	V_{OL}	HCSL	-150	0		mV
Crossing Point Voltage[1,2]		Absolute	250	350	550	mV
Crossing Point Voltage[1,2,4]		Variation over all edges			140	mV
Jitter, Cycle-to-Cycle[1,3]				60		ps
Rise Time[1,2]	t_{OR}	From 0.175 V to 0.525 V	175	332	700	ps
Fall Time[1,2]	t_{OF}	From 0.525 V to 0.175 V	175	344	700	ps
Rise/Fall Time Variation[1,2]					125	ps
Duty Cycle[1,3]			45		55	%
Output Enable Time[5]		All outputs		10		µs
Output Disable Time[5]		All outputs		10		µs
Stabilization Time	t_{STABLE}	From power-up VDD=3.3 V		3.0		ms
Input to Output Delay		Measured at crossing points		4		ns

[1] Test setup is R_L=50 ohms with 2 pF, Rr = 475Ω (1%).

[2] Measurement taken from a single-ended waveform.

[3] Measurement taken from a differential waveform.

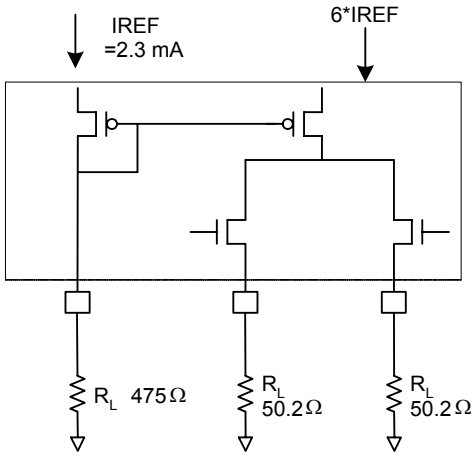
[4] Measured at the crossing point where instantaneous voltages of both CLKOUT and $\overline{CLKOUT}$ are equal.

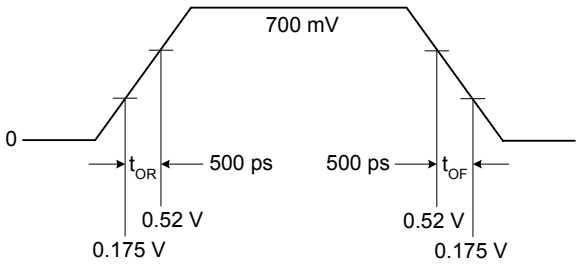
[5] CLK and $\overline{CLK}$ pins are tri-stated when OE is Low. CLK and $\overline{CLK}$ are driven differential when OE is High unless its $\overline{PD}$ = low.

Thermal Characteristics

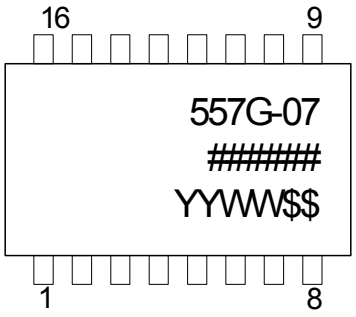
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		93		°C/W
	θ_{JA}	1 m/s air flow		78		°C/W
	θ_{JA}	3 m/s air flow		65		°C/W
Thermal Resistance Junction to Case	θ_{JC}			20		°C/W

HCSL Output Loads

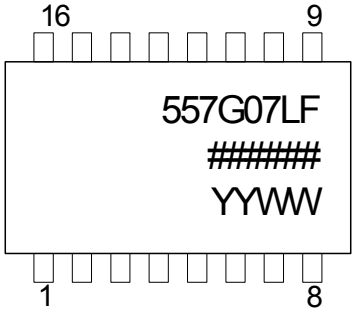




Marking Diagram



Marking Diagram (Pb free)

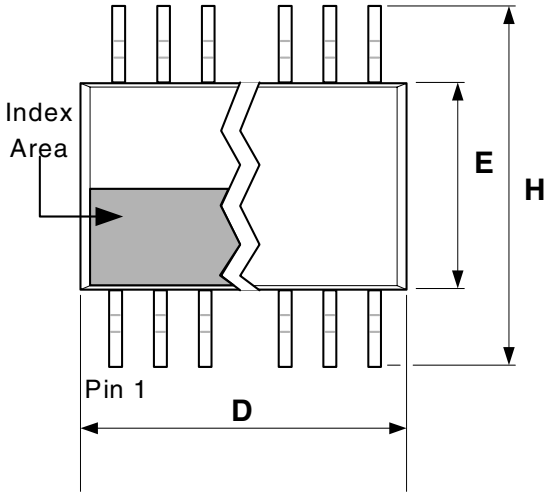


Notes:

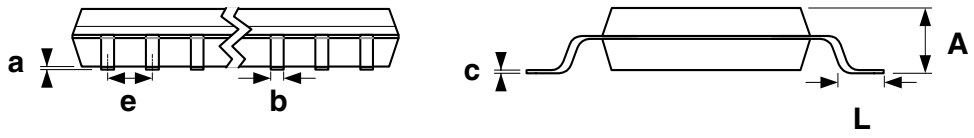
1. ###### is the lot code.
2. YYWW is the last two digits of the year, and the week number that the part was assembled.
3. “LF” denotes Pb free package.
4. Bottom marking: (origin). Origin = country of origin if not USA.

Package Outline and Package Dimensions (16-pin TSSOP, 173 Mil. Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	Min	Max	Min	Max
A	--	1.20	--	0.047
a	0.05	0.15	0.002	0.006
b	0.19	0.30	0.007	0.012
c	0.09	0.20	0.0035	0.008
D	4.90	5.10	0.193	0.201
E	4.30	4.50	0.169	0.177
e	0.65 Basic		0.0256 Basic	
H	6.40 Basic		0.252 Basic	
L	0.45	0.75	0.018	0.030



Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
ICS557G-07	See Page 4	Tubes	16-pin TSSOP	0 to +70° C
ICS557G-07T		Tape and Reel	16-pin TSSOP	0 to +70° C
ICS557G-07LF		Tubes	16-pin TSSOP	0 to +70° C
ICS557G-07LFT		Tape and Reel	16-pin TSSOP	0 to +70° C

Parts that are ordered with a "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.