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Part 1 Product Overview

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The contents described in Part 1 take first priority over Part 2 and Part 3.

Part 1 Overview

1.Description

The LRS1310A is a combination memory organized as 2,097,152×8 bit flash memory and 262,144×8 bit static RAM in one package.
It is fabricated using silicon-gate CMOS process technology.

Features

○Access Time			
Flash memory access time		150 ns Max.	
SRAM access time		85 ns Max.	
○Operating current			
Flash memory	Read	12 mA Max.	(t_{CYCLE}=200ns)
	Word write	57 mA Max.	(F-Vcc$\geq$3.0V)
	Block erase	37 mA Max.	(F-Vcc$\geq$3.0V)
SRAM	Operating	25 mA Max.	(t_{CYCLE}=200ns)
○Standby current			
Flash memory		20 µA Max.	(F-$\overline{CE}\geq$F-V_{CC}-0.2V, F-$\overline{RP}\leq$0.2V, F-$V_{PP}\leq$0.2V)
SRAM		45 µA Max.	(S-$\overline{CE1}$,S-CE2$\geq$S-V_{CC}-0.2V or S-CE2$\leq$0.2V)

(Total standby current is the summation of Flash memory's standby current and SRAM's one.)

○Power supply	2.7V to 3.6V	(Read, SRAM write)
	3.0V to 3.6V	(Flash erase, write)

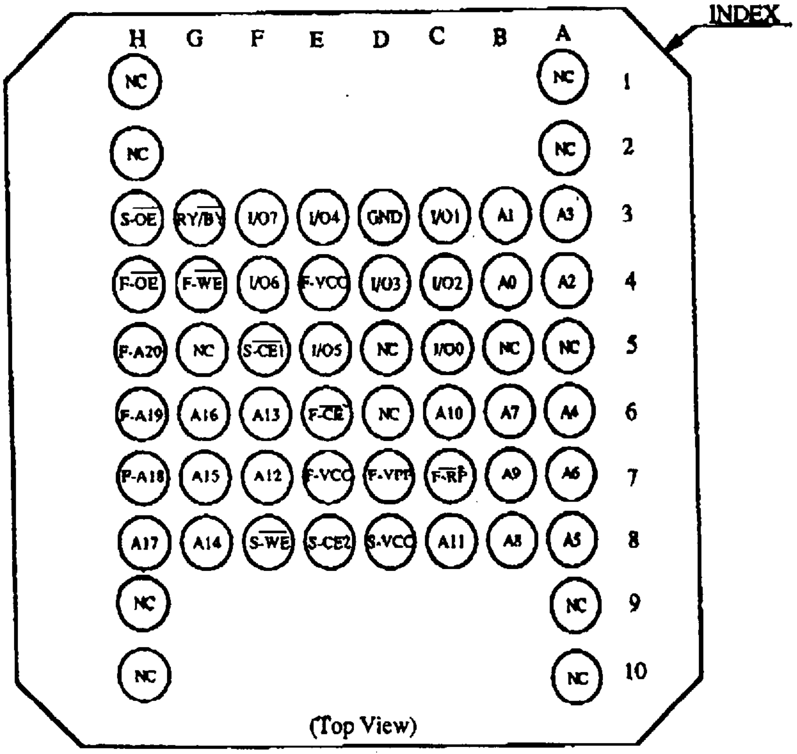
(Block erase and word write operations with V_{CC}<3.0V are not supported.)

○SRAM data retention voltage	2.0 V (Min.)
○Operating temperature	-25℃ to +85℃

○Fully static operation
○Three-state output
○Not designed or rated as radiation hardened
○56 pin CSP (LCSP056-P-0810) plastic package
○Flash memory has P-type bulk silicon, and SRAM has P-type bulk silicon.

The contents described in Part 1 take first priority over Part 2 and Part 3.

2.Pin Configuration



(Top View)

PIN	DESCRIPTION
A_0 to A_{17}	Common Address Input Pins
F-A_{18} to F-A_{20}	Address Input Pins for Flash Memory
F-$\overline{CE}$	Chip Enable Input Pin for Flash Memory
S-$\overline{CE1}$, S-CE2	Chip Enable Input Pin for SRAM
F-$\overline{WE}$	Write Enable Input Pin for Flash Memory
S-$\overline{WE}$	Write Enable Input Pin for SRAM
F-$\overline{OE}$	Output Enable Input Pin for Flash Memory
S-$\overline{OE}$	Output Enable Input Pin for SRAM
I/O_0 to I/O_7	Common Data Input/Output Pins
F-$\overline{RP}$	Reset/Deep Power Down Input Pin for Flash Memory
RY/$\overline{BY}$	Ready/Busy Output Pin for Flash Memory
F-V_{CC}	Power Supply Pin for Flash Memory
F-V_{PP}	Power Supply Pin for Flash Memory Write/Erase
S-V_{CC}	Power Supply Pin for SRAM
GND	Common GND
NC	Non Connect

The contents described in Part 1 take first priority over Part 2 and Part 3.

3. Notes

This product is a stacked CSP package that a 2,097,152×8 bit Flash Memory and a 262,144×8 bit SRAM are assembled into.

SUPPLY POWER

Maximum difference (between F-V_{CC} and S-V_{CC}) of the voltage is less than -0.3V.

POWER SUPPLY AND CHIP ENABLE OF FLASH MEMORY AND SRAM

S-$\overline{CE1}$ should not be "LOW" and S-CE2 should not be "HIGH" when F-$\overline{CE}$ is "LOW" simultaneously. If the two memories are active together, possibly they may not operate normally by interference noises or data collision on I/O bus.

Both F-V_{CC} and S-V_{CC} are needed to be applied by the recommended supply voltage at the same time except SRAM data retention mode.

SRAM DATA RETENTION

SRAM data retention is capable in three ways as below. SRAM power switching between a system battery and a backup battery needs careful device decoupling from Flash Memory to prevent SRAM supply voltage from falling lower than 2.0V by a Flash Memory peak current caused by transition of Flash Memory supply voltage or of control signals (F-$\overline{CE}$, F-$\overline{OE}$ and $\overline{RP}$).

CASE 1: FLASH MEMORY IS IN STANDBY MODE. (F-V_{CC}=2.7V to 3.6V)

- SRAM inputs and input/outputs except S-$\overline{CE1}$, S-CE2 are needed to be applied with voltages in the range of -0.3V to S-V_{CC}+0.3V or to be open(High-Z).
- Flash Memory inputs and input/outputs except F-$\overline{CE}$ and $\overline{RP}$ are needed to be applied with voltages in the range of -0.3V to S-V_{CC}+0.3V or to be open(High-Z).

CASE 2: FLASH MEMORY IS IN DEEP POWER DOWN MODE. (F-V_{CC}=2.7V to 3.6V)

- SRAM inputs and input/outputs except S-$\overline{CE1}$, S-CE2 are needed to be applied with voltages in the range of -0.3V to S-V_{CC}+0.3V or to be open.
- Flash Memory inputs and input/outputs except $\overline{RP}$ are needed to be applied with voltages in the range of -0.3V to S-V_{CC}+0.3V or to be open(High-Z). $\overline{RP}$ is needed to be at the same level as F-V_{CC} or to be open.

CASE 3: FLASH MEMORY POWER SUPPLY IS TURNED OFF. (F-V_{CC}=0V)

- Fix $\overline{RP}$ LOW level before turning off Flash memory power supply.
- SRAM inputs and input/outputs except S-$\overline{CE1}$, S-CE2 are needed to be applied with voltages in the range of -0.3V to S-V_{CC}+0.3V or to be open(High-Z).
- Flash Memory inputs and input/outputs except $\overline{RP}$ are needed to be at GND or to be open(High-Z).

POWER UP SEQUENCE

When turning on Flash memory power supply, keep $\overline{RP}$ LOW. After F-V_{CC} reaches over 2.7V, keep $\overline{RP}$ LOW for more than 100nsec.

DEVICE DECOUPLING

The power supply is needed to be designed carefully because one of the SRAM and the Flash Memory is in standby mode when the other is active. A careful decoupling of power supplies is necessary between SRAM and Flash Memory. Note peak current caused by transition of control signals(F-$\overline{CE}$, S-$\overline{CE1}$, S-CE2).

The contents described in Part 1 take first priority over Part 2 and Part 3.

4.Truth table(*1,3)

F-$\overline{\text{CE}}$	F-$\overline{\text{OE}}$	F-$\overline{\text{WE}}$	F-$\overline{\text{RP}}$	S-$\overline{\text{CE1}}$	S-CE2	S-$\overline{\text{OE}}$	S-$\overline{\text{WE}}$	address	Mode	I/O_0 to I/O_7	F-I/O_8 to F-I/O_{15}	Current	Note
L	L	H	H	H	L	X	X	X	Flash read	Output	Output	I_{CC}	*2,4,8,9
L	H	H	H	H	L	X	X	X	Flash read	High-Z	High-Z	I_{CC}	*4
L	H	L	H	H	L	X	X	X	Flash read	Input	Input	I_{CC}	*4,6,7,8,9
H	X	X	X	L	H	L	H	X	SRAM read	Output	High-Z	I_{CC}	
H	X	X	X	L	H	H	H	X	SRAM read	High-Z	High-Z	I_{CC}	
H	X	X	X	L	H	X	L	X	SRAM read	Input	High-Z	I_{CC}	
H	X	X	H	H	L	X	X	X	Standby	High-Z	High-Z	I_{CC}	*4,9
X	X	X	L	H	L	X	X	X	Deep power down	High-Z	High-Z	I_{CC}	*5,9

Notes:

*1. S-$\overline{\text{CE1}}$ should not be "LOW" and S-CE2 should not be "HIGH" when F-$\overline{\text{CE}}$ is "LOW" simultaneously.

*2. Refer to DC Characteristics. When F-$V_{PP} \leqq V_{PPLK}$, memory contents can be read, but not altered.

*3. X can be V_{IL} or V_{IH} for control pins and addresses, and V_{PPLK} or V_{PPH} for F-V_{PP}. See DC Characteristics for V_{PPLK} and V_{PPH} voltages.

*4. RY/$\overline{\text{BY}}$ is V_{OL} when the WSM is executing internal block erase, byte write, or lock-bit configuration algorithms. It is V_{OH} during when the WSM is not busy, in block erase suspend mode (with byte write inactive), byte write suspend mode, or deep power-down mode.

*5. F-RP at GND ± 0.2V ensures the lowest deep power-down current.

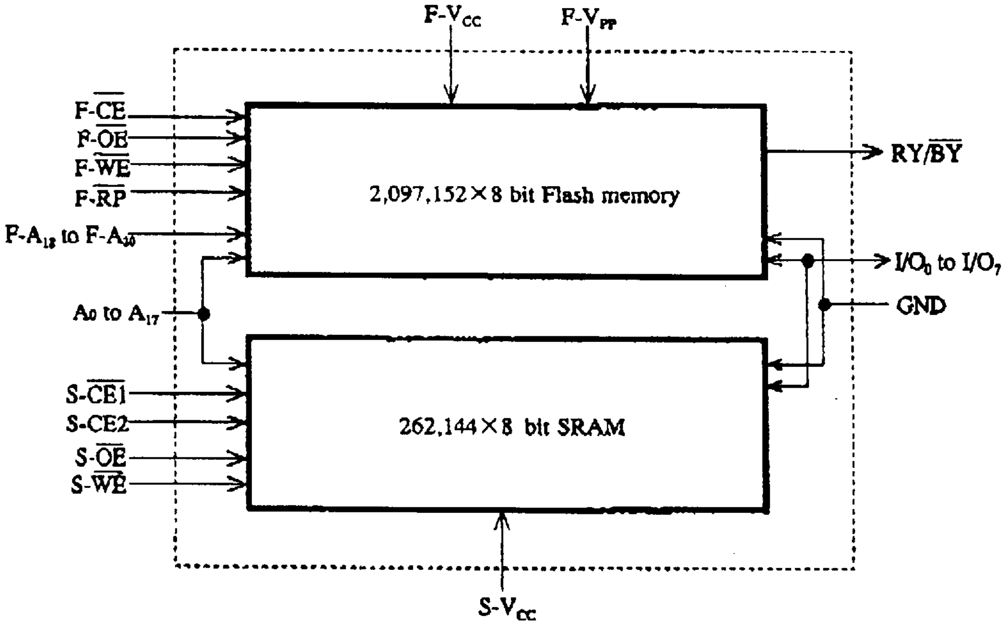
*6. Command writes involving block erase, write, or lock-bit configuration are reliably executed when F-V_{PP}=V_{PPH} and F-V_{CC}=V_{CC2}. Block erase, byte write, or lock-bit configuration with F-$V_{CC}<3.0V$ or $V_{IH}<$F-RP$<V_{HH}$ produce spurious results and should not be attempted.

*7. Refer to Part 2 Section 3 Table 4 for valid D_{IN} during a write operation.

*8. Do not use in a timing that both F-$\overline{\text{OE}}$ and F-$\overline{\text{WE}}$ is "LOW" level.

*9. With S-$\overline{\text{CE1}}$ at a "Low" level or S-CE2 at a "High" level, SRAM becomes standby mode. S-CE2 should be "HIGH" or "LOW" when S-$\overline{\text{CE1}}$ is "HIGH".

5. Block Diagram



The contents described in Part 1 take first priority over Part 2 and Part 3.

6.Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage(*10,11)	V_{CC}	-0.2 to 4.6	V
Input voltage(*10,12)	V_{IN}	-0.3 (*13) to V_{CC}+0.3	V
Operating temperature	T_{opr}	-25 to +85	℃
Storage temperature	T_{stg}	-65 to +125	℃
V_{PP} voltage(*10)	V_{PP}	-0.2 to +12.6 (*14)	V
Input voltage(*10)	$\overline{RP}$	-0.5 (*13) to +12.6 (*14)	V

Notes) * 10.The maximum applicable voltage on any pin with respect to GND.

* 11. Except V_{PP}.
* 12. Except $\overline{RP}$.
* 13. -2.0V undershoot is allowed when the pulse width is less than 20nsec.
* 14. +14.0V overshoot is allowed when the pulse width is less than 20nsec.

7.Recommended DC Operating Conditions

(T_a= -25℃ to +85℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	2.7	3.0	3.6	V
Input voltage	V_{IH}	2.0		V_{CC}+0.3(*17)	V
	V_{IL}	-0.3 (*15)		0.8	V
	V_{HH}(*16)	11.4		12.6	

Notes) * 15. -2.0V undershoot is allowed when the pulse width is less than 20nsec.

* 16. This voltage is applicable to F-$\overline{RP}$ Pin only.
* 17. V_{CC} is the lower one of S-V_{CC} and F-V_{CC}.

8.Pin Capacitance

(T_a=25℃, f=1MHz)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	
Input capacitance	C_{IN}	V_{IN}=0V			18	pF	*18
I/O capacitance	C_{IO}	V_{IO}=0V			22	pF	*18

Note) * 18. Sampled but not 100% tested

9.DC Electrical Characteristics

(T_a= -25℃ to +85℃ , V_{CC}= 2.7V to 3.6V)

Parameter		Note	Conditions		Min.	Typ.	Max.	Unit
Input leakage current(I_{LI})			V_{IN}=0V to V_{CC}		-1.5		1.5	μA
Output leakage current (I_{LO})			F-$\overline{CE}$,S-$\overline{CE1}$=V_{IH} or F-$\overline{CE}$=V_{IH} ,S-CE2=V_{IL} or F-$\overline{OE}$, S-$\overline{OE}$=V_{IH} or F-$\overline{WE}$, S-$\overline{WE}$=V_{IH}, $V_{I/O}$=0V to V_{CC}		-1.5		1.5	μA
Operating supply current (I_{CC})	FLASH	*20	Read current, F-V_{PP}≦F-V_{CC} F-$\overline{CE}$≦0.2V, VIN≧V_{CC}-0.2V or V_{IN}≦0.2V	t_{CYCLE}=200ns $I_{I/O}$=0mA			12	mA
		*21 *22	Summation of V_{CC} Byte Write or set lock-bit current, and V_{PP} Byte Write or set lock-bit current. F-V_{CC}≧3.0V				57	mA
		*21 *23	Summation of V_{CC} Block Erase or Clear Block lock-bits current, and V_{PP} Block Erase or Clear Block lock-bits current. F-V_{CC}≧3.0V				37	mA
	SRAM	*24	S-$\overline{CE1}$≦0.2V ,S-CE2≧V_{CC}-0.2V V_{IN}≧V_{CC}-0.2V or V_{IN}≦0.2V	t_{CYCLE}=200ns $I_{I/O}$=0mA			25	mA
Standby current (I_{SB})	FLASH	*25 *26	F-$\overline{CE}$=V_{IH}, $\overline{RP}$=V_{IH}				2.2	mA
		*25 *27	F-$\overline{CE}$≧V_{CC}-0.2V, F-V_{PP}≦0.2V, $\overline{RP}$≦0.2V				20	μA
	SRAM	*28	S-$\overline{CE1}$,S-CE2=V_{IH} or S-CE2=V_{IL}				3.0	mA
		*29	S-$\overline{CE1}$,S-CE2≧V_{CC}-0.2V or S-CE2≦0.2V			0.6 (*19)	43 40	μA
Output voltage (V_{OL}, V_{OH})		*30	I_{OL}=2.0mA				0.4	V
		*30	I_{OH}=-1.0mA		2.4			V

Note) ＊19. T_a=25℃, V_{CC}=3.0V Refference value at.
＊20. This value is read current (I_{CCR}+I_{PPR}) of the flash memory.
＊21. Sampled but not 100% tested.
＊22. This value is operation current (I_{CCW}+I_{PPW}) of flash memory.
＊23. This value is operation current (I_{CCE}+I_{PPE}) of flash memory.
＊24. This value is operation current (I_{CC2}) of SRAM.
＊25. RY/$\overline{BY}$ Pin must be opened.
＊26. This value is stand-by current (I_{CCS}+I_{PPS}) of flash memory.
＊27. This value is deep power down cuurent (I_{CCD}+I_{PPD}) of flash memory.
＊28. This value is stand-by current (I_{SB1}) of SRAM.
＊29. This value is stand-by current (I_{SB}) of SRAM.
＊30. Including RY/$\overline{BY}$ Pin.

CONTENTS

1 INTRODUCTION

This datasheet contains LRS1310A specifications. Section 1 provides a flash memory overview. Sections 2, 3, 4, and 5 describe the memory organization and functionality. Section 6 covers electrical specifications. LRS1310A Flash memory documentation also includes application notes and design tools which are referenced in Section 7.

1.1 New Features

The LRS1310A SmartVoltage Flash memory maintains backwards-compatibility with SHARP's 28F008SA. Key enhancements over the 28F008SA include:

- SmartVoltage Technology
- Enhanced Suspend Capabilities
- In-System Block Locking

Both devices share a compatible status register, and software command set. These similarities enable a clean upgrade from the 28F008SA to LRS1310A. When upgrading, it is important to note the following differences:

- Because of new feature support, the two devices have different device codes. This allows for software optimization.
- V_{PPLK} has been lowered to 1.5V to support 3.3V block erase, byte write, and lock-bit configuration operations. Designs that switch V_{PP} off during read operations should make sure that the V_{PP} voltage transitions to GND.
- To take advantage of SmartVoltage technology, allow V_{PP} connection to 3.3V.

1.2 Product Overview

The LRS1310A is a high-performance 16-Mbit SmartVoltage Flash memory organized as 2 Mbyte of 8 bits. The 2 Mbyte of data is arranged in thirty-two 64-Kbyte blocks which are individually erasable, lockable, and unlockable in-system. The memory map is shown in Figure 2.

SmartVoltage technology provides a choice of V_{CC} and V_{PP} combinations, as shown in Table 1, to meet system performance and power expectations. In addition to flexible erase and program voltages, the dedicated V_{PP} pin gives complete data protection when $V_{PP} \leq V_{PPLK}$.

Table 1. V_{CC} and V_{PP} Voltage Combinations Offered by SmartVoltage Technology

V_{CC} Voltage	V_{PP} Voltage
2.7V-3.6V(1)	3.0V-3.6V

NOTE:

1. Block erase, byte write and lock-bit configuration operations with V_{CC}<3.0V are not supported.

Internal V_{CC} and V_{PP} detection Circuitry automatically configures the device for optimized read and write operations.

A Command User Interface (CUI) serves interface between the system processor and internal operation of the device. A valid command sequence written to the CUI initiates device automation. An internal Write State Machine (WSM) automatically executes the algorithms and timings necessary for block erase, byte write, and lock-bit configuration operations.

A block erase operation erases one of the device's 64-Kbyte blocks typically within 0.8 seconds independent of other blocks. Each block can be independently erased 100,000 times (3.2 million block erases per device). Block erase suspend mode allows system software to suspend block erase to read or write data from any other block.

Writing memory data is performed in byte increments typically within 19 µs. Byte write suspend mode enables the system to read data or execute code from any other flash memory array location.

Individual block locking uses a combination of bits, thirty-two block lock-bits and a master lock-bit, to lock and unlock blocks. Block lock-bits gate block erase and byte write operations, while the master lock-bit gates block lock-bit modification. Lock-bit configuration operations (Set Block Lock-Bit, Set Master Lock-Bit, and Clear Block Lock-Bits commands) set and cleared lock-bits.

The status register indicates when the WSM's block erase, byte write, or lock-bit configuration operation is finished.

The RY/$\overline{BY}$ output gives an additional indicator of WSM activity by providing both a hardware signal of status (versus software polling) and status masking (interrupt masking for background block erase, for example). Status polling using RY/$\overline{BY}$ minimizes both CPU overhead and system power consumption. When low, RY/$\overline{BY}$ indicates that the WSM is performing a block erase, byte write, or lock-bit configuration. RY/$\overline{BY}$-high indicates that the WSM is ready for a new command, block erase is suspended (and byte write is inactive), byte write is suspended, or the device is in deep power-down mode.

The access time is 150 ns (t_{AVAV}) over the co[illegible] temperature range (-25°C to +85°C) and V_{CC} supply voltage range of 2.7V-3.6V.

The Automatic Power Savings (APS) feature substantially reduces active current when the device is in static mode (addresses not switching).

When $\overline{CE}$ and $\overline{RP}$ pins are at V_{CC}, the I_{CC} CMOS standby mode is enabled. When the $\overline{RP}$ pin is at GND, deep power-down mode is enabled which minimizes power consumption and provides write protection during reset. A reset time (t_{PHQV}) is required from $\overline{RP}$ switching high until outputs are valid. Likewise, the device has a wake time (t_{PHEL}) from $\overline{RP}$-high until writes to the CUI are recognized. With $\overline{RP}$ at GND, the WSM is reset and the status register is cleared.

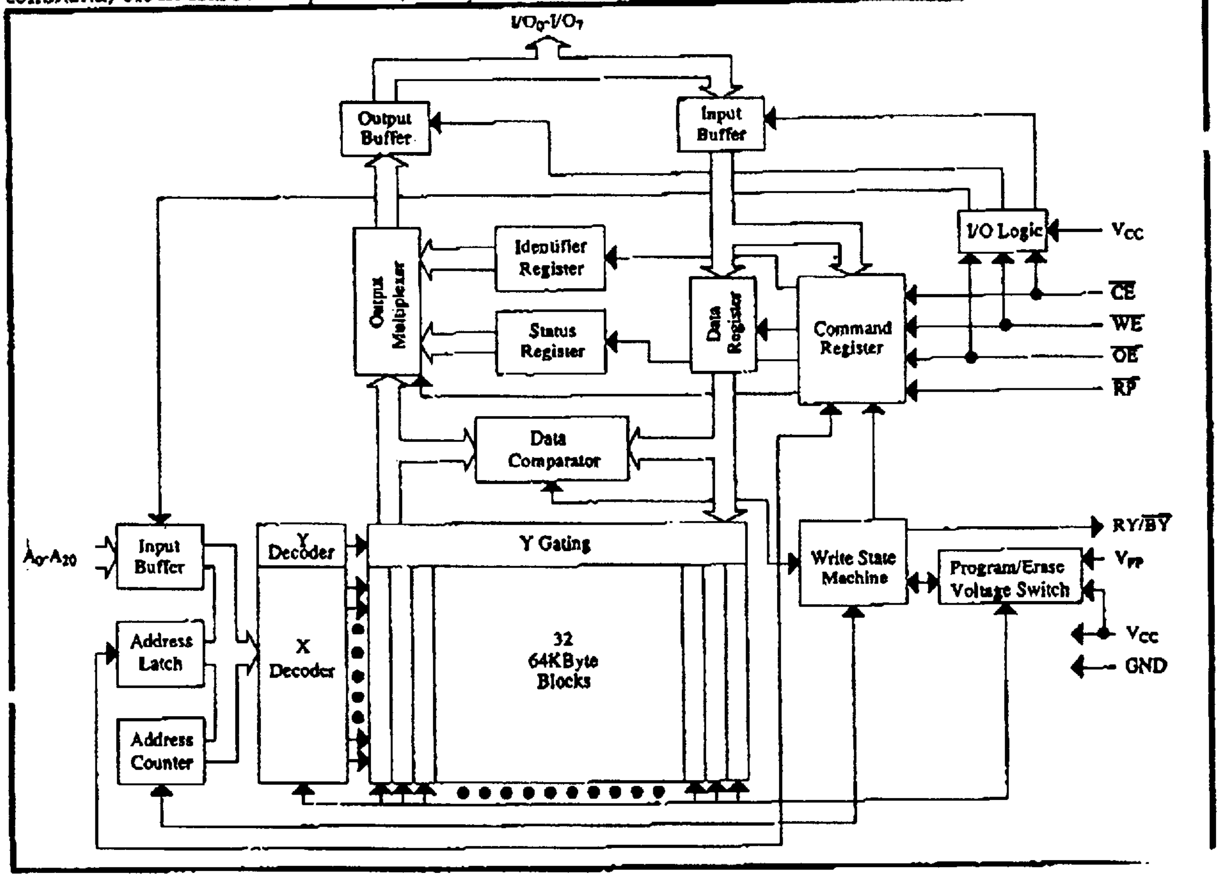


Figure 1. Block Diagram

Table 2. Pin Descriptions

Sym	Type	Name and Function
A_0-A_{20}	INPUT	ADDRESS INPUTS: Inputs for addresses during read and write operations. Addresses are internally latched during a write cycle.
I/O_0-I/O_7	INPUT/ OUTPUT	DATA INPUT/OUTPUTS: Inputs data and commands during CUI write cycles; outputs data during memory array, status register, and identifier code read cycles. Data pins float to high-impedance when the chip is deselected or outputs are disabled. Data is internally latched during a write cycle.
$\overline{CE}$	INPUT	CHIP ENABLE: Activates the device's control logic, input buffers, decoders, and sense amplifiers. $\overline{CE}$-high deselects the device and reduces power consumption to standby levels.
$\overline{RP}$	INPUT	RESET/DEEP POWER-DOWN: Puts the device in deep power-down mode and resets internal automation. $\overline{RP}$-high enables normal operation. When driven low, $\overline{RP}$ inhibits write operations which provides data protection during power transitions. Exit from deep power-down sets the device to read array mode. $\overline{RP}$ at V_{HH} enables setting of the master lock-bit and enables configuration of block lock-bits when the master lock-bit is set. $\overline{RP}=V_{HH}$ overrides block lock-bits thereby enabling block erase and byte write operations to locked memory blocks. Block erase, byte write, or lock-bit configuration with $V_{IH}<\overline{RP}<V_{HH}$ produce spurious results and should not be attempted.
$\overline{OE}$	INPUT	OUTPUT ENABLE: Gates the device's outputs during a read cycle.
$\overline{WE}$	INPUT	WRITE ENABLE: Controls writes to the CUI and array blocks. Addresses and data are latched on the rising edge of the $\overline{WE}$ pulse.
RY/$\overline{BY}$	OUTPUT	READY/$\overline{BUSY}$: Indicates the status of the internal WSM. When low, the WSM is performing an internal operation (block erase, byte write, or lock-bit configuration). RY/$\overline{BY}$-high indicates that the WSM is ready for new commands, block erase is suspended, and byte write is inactive, byte write is suspended, or the device is in deep power-down mode. RY/$\overline{BY}$ is always active and does not float when the chip is deselected or data outputs are disabled.
V_{PP}	SUPPLY	BLOCK ERASE, BYTE WRITE, LOCK-BIT CONFIGURATION POWER SUPPLY: For erasing array blocks, writing bytes, or configuring lock-bits. With $V_{PP} \le V_{PPLK}$, memory contents cannot be altered. Block erase, byte write, and lock-bit configuration with an invalid V_{PP} (see DC Characteristics) produce spurious results and should not be attempted.
V_{CC}	SUPPLY	DEVICE POWER SUPPLY: Do not float any power pins. With $V_{CC} \le V_{LKO}$, all write attempts to the flash memory are inhibited. Device operations at invalid V_{CC} voltage (see DC Characteristics) produce spurious results and should not be attempted. Block erase, byte write and lock-bit configuration operations with $V_{CC}<3.0V$ are not supported.
GND	SUPPLY	GROUND: Do not float any ground pins.
NC		NO CONNECT: Lead is not internal connected; it may be driven or floated.

Note:
V_{CC}, V_{PP}, $\overline{CE}$, $\overline{RP}$, $\overline{WE}$ and $\overline{OE}$ mean F-V_{CC}, F-V_{PP}, F-$\overline{CE}$, F-$\overline{RP}$, F-$\overline{WE}$ and F-$\overline{OE}$.

2 PRINCIPLES OF OPERATION

The LRS1310A SmartVoltage Flash memory includes an on-chip WSM to manage block erase, byte write, and lock-bit configuration functions. It allows for: 100% TTL-level control inputs, fixed power supplies during block erasure, byte write, and lock-bit configuration, and minimal processor overhead with RAM-Like interface timings.

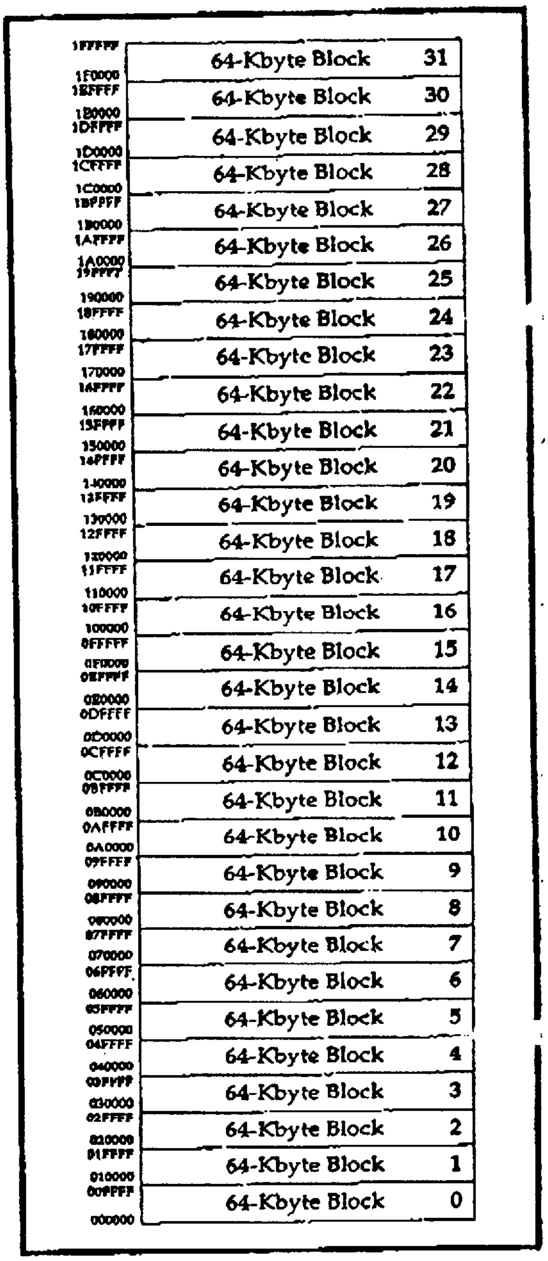
After initial device power-up or return from deep power-down mode (see Bus Operations), the device defaults to read array mode. Manipulation of external memory control pins allow array read, standby, and output disable operations.

Status register and identifier codes can be accessed through the CUI independent of the V_{PP} voltage. High voltage on V_{PP} enables successful block erasure, byte writing, and lock-bit configuration. All functions associated with altering memory contents–block erase, byte write, Lock-bit configuration, status, and identifier codes–are accessed via the CUI and verified through the status register.

Commands are written using standard microprocessor write timings. The CUI contents serve as input to the WSM, which controls the block erase, byte write, and lock-bit configuration. The internal algorithms are regulated by the WSM, including pulse repetition, internal verification, and margining of data. Addresses and data are internally latch during write cycles. Writing the appropriate command outputs array data, accesses the identifier codes, or outputs status register data.

Interface software that initiates and polls progress of block erase, byte write, and lock-bit configuration can be stored in any block. This code is copied to and executed from system RAM during flash memory updates. After successful completion, reads are again possible via the Read Array command. Block erase suspend allows system software to suspend a block erase to read or write data from any other block. Byte write suspend allows system software to suspend a byte write to read data from any other flash memory array location.

Figure 2. Memory Map



2.1 Data Protection

Depending on the application, the system designer may choose to make the V_{PP} power supply switchable (available only when memory block erases, byte writes, or lock-bit configurations are required) or hardwired to V_{PPH}. The device accommodates either design practice and encourages optimization of the processor-memory interface.

When $V_{PP} \le V_{PPLK}$, memory contents cannot be altered. The CUI, with two-step block erase, byte write, or lock-bit configuration command sequences, provides protection from unwanted operations even when high voltage is applied to V_{PP}. All write functions are disabled when V_{CC} is below the write lockout voltage V_{LKO} or when $\overline{RP}$ is at V_{IL}. The device's block locking capability provides additional protection from inadvertent code or data alteration by gating erase and byte write operations.

3 BUS OPERATION

The local CPU reads and writes flash memory in-system. All bus cycles to or from the flash memory conform to standard microprocessor bus cycles.

3.1 Read

Information can be read from any block, identifier codes, or status register independent of the V_{PP} voltage. $\overline{RP}$ can be at either V_{IH} or V_{HH}.

The first task is to write the appropriate read mode command (Read Array, Read Identifier Codes, or Read Status Register) to the CUI. Upon initial device power-up or after exit from deep power-down mode, the device automatically resets to read array mode. Four control pins dictate the data flow in and out of the component: $\overline{CE}$, $\overline{OE}$, $\overline{WE}$, and $\overline{RP}$. $\overline{CE}$ and $\overline{OE}$ must be driven active to obtain data at the outputs. $\overline{CE}$ is the device selection control, and when active enables the selected memory device. $\overline{OE}$ is the data output (I/O_0-I/O_7) control and when active drives the selected memory data onto the I/O bus. $\overline{WE}$ must be at V_{IH} and $\overline{RP}$ must be at V_{IH} or V_{HH}. Figure 12 illustrates a read cycle.

3.2 Output Disable

With $\overline{OE}$ at a logic-high level (V_{IH}), the device outputs are disabled. Output pins I/O_0-I/O_7 are placed in a high-impedance state.

3.3 Standby

$\overline{CE}$ at a logic-high level (V_{IH}) places the device in standby mode which substantially reduces device power consumption. I/O_0-I/O_7 outputs are placed in a high-impedance state independent of $\overline{OE}$. If deselected during block erase, byte write, or lock-bit configuration, the device continues functioning, and consuming active power until the operation completes.

3.4 Deep Power-Down

$\overline{RP}$ at V_{IL} initiates the deep power-down mode.

In read modes, $\overline{RP}$-low deselects the memory, places output drivers in a high-impedance state and turns off all internal circuits. $\overline{RP}$ must be held low for a minimum of 100 ns. Time t_{PHQV} is required after return from power-down until initial memory access outputs are valid. After this wake-up interval, normal operation is restored. The CUI is reset to read array mode and status register is set to 80H.

During block erase, byte write, or lock-bit configuration modes, $\overline{RP}$-low will abort the operation. RY/$\overline{BY}$ remains low until the reset operation is complete. Memory contents being altered are no longer valid; the data may be partially erased or written. Time t_{PHWL} is required after $\overline{RP}$ goes to logic-high (V_{IH}) before another command can be written.

As with any automated device, it is important to assert $\overline{RP}$ during system reset. When the system comes out of reset, it expects to read from the flash memory. Automated flash memories provide status information when accessed during block erase, byte write, or lock-bit configuration modes. If a CPU reset occurs with no flash memory reset, proper CPU initialization may not occur because the flash memory may be providing status information instead of array data. SHARP's flash memories allow proper CPU initialization following a system reset through the use of the $\overline{RP}$ input. In this application, $\overline{RP}$ is controlled by the same $\overline{RESET}$ signal that resets the system CPU.

3.5 Read Identifier Codes Operation

The read identifier codes operation outputs the manufacturer code, device code, block lock configuration codes for each block, and the master lock configuration code (see Figure 3). Using the manufacturer and device codes, the system CPU can automatically match the device with its proper algorithms. The block lock and master lock configuration codes identify locked and unlocked blocks and master lock-bit setting.

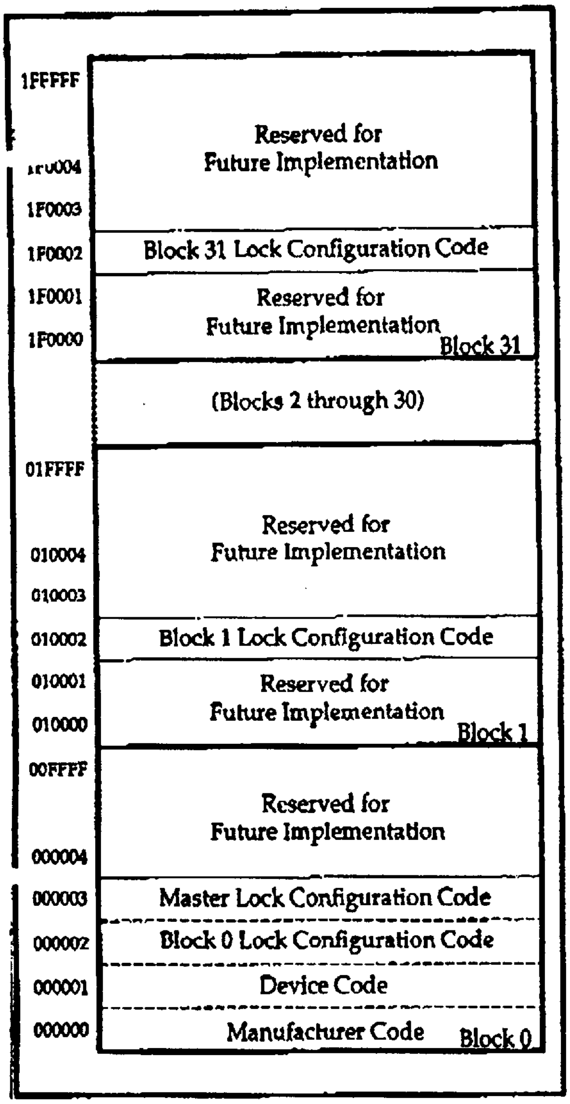


Figure 3. Device Identifier Code Memory Map

3.6 Write

Writing commands to the CUI enable reading of device data and identifier codes. They also control inspection and clearing of the status register. When $V_{CC}=V_{CC2}$ and $V_{PP}=V_{PPH}$, the CUI additionally controls block erasure, byte write, and lock-bit configuration.

The Block Erase command requires appropriate command data and an address within the block to be erased. The Byte Write command requires the command and address of the location to be written. Set Master and Block Lock-Bit commands require the command and address within the device (Master Lock) or block within the device (Block Lock) to be locked. The Clear Block Lock-Bits command requires the command and address within the device.

The CUI does not occupy an addressable memory location. It is written when $\overline{WE}$ and $\overline{CE}$ are active. The address and data needed to execute a command are latched on the rising edge of $\overline{WE}$ or $\overline{CE}$ (whichever goes high first). Standard microprocessor write timings are used. Figures 13 and 14 illustrate $\overline{WE}$ and $\overline{CE}$-controlled write operations.

4 COMMAND DEFINITIONS

When the V_{PP} voltage ≤ V_{PPLK}, Read operations from the status register, identifier codes, or blocks are enabled. Placing V_{PPH} on V_{PP} enables successful block erase, byte write and lock-bit configuration operations.

Device operations are selected by writing specific commands into the CUI. Table 4 defines these commands.

Table 3. Bus Operations

Mode	Notes	$\overline{RP}$	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Address	V_{PP}	I/O_{0-7}	RY/$\overline{BY}$
Read	1,2,3,8	V_{IH} or V_{HH}	V_{IL}	V_{IL}	V_{IH}	X	X	D_{OUT}	X
Output Disable	3	V_{IH} or V_{HH}	V_{IL}	V_{IH}	V_{IH}	X	X	High Z	X
Standby	3	V_{IH} or V_{HH}	V_{IH}	X	X	X	X	High Z	X
Deep Power-Down	4	V_{IL}	X	X	X	X	X	High Z	V_{OH}
Read Identifier Codes		V_{IH} or V_{HH}	V_{IL}	V_{IL}	V_{IH}	See Figure 3	X	Note 5	V_{OH}
Write	3,6,7,8	V_{IH} or V_{HH}	V_{IL}	V_{IH}	V_{IL}	X	X	D_{IN}	X

NOTES:

1. Refer to DC Characteristics. When $V_{PP} \leq V_{PPLK}$, memory contents can be read, but not altered.
2. X can be V_{IL} or V_{IH} for control pins and addresses, and V_{PPLK} or V_{PPH} for V_{PP}. See DC Characteristics for V_{PPLK} and V_{PPH} voltages.
3. RY/$\overline{BY}$ is V_{OL} when the WSM is executing internal block erase, byte write, or lock-bit configuration algorithms. It is V_{OH} during when the WSM is not busy, in block erase suspend mode (with byte write inactive), byte write suspend mode, or deep power-down mode.
4. $\overline{RP}$ at GND±0.2V ensures the lowest deep power-down current.
5. See Section 4.2 for read identifier code data.
6. Command writes involving block erase, write, or lock-bit configuration are reliably executed when $V_{PP}=V_{PPH}$ and $V_{CC}=V_{CC2}$. Block erase, byte write, or lock-bit configuration with $V_{CC}<3.0V$ or $V_{IH}<\overline{RP}<V_{HH}$ produce spurious results and should not be attempted.
7. Refer to Table 4 for valid D_{IN} during a write operation.
8. Don't use the timing both $\overline{OE}$ and $\overline{WE}$ are V_{IL}.

Table 4. Command Definitions[9]

Command	Bus Cycles Req'd.	Notes	First Bus Cycle			Second Bus Cycle		
			Oper[1]	Addr[2]	Data[3]	Oper[1]	Addr[2]	Data[3]
Read Array/Reset	1		Write	X	FFH			
Read Identifier Codes	≥2	4	Write	X	90H	Read	IA	ID
Read Status Register	2		Write	X	70H	Read	X	SRD
Clear Status Register	1		Write	X	50H			
Block Erase	2	5	Write	BA	20H	Write	BA	D0H
Byte Write	2	5,6	Write	WA	40H or 10H	Write	WA	WD
Block Erase and Byte Write Suspend	1	5	Write	X	B0H			
Block Erase and Byte Write Resume	1	5	Write	X	D0H			
Set Block Lock-Bit	2	7	Write	BA	60H	Write	BA	01H
Set Master Lock-Bit	2	7	Write	X	60H	Write	X	F1H
Clear Block Lock-Bits	2	8	Write	X	60H	Write	X	D0H

NOTES:

1. BUS operations are defined in Table 3.
2. X=Any valid address within the device.
   IA=Identifier Code Address: see Figure 3.
   BA=Address within the block being erased or locked.
   WA=Address of memory location to be written.
3. SRD=Data read from status register. See Table 7 for a description of the status register bits.
   WD=Data to be written at location WA. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$ (whichever goes high first).
   ID=Data read from identifier codes.
4. Following the Read Identifier Codes command, read operations access manufacturer, device, block lock, and master lock codes. See Section 4.2 for read identifier code data.
5. If the block is locked, $\overline{RP}$ must be at V_{HH} to enable block erase or byte write operations. Attempts to issue a block erase or byte write to a locked block while $\overline{RP}$ is V_{IH}.
6. Either 40H or 10H are recognized by the WSM as the byte write setup.
7. If the master lock-bit is set, $\overline{RP}$ must be at V_{HH} to set a block lock-bit. $\overline{RP}$ must be at V_{HH} to set the master
   If the master lock-bit is not set, a block lock-bit can be set while $\overline{RP}$ is V_{IH}.
8. If the master lock-bit is set, $\overline{RP}$ must be at V_{HH} to clear block lock-bits. The clear block lock-bits operation simultaneously clears all block lock-bits. If the master lock-bit is not set, the Clear Block Lock-Bits command can be done while $\overline{RP}$ is V_{IH}.
9. Commands other than those shown above are reserved by SHARP for future device implementations and should not be used.

4.1 Read Array Command

Upon initial device power-up and after exit from deep power-down mode, the device defaults to read array mode. This operation is also initiated by writing the Read Array command. The device remains enabled for reads until another command is written. Once the internal WSM has started a block erase, byte write or lock-bit configuration, the device will not recognize the Read Array command until the WSM completes its operation unless the WSM is suspended via an Erase Suspend or Byte Write Suspend command. The Read Array command functions independently of the V_{PP} voltage and $\overline{\text{RP}}$ can be V_{IH} or V_{HH}.

4.2 Read Identifier Codes Command

The identifier code operation is initiated by writing the Read Identifier Codes command. Following the command write, read cycles from addresses shown in Figure 3 retrieve the manufacturer, device, block lock configuration and master lock configuration codes (see Table 5 for identifier code values). To terminate the operation, write another valid command. Like the Read Array command, the Read Identifier Codes command functions independently of the V_{PP} voltage and $\overline{\text{RP}}$ can be V_{IH} or V_{HH}. Following the Read Identifier Codes command, the following information can be read:

Table 5. Identifier Codes

Code	Address	Data
Manufacture Code	00000	89
Device Code	00001	AA
Block Lock Configuration	X0002[1]	▨
·Block is Unlocked		$I/O_0=0$
·Block is Locked		$I/O_0=1$
·Reserved for Future Use		I/O_{1-7}
Master Lock Configuration	00003	▨
·Device is Unlocked		$I/O_0=0$
·Device is Locked		$I/O_0=1$
·Reserved for Future Use		I/O_{1-7}

NOTE:

1. X selects the specific block lock configuration code to be read. See Figure 3 for the device identifier code memory map.

4.3 Read Status Register Command

The status register may be read to determine when a block erase, byte write, or lock-bit configuration is complete and whether the operation completed successfully. It may be read at any time by writing the Read Status Register command. After writing this command, all subsequent read operations output data from the status register until another valid command is written. The status register contents are latched on the falling edge of $\overline{\text{OE}}$ or $\overline{\text{CE}}$, whichever occurs. $\overline{\text{OE}}$ or $\overline{\text{CE}}$ must toggle to V_{IH} before further reads to update the status register latch. The Read Status [illegible] command functions independently of the V_{PP} voltage. $\overline{\text{RP}}$ can be V_{IH} or V_{HH}.

4.4 Clear Status Register Command

Status register bits SR.5, SR.4, SR.3, and SR.1 are set to "1"s by the WSM and can only be reset by the Clear Status Register command. These bits indicate various failure conditions (see Table 7). By allowing system software to reset these bits, several operations (such as cumulatively erasing or locking multiple blocks or writing several bytes in sequence) may be performed. The status register may be polled to determine if an error occurre during the sequence.

To clear the status register, the Clear Status Register command (50H) is written. It functions independently of the applied V_{PP} Voltage. $\overline{\text{RP}}$ can be V_{IH} or V_{HH}. This command is not functional during block erase or byte write suspend modes.

4.5 Block Erase Command

Erase is executed one block at a time and initiated by a two-cycle command. A block erase setup [illegible] written, followed by an block erase confirm. This command sequence requires appropriate sequencing and an address within the block to be erased (erase changes all block data to FFH). Block preconditioning, erase, and verify are handled internally by the WSM (invisible to the system). After the two-cycle block erase sequence is written, the device automatically outputs status register data when read (see Figure 4). The CPU can detect block erase completion by analyzing the output data of the RY/$\overline{\text{BY}}$ pin or status register bit SR.7.

When the block erase is complete, status register bit SR.5 should be checked. If a block erase error is detected, the status register should be cleared before system software attempts corrective actions. The CUI remains in read status register mode until a new command is issued.

This two-step command sequence of set-up followed by execution ensures that block contents are not accidentally erased. An invalid Block Erase command sequence will result in both status register bits SR.4 and SR.5 being set to "1". Also, reliable block erasure [illegible] only occur when $V_{CC}=V_{CC2}$ and $V_{PP}=V_{PPH}$. In the absence of this high voltage, block contents are protected against erasure. If block erase is attempted while $V_{PP} \leq V_{PPLK}$, SR.3 and SR.5 will be set to "1". Successful block erase requires that the corresponding block lock-bit be cleared or, if set, that $\overline{RP}=V_{HH}$. If block erase is attempted when the corresponding block lock-bit is set and $\overline{RP}=V_{IH}$, SR.1 and SR.5 will be set to "1". Block erase operations with $V_{IH}<\overline{RP}<V_{HH}$ produce spurious results and should not be attempted.

4.6 Byte Write Command

Byte write is executed by a two-cycle command sequence. Byte write setup (standard 40H or alternate 10H) is written, followed by a second write that specifies the address and data (latched on the rising edge of $\overline{WE}$). The WSM then takes over, controlling the byte write and write verify algorithms internally. After the byte write sequence is written, the device automatically outputs status register data when read (see Figure 5). The CPU can detect the completion of the byte write event by analyzing the RY/$\overline{BY}$ pin or status register bit SR.7.

[illegible] byte write is complete, status register bit SR.4 should be checked. If byte write error is detected, the status register should be cleared. The internal WSM verify only detects errors for "1"s that do not successfully write to "0"s. The CUI remains in read status register mode until it receives another command.

Reliable byte writes can only occur when $V_{CC}=V_{CC2}$ and $V_{PP}=V_{PPH}$. In the absence of this high voltage, memory contents are protected against byte writes. If byte write is attempted while $V_{PP} \leq V_{PPLK}$, status register bits SR.3 and SR.4 will be set to "1". Successful byte write requires that the corresponding block lock-bit be cleared or, if set, that $\overline{RP}=V_{HH}$. If byte write is attempted when the corresponding block lock-bit is set and $\overline{RP}=V_{IH}$, SR.1 and SR.4 will be set to "1". Byte write operations with $V_{IH}<\overline{RP}<V_{HH}$ produce spurious results and should not be attempted.

4.7 Block Erase Suspend Command

The Block Erase Suspend command allows block-erase interruption to read or byte-write data in another block of memory. Once the block-erase process starts, writing the Block Erase Suspend command requests that the WSM suspend the block erase sequence at a predetermined point in the algorithm. The device outputs status register data when read after the Block Erase Suspend command is written. Polling status register bits SR.7 and SR.6 can determine when the block erase operation has been suspended (both [illegible] be set to "1"). RY/$\overline{BY}$ will also transition to V_{OH}. Specification t_{WHRH2} defines the block erase suspend latency.

At this point, a Read Array command can be written to read data from blocks other than that which is suspended. A Byte Write command sequence can also be issued during erase suspend to program data in other blocks. Using the Byte Write Suspend command (see Section 4.8), a byte write operation can also be suspended. During a byte write operation with block erase suspended, status register bit SR.7 will return to "0" and the RY/$\overline{BY}$ output will transition to V_{OL}. However, SR.6 will remain "1" to indicate block erase suspend status.

The only other valid commands while block erase is suspended are Read Status Register and Block Erase Resume. After a Block Erase Resume command is written to the flash memory, the WSM will continue the block erase process. Status register bits SR.6 and SR.7 will automatically clear and RY/$\overline{BY}$ will return to V_{OL}. After the Erase Resume command is written, the device automatically outputs status register data when read (see Figure 6). V_{PP} must remain at V[illegible] same V_{PP} level used for block erase) while block erase is suspended. $\overline{RP}$ must also remain at V_{IH} or V_{HH} (the same $\overline{RP}$ level used for block erase). Block erase cannot resume until byte write operations initiated during block erase suspend have completed.

4.8 Byte Write Suspend Command

The Byte Write Suspend command allows byte write interruption to read data in other flash memory locations. Once the byte write process starts, writing the Byte Write Suspend command requests that the WSM suspend the byte write sequence at a predetermined point in the algorithm. The device continues to output status register data when read after the Byte Write Suspend command is written. Polling status register bits SR.7 and SR.2 can determine when the byte write operation has been suspended (both will be set to "1"). $RY/\overline{BY}$ will also transition to V_{OH}. Specification t_{WHRH1} defines the byte write suspend latency.

At this point, a Read Array command can be written to read data from locations other than that which is suspended. The only other valid commands while byte write is suspended are Read Status Register and Byte Write Resume. After Byte Write Resume command is written to the flash memory, the WSM will continue the byte write process. Status register bits SR.2 and SR.7 will automatically clear and $RY/\overline{BY}$ will return to V_{OL}. After the Byte Write Resume command is written, the device automatically outputs status register data when read (see Figure 7). V_{PP} must remain at V_{PPH} (the same V_{PP} level used for byte write) while in byte write suspend mode. $\overline{RP}$ must also remain at V_{IH} or V_{HH} (the same $\overline{RP}$ level used for byte write).

4.9 Set Block and Master Lock-Bit Commands

A flexible block locking and unlocking scheme is enabled via a combination of block lock-bits and a master lock-bit. The block lock-bits gate program and erase operations while the master lock-bit gates block-lock bit modification. With the master lock-bit not set, individual block lock-bits can be set using the Set Block Lock-Bit command. The Set Master Lock-Bit command, in conjunction with $\overline{RP}=V_{HH}$, sets the master lock-bit. After the master lock-bit is set, subsequent setting of block lock-bits requires both the Set Block Lock-Bit command and V_{HH} on the $\overline{RP}$ pin. See Table 6 for a summary of hardware and software write protection options.

Set block lock-bit and master lock-bit are executed by a two-cycle command sequence. The set block or master lock-bit setup along with appropriate block or device address is written followed by either the set block lock-bit confirm (and an address within the block to be locked) or the set master lock-bit confirm (and any device address). The WSM then controls the set lock-bit algorithm. After the sequence is written, the device automatically outputs status register data when read (see Figure 8). The CPU can detect the completion of the set lock-bit event by analyzing the $RY/\overline{BY}$ pin output or status register bit SR.7.

When the set lock-bit operation is complete, status register bit SR.4 should be checked. If an error is detected, the status register should be cleared. The CUI will remain in read status register mode until a new command is issued.

This two-step sequence of set-up followed by execution ensures that lock-bits are not accidentally set. An invalid Set Block or Master Lock-Bit command will result in status register bits SR.4 and SR.5 being set to "1". Also, reliable operations occur only when $V_{CC}=V_{CC2}$ and $V_{PP}=V_{PPH}$. In the absence of this high voltage, lock-bit contents are protected against alteration.

A successful set block lock-bit operation requires that the master lock-bit be cleared or, if the master lock-bit is set, that $\overline{RP}=V_{HH}$. If it is attempted with the master lock-bit set and $\overline{RP}=V_{IH}$, SR.1 and SR.4 will be set to "1" and the operation will fail. Set block lock-bit operations while $V_{IH}<\overline{RP}<V_{HH}$ produce spurious results and should not be attempted. A successful set master lock-bit operation requires that $\overline{RP}=V_{HH}$. If it is attempted with $\overline{RP}=V_{IH}$, SR.1 and SR.4 will be set to "1" and the operation will fail. Set master lock-bit operations with $V_{IH}<\overline{RP}<V_{HH}$ produce spurious results and should not be attempted.

4.10 Clear Block Lock-Bits Command

All set block lock-bits are cleared in parallel via the Clear Block Lock-Bits command. With the master lock-bit not set, block lock-bits can be cleared using only the Clear Block Lock-Bits command. If the master lock-bit is set, clearing block lock-bits requires both the Clear Block Lock-Bits command and V_{HH} on the $\overline{RP}$ pin. See Table 6 for a summary of hardware and software write protection options.

Clear block lock-bits operation is executed by a two-cycle command sequence. A clear block lock-bits setup is first written. After the command is written, the device automatically outputs status register data when read (see Figure 9). The CPU can detect completion of the clear block lock-bits event by analyzing the RY/$\overline{BY}$ Pin output or status register bit SR.7.

When the operation is complete, status register bit SR.5 should be checked. If a clear block lock-bit error is detected, the status register should be cleared. The CUI will remain in read status register mode until another command is issued.

This two-step sequence of set-up followed by execution ensures that block lock-bits are not accidentally cleared. An invalid Clear Block Lock-Bits command sequence will result in status register bits SR.4 and SR.5 being set to "1". Also, a reliable [illegible] block lock-bits operation can only occur when $V_{CC}=V_{CC2}$ and $V_{PP}=V_{PPH}$. If a clear block lock-bits operation is attempted while $V_{PP} \leq V_{PPLK}$, SR.3 and SR.5 will be set to "1". In the absence of this high voltage, the block lock-bits content are protected against alteration. A successful clear block lock-bits operation requires that the master lock-bit is not set or, if the master lock-bit is set, that $\overline{RP}=V_{HH}$. If it is attempted with the master lock-bit set and $\overline{RP}=V_{IH}$, SR.1 and SR.5 will be set to "1" and the operation will fail. A clear block lock-bits operation with $V_{IH}<\overline{RP}<V_{HH}$ produce spurious results and should not be attempted.

If a clear block lock-bits operation is aborted due to V_{PP} or V_{CC} transitioning out of valid range or $\overline{RP}$ active transition, block lock-bit values are left in an undetermined state. A repeat of clear block lock-bits is required to initialize block lock-bit contents to known values. Once the master lock-bit is set, it cannot be cleared.

Table 6. Write Protection Alternatives

Operation	Master Lock-Bit	Block Lock-Bit	$\overline{RP}$	Effect
Block Erase or Byte Write	X	0	V_{IH} or V_{HH}	Block Erase and Byte Write Enabled
		1	V_{IH}	Block is Locked. Block Erase and Byte Write Disabled
			V_{HH}	Block Lock-Bit Override. Block Erase and Byte Write Enabled
Set Block Lock-Bit	0	X	V_{IH} or V_{HH}	Set Block Lock-Bit Enabled
	1	X	V_{IH}	Master Lock-Bit is Set. Set Block Lock-Bit Disabled
			V_{HH}	Master Lock-Bit Override. Set Block Lock-Bit Enabled
Set Master Lock-Bit	X	X	V_{IH}	Set Master Lock-Bit Disabled
			V_{HH}	Set Master Lock-Bit Enabled
Clear Block Lock-Bits	0	X	V_{IH} or V_{HH}	Clear Block Lock-Bits Enabled
	1	X	V_{IH}	Master Lock-Bit is Set. Clear Block Lock-Bits Disabled
			V_{HH}	Master Lock-Bit Override. Clear Block Lock-Bits Enabled

Table 7. Status Register Definition

WSMS	ESS	ECLBS	BWSLBS	VPPS	BWSS	DPS	R
7	6	5	4	3	2	1	0

SR.7 = WRITE STATE MACHINE STATUS
  1 = Ready
  0 = Busy

SR.6 = ERASE SUSPEND STATUS
  1 = Block Erase Suspended
  0 = Block Erase in Progress/Completed

SR.5 = ERASE AND CLEAR LOCK-BITS STATUS
  1 = Error in Block Erasure or Clear Lock-Bits
  0 = Successful Block Erase or Clear Lock-Bits

SR.4 = BYTE WRITE AND SET LOCK-BIT STATUS
  1 = Error in Byte Write or Set Master/Block Lock-Bit
  0 = Successful Byte Write or Set Master/Block Lock-Bit

SR.3 = V_{PP} STATUS
  1 = V_{PP} Low Detect, Operation Abort
  0 = V_{PP} OK

[illegible] = BYTE WRITE SUSPEND STATUS
  1 = Byte Write Suspended
  0 = Byte Write in Progress/Completed

SR.1 = DEVICE PROTECT STATUS
  1 = Master Lock-Bit, Block Lock-Bit and/or $\overline{RP}$ Lock Detected, Operation Abort
  0 = Unlock

SR.0 = RESERVED FOR FUTURE ENHANCEMENTS

NOTES:

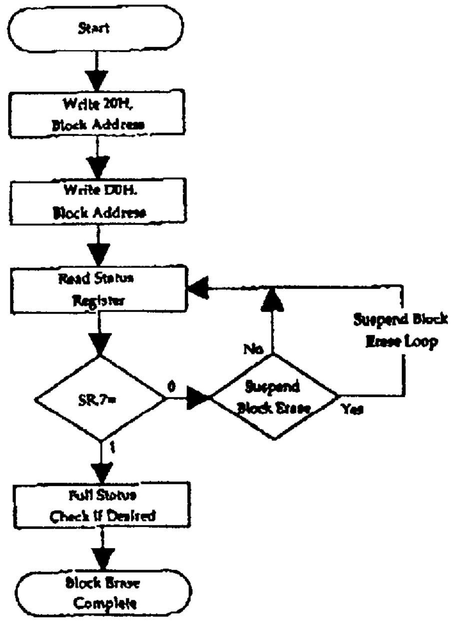
Check RY/$\overline{BY}$ or SR.7 to determine block erase, byte write, or lock-bit configuration completion.
SR.6-0 are invalid while SR.7="0".

If both SR.5 and SR.4 are "1"s after a block erase or lock-bit configuration attempt, an improper command sequence was entered.

SR.3 does not provide a continuous indication of V_{PP} level. The WSM interrogates and indicates the V_{PP} level only after Block Erase, Byte Write, Set Block/Master Lock-Bit, or Clear Block Lock-Bits command sequences. SR.3 is not guaranteed to reports accurate feedback only when $V_{PP}=V_{PPH}$.

SR.1 does not provide a continuous indication of master and block lock-bit values. The WSM interrogates the master lock-bit, block lock-bit, and $\overline{RP}$ only after Block Erase, Byte Write, or Lock-Bit configuration command sequences. It informs the system, depending on the attempted operation, if the block lock-bit is set, master lock-bit is set, and/or $\overline{RP}$ is not V_{HH}. Reading the block lock and master lock configuration codes after writing the Read Identifier Codes command indicates master and block lock-bit status.

SR.0 is reserved for future use and should be masked out when polling the status register.



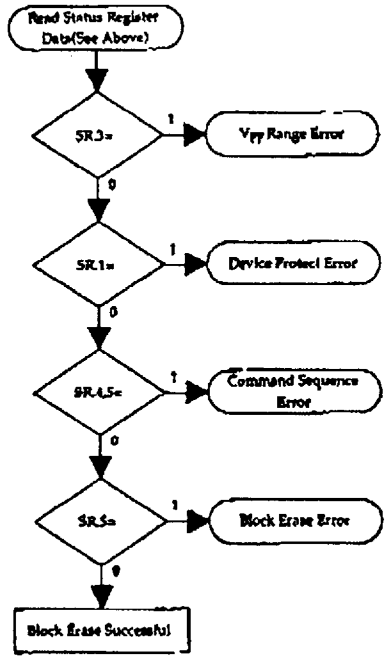
Bus Operation	Command	Comments
Write	Erase Setup	Data=20H Addr=Within Block to be Erased
Write	Erase Confirm	Data=D0H Addr=Within Block to be Erased
Read		Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy

Repeat for subsequent block erasures.

Full status check can be done after each block erase or after a sequence of block erasures.

Write FFH after the last operation to place device in read array mode.

FULL STATUS CHECK PROCEDURE

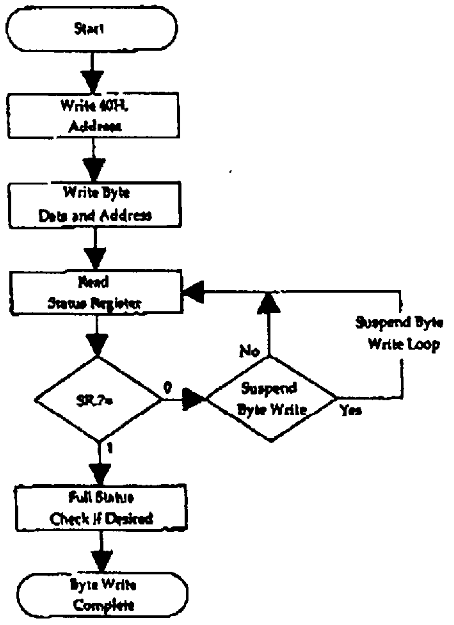


Bus Operation	Command	Comments
Standby		Check SR.3 1=V_{PP} Error Detect
Standby		Check SR.1 1=Device Protect Detect $\overline{RP}=V_{IH}$,Block Lock-Bit is Set Only required for systems implementing lock-bit configuration
Standby		Check SR.4,5 Both 1=Command Sequence Error
Standby		Check SR.5 1=Block Erase Error

SR.5,SR.4,SR.3 and SR.1 are only cleared by the Clear Status Register Command in cases where multiple blocks are erased before full status is checked.

If error is detected, clear the Status Register before attempting retry or other error recovery.

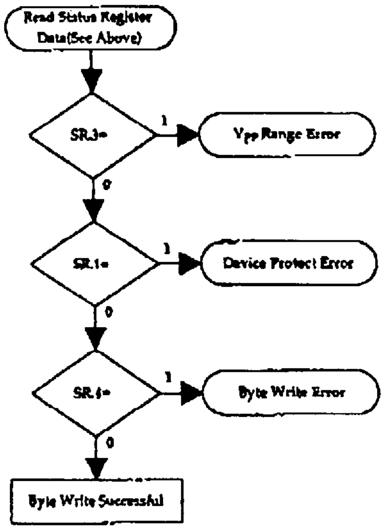
Figure 4. Automated Block Erase Flowchart



Bus Operation	Command	Comments
Write	Setup Byte Write	Data=40H Addr=Location to Be Written
Write	Byte Write	Data=Data to Be Written Addr=Location to Be Written
Read		Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy

Repeat for subsequent byte writes.
SR full status check can be done after each byte write, or after a sequence of byte writes.
Write FFH after the last byte write operation to place device in read array mode.

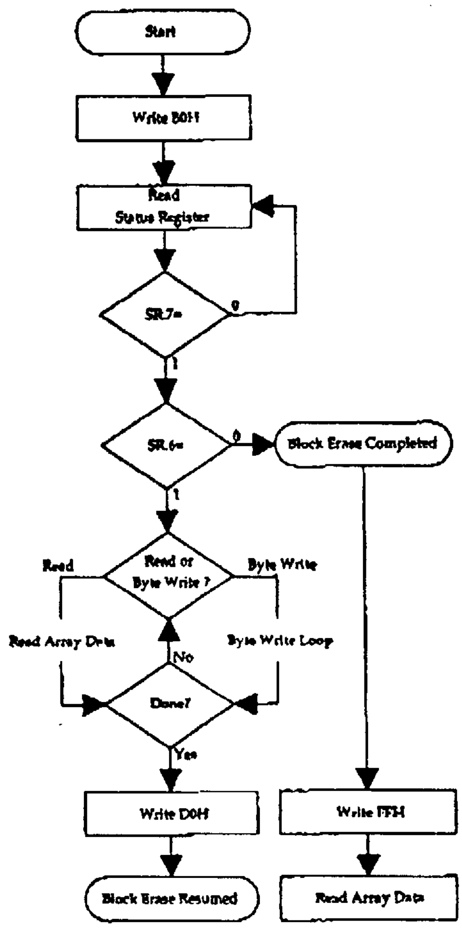
FULL STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Standby		Check SR.3 1=V_{PP} Error Detect
Standby		Check SR.1 1=Device Protect Detect $\overline{RP}=V_{IH}$,Block Lock-Bit is Set Only required for systems implementing lock-bit configuration
Standby		Check SR.4 1=Data Write Error

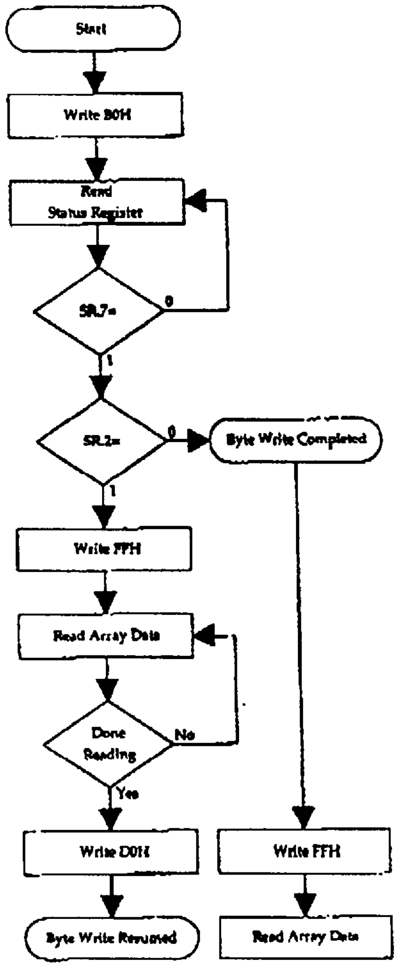
SR.4,SR.3 and SR.1 are only cleared by the Clear Status Register command in cases where multiple locations are written before full status is checked.
If error is detected, clear the Status Register before attempting retry or other error recovery.

Figure 5. Automated Byte Write Flowchart



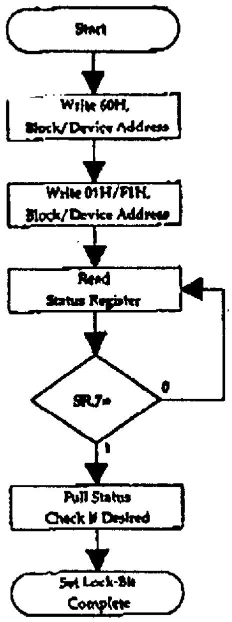
Bus Operation	Command	Comments
Write	Erase Suspend	Data=B0H Addr=X
Read		Status Register Data Addr=X
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Standby		Check SR.6 1=Block Erase Suspended 0=Block Erase Completed
Write	Erase Resume	Data=D0H Addr=X

Figure 6. Block Erase Suspend/Resume Flowchart



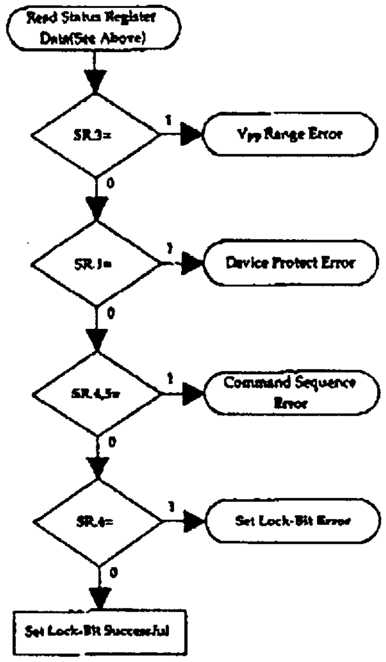
Bus Operation	Command	Comments
Write	Byte Write Suspend	Data=B0H Addr=X
Read		Status Register Data Addr=X
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Standby		Check SR.2 1=Byte Write Suspended 0=Byte Write Completed
Write	Read Array	Data=FFH Addr=X
Read		Read Array locations other than that being written.
Write	Byte Write Resume	Data=D0H Addr=X

Figure 7. Byte Write Suspend/Resume Flowchart



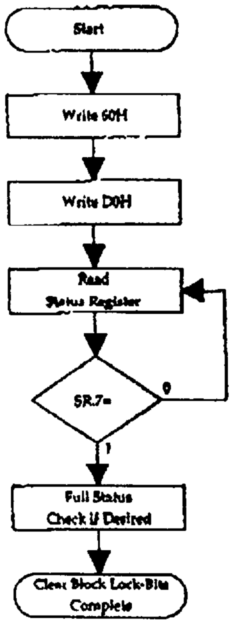
Bus Operation	Command	Comments
Write	Set Block/Master Lock-Bit Setup	Data=60H Addr=Block Address(Block), Device Address(Master)
Write	Set Block or Master Lock-Bit Confirm	Data=01H(Block), F1H(Master) Addr=Block Address(Block), Device Address(Master)
Read		Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Repeat for subsequent lock-bit set operations. Full status check can be done after each lock-bit set operation or after a sequence of lock-bit set operations. Write FFH after the last lock-bit set operation to place device in read array mode.		

FULL STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Standby		Check SR.3 1=V_{PP} Error Detect
Standby		Check SR.1 1=Device Protect Detect $\overline{RP}=V_{IH}$ (Set Master Lock-Bit Operation) $\overline{RP}=V_{HH}$, Master Lock-Bit is Set (Set Block Lock-Bit Operation)
Standby		Check SR.4,5 Both 1=Command Sequence Error
Standby		Check SR.4 1=Set Lock-Bit Error
SR.5,SR.4,SR.3 and SR.1 are only cleared by the Clear Status Register command in cases where multiple lock-bits are set before full status is checked. If error is detected, clear the Status Register before attempting retry or other error recovery.		

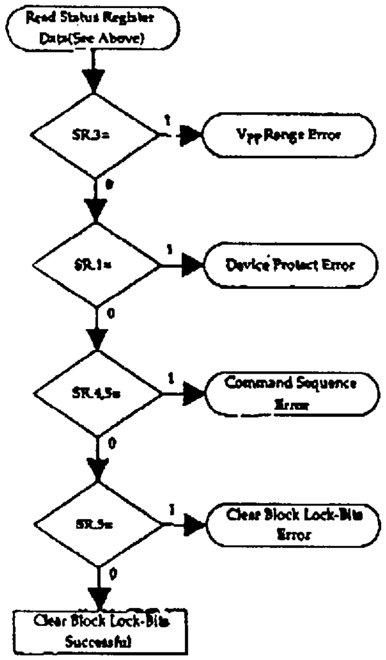
Figure 8. Set Block and Master Lock-Bit Flowchart



Bus Operation	Command	Comments
Write	Clear Block Lock-Bits Setup	Data=60H Addr=X
Write	Clear Block Lock-Bits Confirm	Data=D0H Addr=X
Read		Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy

Write FFH after the Clear Block Lock-Bits operation to place device in read array mode.

FULL STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Standby		Check SR.3 1=V_{PP} Error Detect
Standby		Check SR.1 1=Device Protect Detect $\overline{RP}$=V_{IH}, Master Lock-Bit Is Set
Standby		Check SR.4,5 Both 1=Command Sequence Error
Standby		Check SR.5 1=Clear Block Lock-Bits Error

SR.5,SR.4,SR.3 and SR.1 are only cleared by the Clear Status Register command.
If error is detected, clear the Status Register before attempting retry or other error recovery.

Figure 9. Clear Block Lock-Bits Flowchart

5 DESIGN CONSIDERATIONS

5.1 Three-Line Output Control

The device will often be used in large memory arrays. SHARP provides three control inputs to accommodate multiple memory connections. Three-line control provides for:

a. Lowest possible memory power dissipation.
b. Complete assurance that data bus contention will not occur.

To use these control inputs efficiently, an address decoder should enable $\overline{CE}$ while $\overline{OE}$ should be connected to all memory devices and the system's $\overline{READ}$ control line. This assures that only selected memory devices have active outputs while deselected memory devices are in standby mode. $\overline{RP}$ should be connected to the system POWERGOOD signal to prevent unintended writes during system power transitions. POWERGOOD should also toggle during system reset.

5.2 RY/$\overline{BY}$ and Block Erase, Byte Write, and Lock-Bit Configuration Polling

RY/$\overline{BY}$ is a full CMOS output that provides a hardware method of detecting block erase, byte write and lock-bit configuration completion. It transitions low after block erase, byte write, or lock-bit configuration commands and returns to V_{OH} when the WSM has finished executing the internal algorithm.

RY/$\overline{BY}$ can be connected to an interrupt input of the system CPU or controller. It is active at all times. RY/$\overline{BY}$ is also V_{OH} when the device is in block erase suspend (with byte write inactive), byte write suspend or deep power-down modes.

5.3 Power Supply Decoupling

Flash memory power switching characteristics require careful device decoupling. System designers are interested in three supply current issues; standby current levels, active current levels and transient peaks produced by falling and rising edges of $\overline{CE}$ and $\overline{OE}$. Transient current magnitudes depend on the device outputs' capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1 µF ceramic capacitor connected between its V_{CC} and GND and between its V_{PP} and GND. These high-frequency, low inductance capacitors should be placed as close as possible to package leads. Additionally, for every eight devices, a 4.7 µF electrolytic capacitor should be placed at the [illegible] power supply connection between V_{CC} and GND. The bulk capacitor will overcome voltage slumps caused by PC board trace inductance.

5.4 V_{PP} Trace on Printed Circuit Boards

Updating flash memories that reside in the target system requires that the printed circuit board designer pay attention to the V_{PP} Power supply trace. The V_{PP} pin supplies the memory cell current for byte writing and block erasing. Use similar trace widths and layout considerations given to the V_{CC} power bus. Adequate V_{PP} supply traces and decoupling will decrease V_{PP} voltage spikes and overshoots.

5.5 V_{CC}, V_{PP}, $\overline{RP}$ Transitions

Block erase, byte write and lock-bit configuration are not guaranteed if V_{PP} falls outside of a valid V_{PPH} range, V_{CC} falls outside of a valid V_{CC2} range, or $\overline{RP} \neq V_{IH}$ or V_{HH}. If V_{PP} error is detected, status register bit SR.3 is set to "1" along with SR.4 or SR.5, depending on the attempted operation. If $\overline{RP}$ transitions to V_{IL} during block erase, byte write, or lock-bit configuration, RY/$\overline{BY}$ will remain low until the reset operation is complete. Then, the operation will abort and the device will enter deep power-down. The aborted operation may leave data partially altered. Therefore, the command sequence must be repeated after normal operation is restored. Device power-off or $\overline{RP}$ transitions to V_{IL} clear the status register.

The CUI latches commands issued by system software and is not altered by V_{PP} or $\overline{CE}$ transitions or WSM actions. Its state is read array mode upon power-up, after exit from deep power-down or after V_{CC} transitions below V_{LKO}.

After block erase, byte write, or lock-bit configuration, even after V_{PP} transitions down to V_{PPLK}, the CUI must be placed in read array mode via the Read Array command if subsequent access to the memory array is desired.

5.6 Power-Up/Down Protection

The device is designed to offer protection against accidental block erasure, byte writing, or lock-bit configuration during power transitions. Upon power-up, the device is indifferent as to which power supply (V_{PP} or V_{CC}) powers-up first. Internal circuitry resets the CUI to read array mode at power-up.

A system designer must guard against spurious writes for V_{CC} voltages above V_{LKO} when V_{PP} is active. Since both $\overline{WE}$ and $\overline{CE}$ must be low for a command write, driving either to V_{IH} will inhibit writes. The CUI's two-step command sequence architecture provides added level of protection against data alteration.

In-system block lock and unlock capability prevents inadvertent data alteration. The device is disabled while $\overline{RP}=V_{IL}$ regardless of its control inputs state.

5.7 Power Dissipation

When designing portable systems, designers must consider battery power consumption not only during device operation, but also for data retention during system idle time. Flash memory's nonvolatility increases usable battery life because data is retained when system power is removed.

In addition, deep power-down mode ensures extremely low power consumption even when system power is applied. For example, portable computing products and other power sensitive applications that use an array of devices for solid-state storage can consume negligible power by lowering $\overline{RP}$ to V_{IL} standby or sleep modes. If access is again needed, the devices can be read following the t_{PHQV} and t_{PHWL} wake-up cycles required after $\overline{RP}$ is first raised to V_{IH}. See AC Characteristics– Read Only and Write Operations and Figures 12, 13 and 14 for more information.

6 ELECTRICAL SPECIFICATIONS

6.1 Absolute Maximum Ratings*

Commercial Operating Temperature
During Read, Block Erase, Byte Write
and Lock-Bit Configuration..........-25°C to +85°C[1]
Temperature under Bias ....-25°C to +85°C

Storage Temperature ....-65°C to +125°C

Voltage On Any Pin
(except V_{CC}, V_{PP}, and $\overline{RP}$) ....-2.0V to +7.0V[2]

V_{CC} Supply Voltage..............................-2.0V to +7.0V[2]

V_{PP} Update Voltage during
Block Erase, Byte Write and
Lock-Bit Configuration..............-2.0V to +14.0V[2,3]

$\overline{RP}$ Voltage with Respect to
GND during Lock-Bit
Configuration Operations.........-2.0V to +14.0V[2,3]

Output Short Circuit Current.......................... 100mA[4]

WARNING: *Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

NOTES:
1. Operating temperature is for commercial product defined by this specification.
2. All specified voltages are with respect to GND. Minimum DC voltage is -0.5V on input/output pins and -0.2V on V_{CC} and V_{PP} pins. During transitions, this level may undershoot to -2.0V for periods <20ns. Maximum DC voltage on input/output pins and V_{CC} is V_{CC}+0.5V which, during transitions, may overshoot to V_{CC}+2.0V for periods <20ns.
3. Maximum DC voltage on V_{PP} and $\overline{RP}$ may overshoot to +14.0V for periods <20ns.
4. Output shorted for no more than one second. No more than one output shorted at a time.

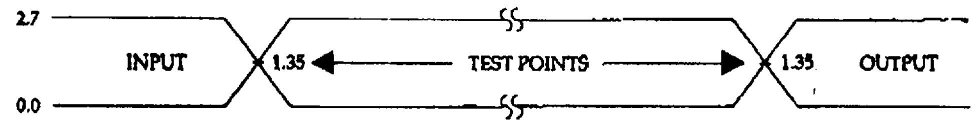
6.2 Operating Conditions

Temperature and V_{CC} Operating Conditions

Symbol	Parameter	Notes	Min	Max	Unit	Test Condition
T_A	Operating Temperature		-25	+85	°C	Ambient Temperature
V_{CC1}	V_{CC} Supply Voltage (2.7V-3.6V)	1	2.7	3.6	V	
V_{CC2}	V_{CC} Supply Voltage (3.0V-3.6V)		3.0	3.6	V	

NOTE:
1. Block erase, byte write and lock-bit configuration operations with V_{CC}<3.0V should not be attempted.

6.2.1 AC INPUT/OUTPUT TEST CONDITIONS



AC test inputs are driven at 2.7V for a Logic "1" and 0.0V for a Logic "0." Input timing begins, and output timing ends, at 1.35V. Input rise and fall times (10% to 90%) <10 ns.

Figure 10. Transient Input/Output Reference Waveform for V_{CC}=2.7V-3.6V

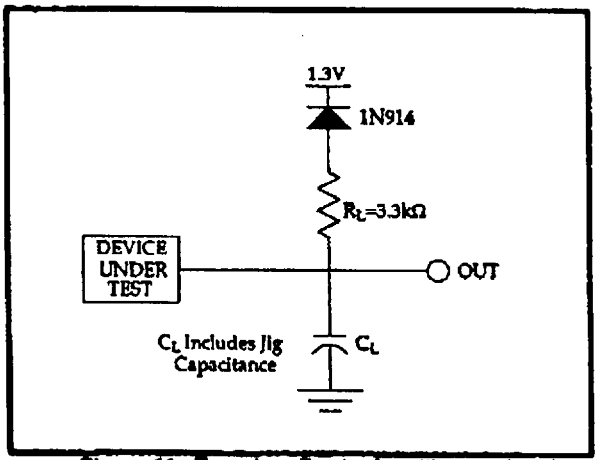


Figure 11. Transient Equivalent Testing Load Circuit

Test Configuration Capacitance Loading Value

Test Configuration	C_L(pF)
V_{CC}= 2.7V-3.6V	50

6.2.2 DC CHARACTERISTICS

DC Characteristics

Sym	Parameter	Notes	V_{CC}=2.7-3.6V		Unit	Test Conditions
			Typ	Max		
I_{LI}	Input Load Current	1		±0.5	µA	$V_{CC}=V_{CC}$Max $V_{IN}=V_{CC}$ or GND
I_{LO}	Output Leakage Current	1		±0.5	µA	$V_{CC}=V_{CC}$Max $V_{OUT}=V_{CC}$ or GND
I_{CCS}	V_{CC} Standby Current	1,3,6	20	100	µA	CMOS Inputs $V_{CC}=V_{CC}$Max $\overline{CE}=\overline{RP}=V_{CC}\pm0.2V$
			0.2	2	mA	TTL Inputs $V_{CC}=V_{CC}$Max $\overline{CE}=\overline{RP}=V_{IH}$
I_{CCD}	V_{CC} Deep Power-Down Current	1		20	µA	$\overline{RP}$=GND±0.2V I_{OUT}(RY/$\overline{BY}$)=0mA
I_{CCR}	V_{CC} Read Current	1,5,6	7	12	mA	CMOS Inputs $V_{CC}=V_{CC}$Max, $\overline{CE}$=GND, I_{OUT}=0mA
			8	18	mA	TTL Inputs $V_{CC}=V_{CC}$Max, $\overline{CE}$=GND f=5MHz, I_{OUT}=0mA
I_{CCW}	V_{CC} Byte Write or Set Lock-Bite Current	1,7		17	mA	$V_{PP}=V_{PPH}$
I_{CCE}	V_{CC} Block Erase or Clear Lock-Bit Current	1,7		17	mA	$V_{PP}=V_{PPH}$
I_{CCWS} I_{CCES}	V_{CC} Byte Write or Block Erase Suspend Current	1,2	1	6	mA	$\overline{CE}=V_{IH}$
I_{PPS} I_{PPR}	V_{PP} Standby or Read Current	1	±2	±15	µA	$V_{PP}\leq V_{CC}$
			10	200	µA	$V_{PP}>V_{CC}$
I_{PPD}	V_{PP} Deep Power-Down Current	1	0.1	5	µA	$\overline{RP}$=GND±0.2V
I_{PPW}	V_{PP} Byte Write or Set Lock-Bite Current	1,7		40	mA	$V_{PP}=V_{PPH}$
I_{PPE}	V_{PP} Block Erase or Clear Lock-Bit Current	1,7		20	mA	$V_{PP}=V_{PPH}$
I_{PPWS} I_{PPES}	V_{PP} Byte Write or Block Erase Suspend Current	1	10	200	µA	$V_{PP}=V_{PPH}$

DC Characteristics (Continued)

Sym	Parameter	Notes	V_{CC}=2.7-3.6V Min	V_{CC}=2.7-3.6V Max	Unit	Test Conditions
V_{IL}	Input Low Voltage	7	-0.5	0.8	V	
V_{IH}	Input High Voltage	7	2.0	V_{CC} +0.5	V	
V_{OL}	Output Low Voltage	3,7		0.4	V	V_{CC}=V_{CC}Min, I_{OL}=2.0mA
V_{OH1}	Output High Voltage (TTL)	3,7	2.4		V	V_{CC}=V_{CC}Min, I_{OH}=-1.0mA
V_{OH2}	Output High Voltage (CMOS)	3,7	0.85 V_{CC}		V	V_{CC}=V_{CC}Min I_{OH}=-2.5mA
			V_{CC} -0.4		V	V_{CC}=V_{CC}Min I_{OH}=-100µA
V_{PPLK}	V_{PP} Lockout during Normal Operations	4,7		1.5	V	
V_{PPH}	V_{PP} during Byte Write, Block Erase or Lock-Bit Operations		3.0	3.6	V	
V_{LKO}	V_{CC} Lockout Voltage		2.0		V	
V_{HH}	$\overline{RP}$ Unlock Voltage	8,9	11.4	12.6	V	Set master lock-bit Override master and block lock-bit

NOTES:

1. All currents are in RMS unless otherwise noted. Contact your local sales office for information about typical specifications.
2. I_{CCWS} and I_{CCES} are specified with the device de-selected. If read or byte written while in erase suspend mode, the device's current draw is the sum of I_{CCWS} or I_{CCES} and I_{CCR} or I_{CCW}, respectively.
3. Includes RY/$\overline{BY}$.
4. Block erases, byte writes, and lock-bit configurations are inhibited when $V_{PP} \leq V_{PPLK}$, and not guaranteed in the range between V_{PPLK}(max) and V_{PPH}(min), and above V_{PPH}(max).
5. Automatic Power Savings (APS) reduces typical I_{CCR} to 3mA at 3.3V V_{CC} in static operation.
6. CMOS inputs are either V_{CC}±0.2V or GND±0.2V. TTL inputs are either V_{IL} or V_{IH}.
7. Sampled, not 100% tested.
8. Master lock-bit set operations are inhibited when $\overline{RP}$=V_{IH}. Block lock-bit configuration operations are inhibited when the master lock-bit is set and $\overline{RP}$=V_{IH}. Block erases and byte writes are inhibited when the corresponding block-lock bit is set and $\overline{RP}$=V_{IH}. Block erase, byte write, and lock-bit configuration operations are not guaranteed with V_{CC}<3.0V or V_{IH}<$\overline{RP}$<V_{HH} and should not be attempted.
9. $\overline{RP}$ connection to a V_{HH} supply is allowed for a maximum cumulative period of 80 hours.

6.2.3 AC CHARACTERISTICS - READ-ONLY OPERATIONS

V_{CC}=2.7V-3.6V, T_A=-25°C to +85°C

Sym	Parameter	Notes	Min	Max	Unit
t_{AVAV}	Read Cycle Time		150		ns
t_{AVQV}	Address to Output Delay			150	ns
t_{ELQV}	$\overline{CE}$ to Output Delay	2		150	ns
t_{PHQV}	$\overline{RP}$ High to Output Delay			600	ns
t_{GLQV}	$\overline{OE}$ to Output Delay	2		50	ns
t_{ELQX}	$\overline{CE}$ to Output in Low Z	3	0		ns
t_{EHQZ}	$\overline{CE}$ High to Output in High Z	3		55	ns
t_{GLQX}	$\overline{OE}$ to Output in Low Z	3	0		ns
t_{GHQZ}	$\overline{OE}$ High to Output in High Z	3		20	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$ Change, Whichever Occurs First	3	0		ns

NOTE:

1. See AC Input/Output Reference Waveform for maximum allowable input slew rate.
2. $\overline{OE}$ may be delayed up to t_{ELQV}-t_{GLQV} after the falling edge of $\overline{CE}$ without impact on t_{ELQV}.
3. Sampled, not 100% tested.

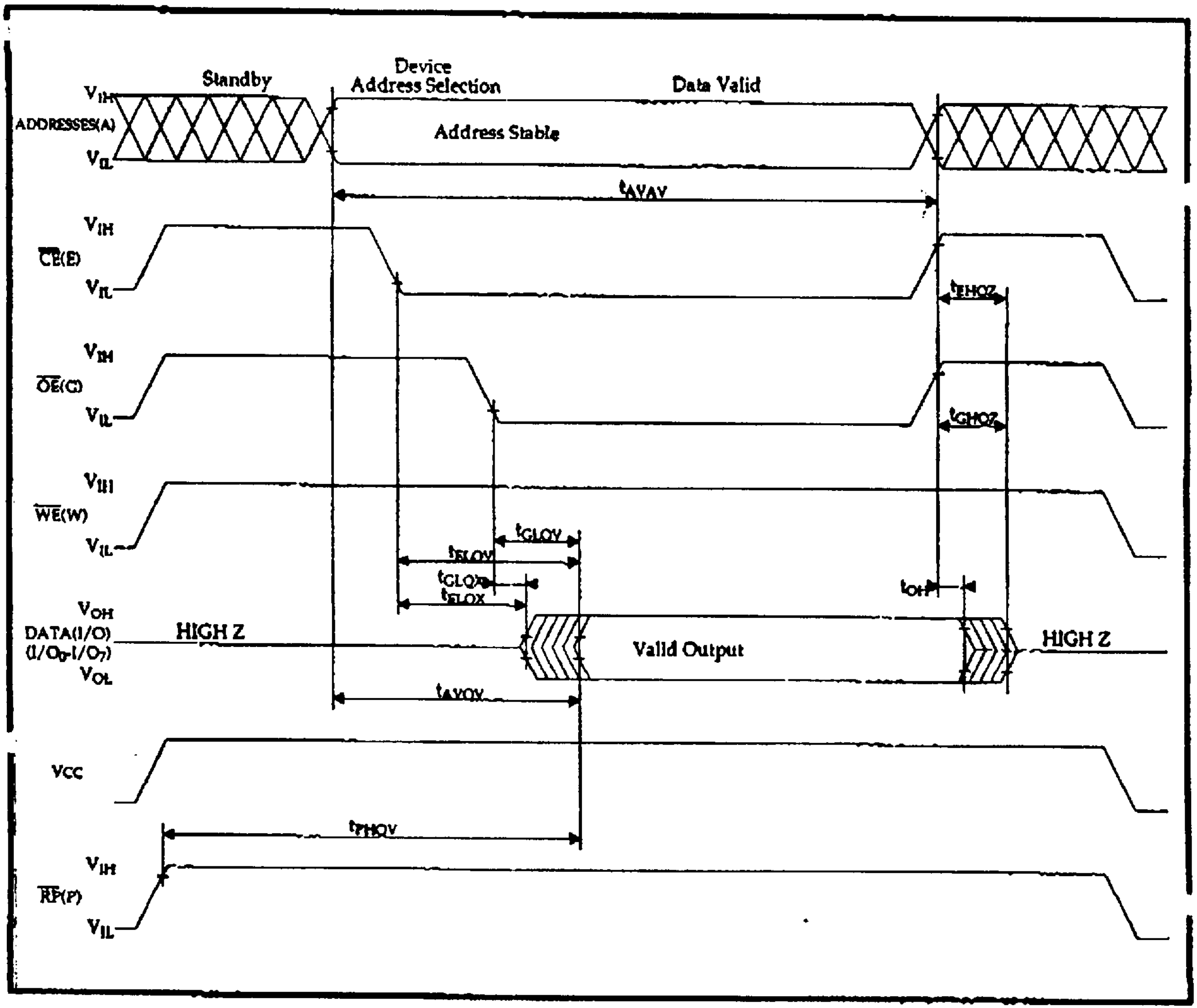


Figure 12. AC Waveform for Read Operations

6.2.4 AC CHARACTERISTICS - WRITE OPERATION(1)

V_{CC}=2.7V-3.6V, T_A=-25°C to +85°C

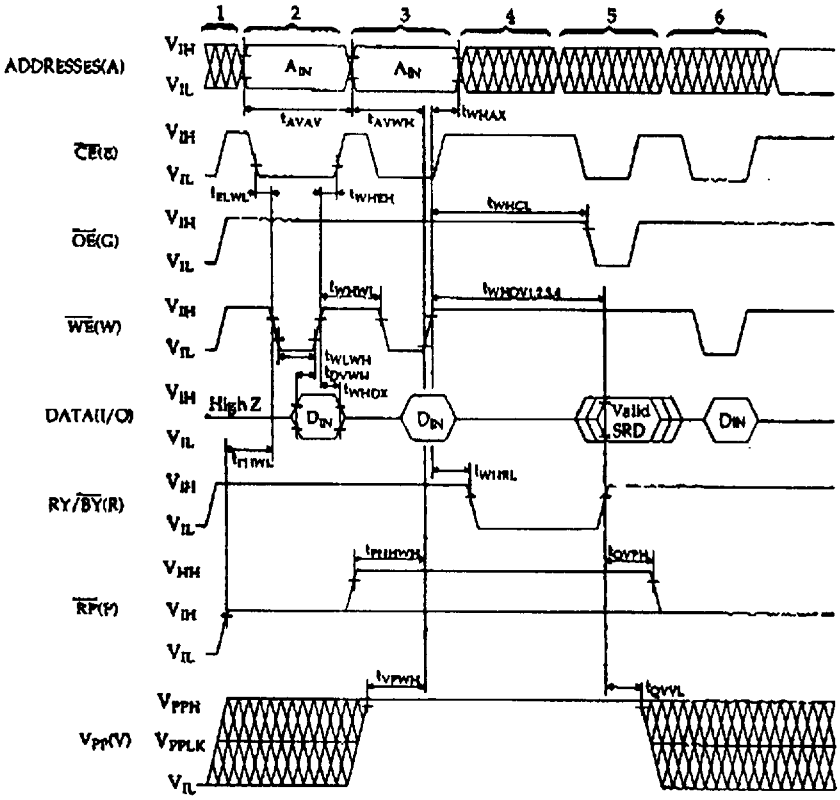
Sym	Parameter	Notes	Min	Max	Unit
t_{AVAV}	Write Cycle Time		150		ns
t_{PHWL}	$\overline{\text{RP}}$ High Recovery to $\overline{\text{WE}}$ Going Low	2	1		µs
t_{ELWL}	$\overline{\text{CE}}$ Setup to $\overline{\text{WE}}$ Going Low		10		ns
t_{WLWH}	$\overline{\text{WE}}$ Pulse Width		50		ns
t_{AVWH}	Address Setup to $\overline{\text{WE}}$ Going High	3	50		ns
t_{DVWH}	Data Setup to $\overline{\text{WE}}$ Going High	3	50		ns
t_{WHDX}	Data Hold from $\overline{\text{WE}}$ High		5		ns
t_{WHAX}	Address Hold from $\overline{\text{WE}}$ High		5		ns
t_{WHEH}	$\overline{\text{CE}}$ Hold from $\overline{\text{WE}}$ High		10		ns
t_{WHWL}	$\overline{\text{WE}}$ Pulse Width High		30		ns
t_{WHGL}	Write Recovery before Read		0		ns

V_{CC}=3.0V-3.6V, T_A=-25°C to +85°C

Sym	Parameter	Notes	Min	Max	Unit
t_{AVAV}	Write Cycle Time		120		ns
t_{PHWL}	$\overline{\text{RP}}$ High Recovery to $\overline{\text{WE}}$ Going Low	2	1		µs
t_{ELWL}	$\overline{\text{CE}}$ Setup to $\overline{\text{WE}}$ Going Low		10		ns
t_{WLWH}	$\overline{\text{WE}}$ Pulse Width		50		ns
t_{PHHWH}	$\overline{\text{RP}}$ V_{HH} Setup to $\overline{\text{WE}}$ Going High	2	100		ns
t_{VPWH}	V_{PP} Setup to $\overline{\text{WE}}$ Going High	2	100		ns
t_{AVWH}	Address Setup to $\overline{\text{WE}}$ Going High	3	50		ns
t_{DVWH}	Data Setup to $\overline{\text{WE}}$ Going High	3	50		ns
t_{WHDX}	Data Hold from $\overline{\text{WE}}$ High		5		ns
t_{WHAX}	Address Hold from $\overline{\text{WE}}$ High		5		ns
t_{WHEH}	$\overline{\text{CE}}$ Hold from $\overline{\text{WE}}$ High		10		ns
[illegible]	$\overline{\text{WE}}$ Pulse Width High		30		ns
t_{WHRL}	$\overline{\text{WE}}$ High to RY/$\overline{\text{BY}}$ Going Low			100	ns
t_{WHGL}	Write Recovery before Read		0		ns
t_{QVVL}	V_{PP} Hold from Valid SRD, RY/$\overline{\text{BY}}$ High	2,4	0		ns
t_{QVPH}	$\overline{\text{RP}}$ V_{HH} Hold from Valid SRD, RY/$\overline{\text{BY}}$ High	2,4	0		ns

NOTES:

1. Read timing characteristics during block erase, byte write and lock-bit configuration operations are the same as during read-only operations. Refer to AC Characteristics for read-only operations.
2. Sampled, not 100% tested.
3. Refer to Table 4 for valid A_{IN} and D_{IN} for block erase, byte write, or lock-bit configuration.
4. V_{PP} should be held at V_{PPH} (and if necessary should be held at V_{HH}) until determination of block erase, byte write, or lock-bit configuration success (SR.1/3/4/5=0).



NOTES:
1. V_{CC} power-up and standby.
2. Write block erase or byte write setup.
3. Write block erase confirm or valid address and data.
4. Automated erase or program delay.
5. Read status register data.
6. Write Read Array command.

Figure 13. AC Waveform for $\overline{WE}$-Controlled Write Operations

6.2.5 ALTERNATIVE $\overline{CE}$-CONTROLLED WRITES[1]

V_{CC}=2.7V-3.6V, T_A=-25°C to +85°C

Sym	Parameter	Notes	Min	Max	Unit
t_{AVAV}	Write Cycle Time		150		ns
t_{PHEL}	$\overline{RP}$ High Recovery to $\overline{CE}$ Going Low	2	1		µs
t_{WLEL}	$\overline{WE}$ Setup to $\overline{CE}$ Going Low		0		ns
t_{ELEH}	$\overline{CE}$ Pulse Width		70		ns
t_{AVEH}	Address Setup to $\overline{CE}$ Going High	3	50		ns
t_{DVEH}	Data Setup to $\overline{CE}$ Going High	3	50		ns
t_{EHDX}	Data Hold from $\overline{CE}$ High		5		ns
t_{EHAX}	Address Hold from $\overline{CE}$ High		5		ns
t_{EHWH}	$\overline{WE}$ Hold from $\overline{CE}$ High		0		ns
t_{EHEL}	$\overline{CE}$ Pulse Width High		25		ns
t_{EHGL}	Write Recovery before Read		0		ns

NOTE:

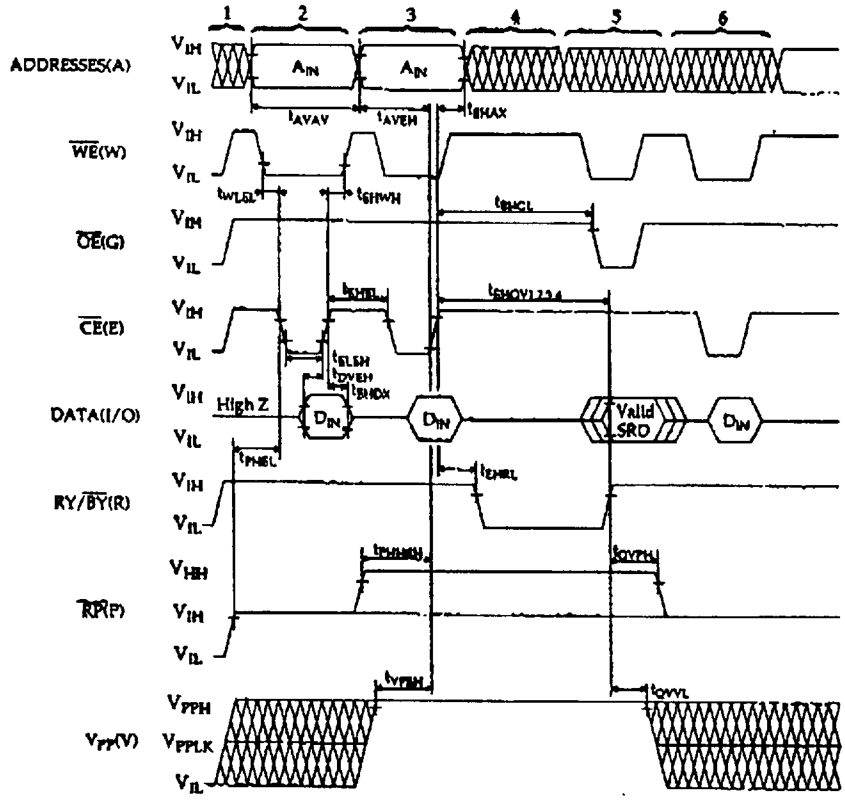
See 5.0V V_{CC} Alternative $\overline{CE}$-Controlled Writes for notes 1 through 5.

V_{CC}=3.0V-3.6V, T_A=-25°C to +85°C

Sym	Parameter	Notes	Min	Max	Unit
t_{AVAV}	Write Cycle Time		120		ns
t_{PHEL}	$\overline{WE}$ High Recovery to $\overline{CE}$ Going Low	2	1		µs
t_{WLEL}	$\overline{WE}$Setup to $\overline{CE}$ Going Low		0		ns
t_{ELEH}	$\overline{CE}$ Pulse Width		70		ns
t_{PHHEH}	$\overline{WE}$ V_{HH} Setup to $\overline{CE}$ Going High	2	100		ns
t_{VPEH}	V_{PP} Setup to $\overline{CE}$ Going High	2	100		ns
t_{AVEH}	Address Setup to $\overline{CE}$ Going High	3	50		ns
t_{DVEH}	Data Setup to $\overline{CE}$ Going High	3	50		ns
t_{EHDX}	Data Hold from $\overline{CE}$ High		5		ns
t_{EHAX}	Address Hold from $\overline{CE}$ High		5		ns
t_{EHWH}	$\overline{WE}$ Hold from $\overline{CE}$ High		0		ns
t_{EHEL}	$\overline{RP}$ Pulse Width High		25		ns
t_{EHRL}	$\overline{RP}$ High to RY/$\overline{BY}$Going Low			100	ns
t_{EHGL}	Write Recovery before Read		0		ns
t_{QVVL}	V_{PP} Hold from Valid SRD, RY/$\overline{BY}$ High	2,4	0		ns
t_{QVPH}	$\overline{WE}$ V_{HH} Hold from Valid SRD, RY/$\overline{BY}$High	2,4	0		ns

NOTES:

1. In systems where $\overline{CE}$ defines the write pulse width (within a longer $\overline{WE}$ timing waveform), all setup, hold, and inactive $\overline{WE}$ times should be measured relative to the $\overline{CE}$ waveform.
2. Sampled, not 100% tested.
3. Refer to Table 4 for valid A_{IN} and D_{IN} for block erase, byte write, or lock-bit configuration.
4. V_{PP} should be held at V_{PPH} (and if necessary $\overline{RP}$ should be held at V_{HH}) until determination of block erase, byte write, or lock-bit configuration success (SR.1/3/4/5=0).



NOTES:
1. V_{CC} power-up and standby.
2. Write block erase or byte write setup.
3. Write block erase confirm or valid address and data.
4. Automated erase or program delay.
5. Read status register data.
6. Write Read Array command.

Figure 14. Alternate AC Waveform for $\overline{CE}$-Controlled Write Operations

6.2.6 RESET OPERATIONS

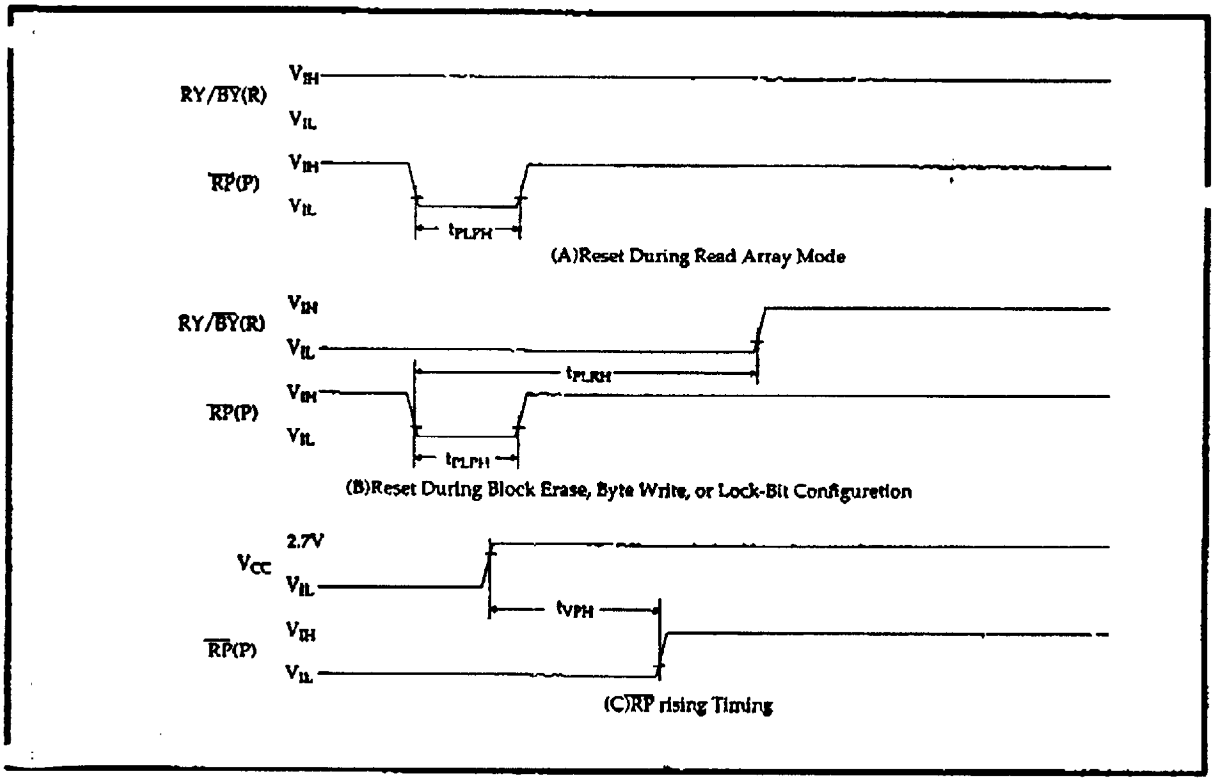


Figure 15. AC Waveform for Reset Operation

Reset AC Specifications(1)

Sym	Parameter	Notes	Min	Max	Unit
t_{PLPH}	$\overline{RP}$ Pulse Low Time (If $\overline{RP}$ is tied to V_{CC}, this specification is not applicable)		100		ns
t_{PLRH}	$\overline{RP}$ Low to Reset during Block Erase, Byte Write or Lock-Bit Configuration	1,2		20	μs
t_{VPH}	V_{CC} 2.7V to $\overline{RP}$ High	3	100		ns

NOTES:

1. If $\overline{RP}$ is asserted while a block erase, byte write, or lock-bit configuration operation is not executing, the reset will complete within 100ns.
2. A reset time, t_{PHQV}, is required from the latter of RY/$\overline{BY}$ or $\overline{RP}$ going high until outputs are valid.
3. When the device power-up, holding $\overline{RP}$ low minimum 100ns is required after V_{CC} has been in predefined range and also has been in stable there.

6.2.7 BLOCK ERASE, BYTE WRITE AND LOCK-BIT CONFIGURATION PERFORMANCE(3)

V_{CC}=3.0V-3.6V, T_A=-25°C to +85°C

Sym	Parameter	Notes	V_{PP}=3.0V-3.6V		Unit
			Typ(1)	Max	
t_{WHQV1} t_{EHQV1}	Byte Write Time	2	19	300	µs
	Block Write Time	2	1.2	4	sec
t_{EHQV2}	Block Erase Time	2	0.8	6	sec
t_{WHQV3} t_{EHQV3}	Set Lock-Bit Time	2	21		µs
t_{WHQV4} t_{EHQV4}	Clear Block Lock-Bits Time	2	1.8		sec
t_{WHRH1} t_{EHRH1}	Byte Write Suspend Latency Time to Read		7.1	10	µs
t_{WHRH2} t_{EHRH2}	Erase Suspend Latency Time to Read		15.2	21.1	µs

NOTES:

1. Typical values measured at T_A=+25°C and nominal voltages. Assumes corresponding lock-bits are not set. Subject to change based on device characterization.
2. Excludes system-level overhead.
3. Sampled but not 100% tested.

Part 3 SRAM
CONTENTS

1.Description

The LRS1310A is a 2M bit static RAM organized as 262,144×8 bit which provides low-power standby mode.

It is fabricated using silicon-gate CMOS process technology.

Features

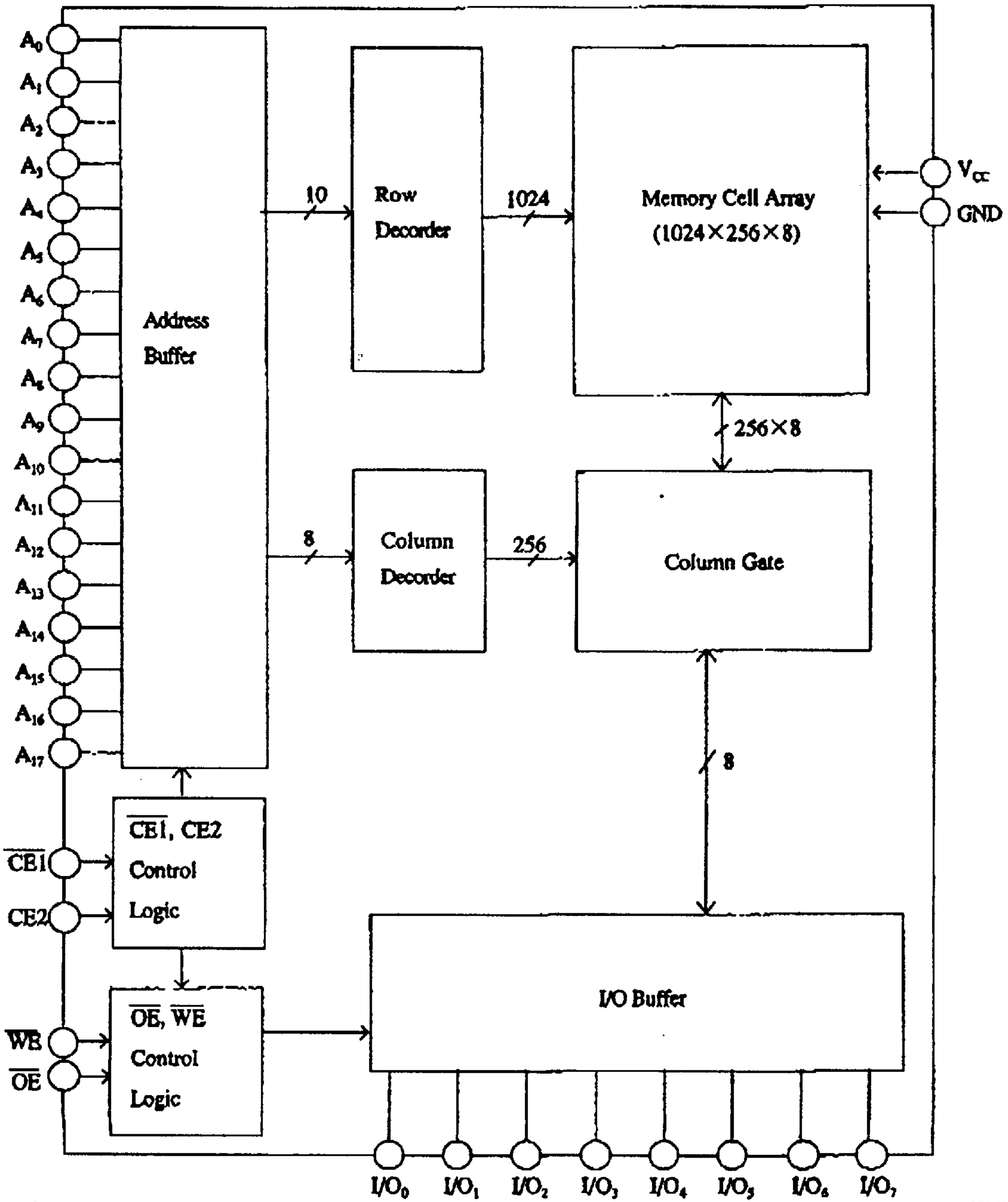
Access Time	85 ns(Max.)
Operating current	40 mA(Max.) 25 mA(Max. t_{CYCLE}=200ns)
Standby current	45 µA(Max.)
Single power supply	2.7V to 3.6V
Operating temperature	-25℃ to +85℃
Fully static operation	
Three-state output	
Not designed or rated as radiation hardened	
P-type bulk silicon	

2.Truth Table ($\overline{CE1}$, CE2, $\overline{OE}$ and $\overline{WE}$ mean S-$\overline{CE1}$, S-CE2, S-$\overline{OE}$ and S-$\overline{WE}$ respectively.)

$\overline{CE1}$	CE2	$\overline{WE}$	$\overline{OE}$	Mode	I/O_0 to I/O_7	Supply current
H	X	X	X	Standby	High impedance	Standby(I_{SB})
X	L	X	X	Standby	High impedance	Standby(I_{SB})
L	H	L	X	Write	Data input	Active(I_{CC})
L	H	H	L	Read	Data output	Active(I_{CC})
L	H	H	H	Output disable	High impedance	Active(I_{CC})

(X=Don't Care, L=Low, H=High)

3.Block Diagram (V_{CC} means S-V_{CC})



4.Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage(*1)	V_{CC}	-0.2 to 4.6	V
Input voltage(*1)	V_{IN}	-0.3 (*2) to V_{CC}+0.3	V
Operating temperature	T_{opr}	-25 to +85	℃
Storage temperature	T_{stg}	-65 to +125	℃

Notes

*1. The maximum applicable voltage on any pin with respect to GND.

*2. -3.0V undershoot is allowed to the pulse width less than 50ns.

5.Recommended DC Operating Conditions

(T_a= -25℃ to +85℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	2.7	3.0	3.6	V
Input voltage	V_{IH}	2.0		V_{CC}+0.3	V
	V_{IL}	-0.3 (*3)		0.8	V

Note

*3.-3.0V undershoot is allowed to the pulse width less than 50ns.

6.DC Electrical Characteristics

(T_a = -25℃ to +85℃, V_{CC}=2.7V to 3.6V)

Parameter	Symbol	Conditions		Min.	Typ. (*4)	Max.	Unit
Input leakage current	I_{LI}	V_{IN}=0V to V_{CC}		-1.0		1.0	μA
Output leakage current	I_{LO}	$\overline{CE1}$=V_{IH} or CE2=V_{IL} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} $V_{I/O}$=0V to V_{CC}		-1.0		1.0	μA
Operating supply current	I_{CC1}	$\overline{CE1}$=V_{IL}, CE2=V_{IH} V_{IN}=V_{IL} or V_{IH}	t_{CYCLE}=Min $I_{I/O}$=0mA			40	mA
	I_{CC2}	$\overline{CE1}$≦0.2V, CE2≧V_{CC}-0.2V V_{IN}=0.2V or V_{CC}-0.2V	t_{CYCLE}=200ns $I_{I/O}$=0mA			25	mA
Standby current	I_{SB}	$\overline{CE1}$, CE2≧V_{CC}-0.2V or CE2≦0.2V			0.6	45	μA
	I_{SB1}	$\overline{CE1}$, CE2=V_{IH} or CE2=V_{IL}				3.0	mA
Output voltage	V_{OL}	I_{OL}=2.0mA				0.4	V
	V_{OH}	I_{OH}=-1.0mA		2.4			V

Note

*4. T_a=25℃, V_{CC}=3.0V

7. AC Electrical Characteristics

AC Test Conditions

Input pulse level	0.6V to 2.2V
Input rise and fall time	5ns
Input and Output timing Ref. level	1.5V
Output load	1TTL+C_L(30pF) (*5)

Note

*5.Including scope and jig capacitance.

Read cycle

(T_a= -25℃ to +85℃ , V_{CC}= 2.7V to 3.6V)

Parameter	Symbol	Min.	Max.	Unit	
Read cycle time	t_{RC}	85		ns	
Address access time	t_{AA}		85	ns	
Chip enable access time	t_{ACE}		85	ns	
Output enable to output valid	t_{OE}		45	ns	
Output hold from address change	t_{OH}	10		ns	
$\overline{CE1}$, CE2 Low to output active	t_{LZ}	10		ns	*6
$\overline{OE}$ Low to output active	t_{OLZ}	5		ns	*6
$\overline{CE1}$, CE2 High to output in High impedance	t_{HZ}	0	30	ns	*6
$\overline{OE}$ High to output in High impedance	t_{OHZ}	0	30	ns	*6

Write cycle

(T_a= -25℃ to +85℃ , V_{CC}= 2.7V to 3.6V)

Parameter	Symbol	Min.	Max.	Unit	
Write cycle time	t_{WC}	85		ns	
Chip enable to end of write	t_{CW}	75		ns	
Address valid to end of write	t_{AW}	75		ns	
Address setup time	t_{AS}	0		ns	
Write pulse width	t_{WP}	65		ns	
Write recovery time	t_{WR}	0		ns	
Input data setup time	t_{DW}	35		ns	
Input data hold time	t_{DH}	0		ns	
$\overline{WE}$ High to output active	t_{OW}	5		ns	*6
$\overline{WE}$ Low to output in High impedance	t_{WZ}	0	30	ns	*6
$\overline{OE}$ High to output in High impedance	t_{OHZ}	0	30	ns	*6

Note

*6. Active output to High impedance and High impedance to output active tests specified for a ±200mV transition from steady state levels into the test load.

8.Data Retention Characteristics

(T_a= -25℃ to +85℃)

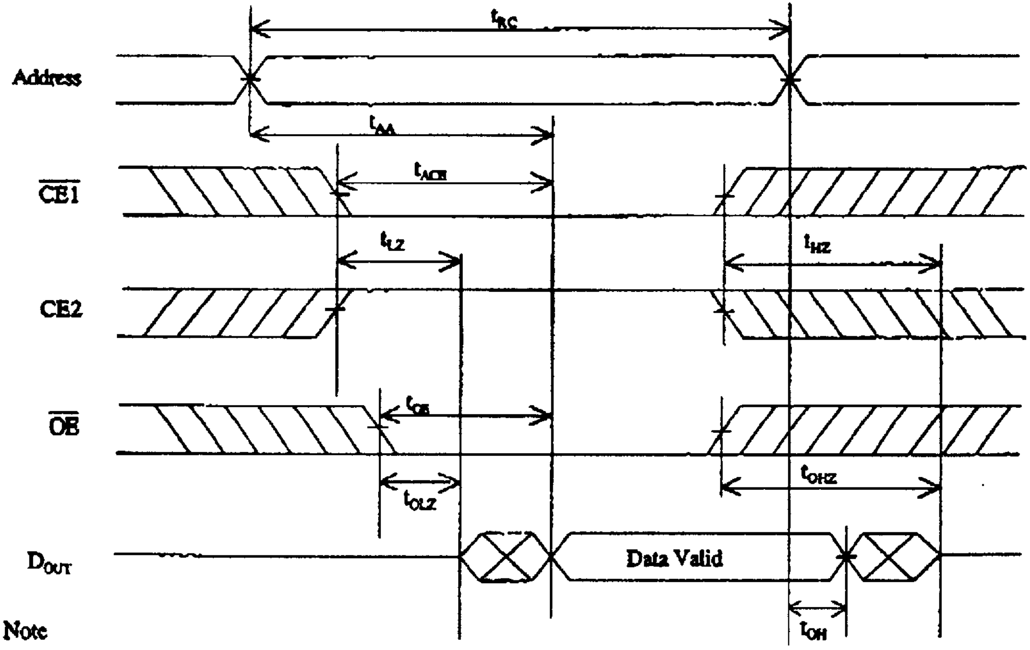
Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Data Retention supply voltage	V_{CCDR}	CE2≦0.2V or $\overline{CE1}$≧V_{CCDR}-0.2V (*7)		2.0		3.6	V
Data Retention supply current	I_{CCDR}	V_{CCDR}=3V $\overline{CE1}$, CE2≧V_{CCDR}-0.2V or CE2≦0.2V	T_a=25℃		0.6	1.0	µA
						35	µA
Chip enable setup time	t_{CDR}			0			ms
Chip enable hold time	t_R			5			ms

Note:

*7. CE2≧V_{CCDR}-0.2V or CE2≦0.2V.

9.Timing Chart

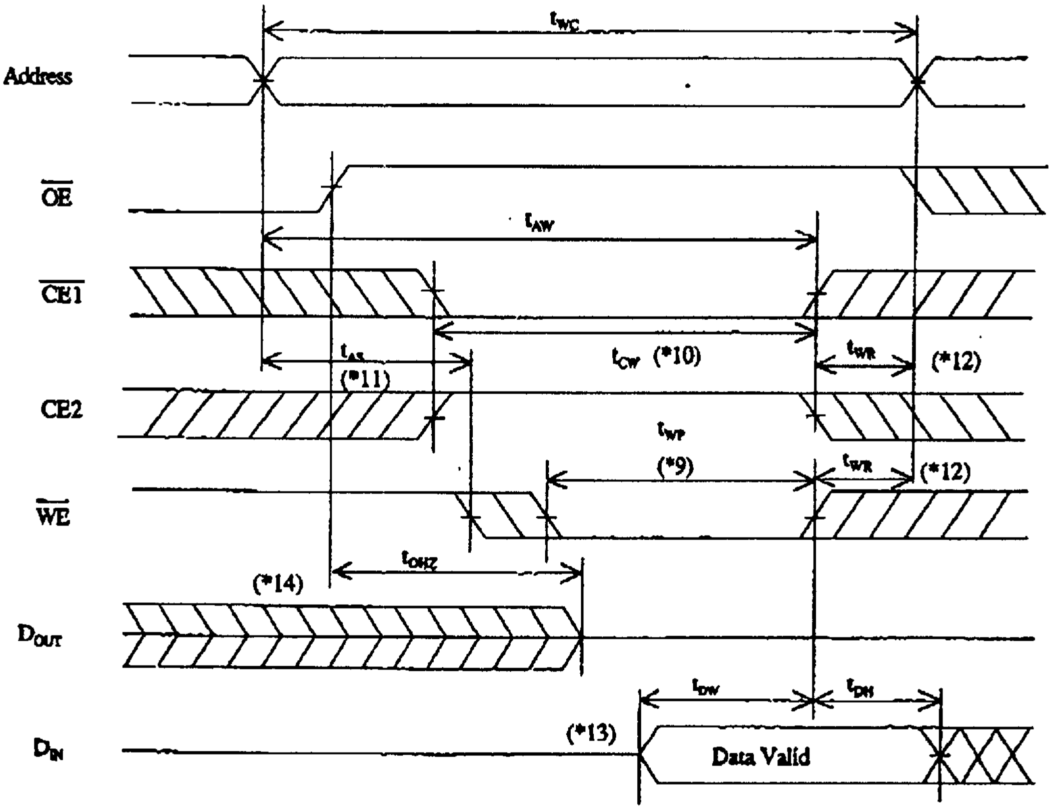
Read cycle timing chart (*8)



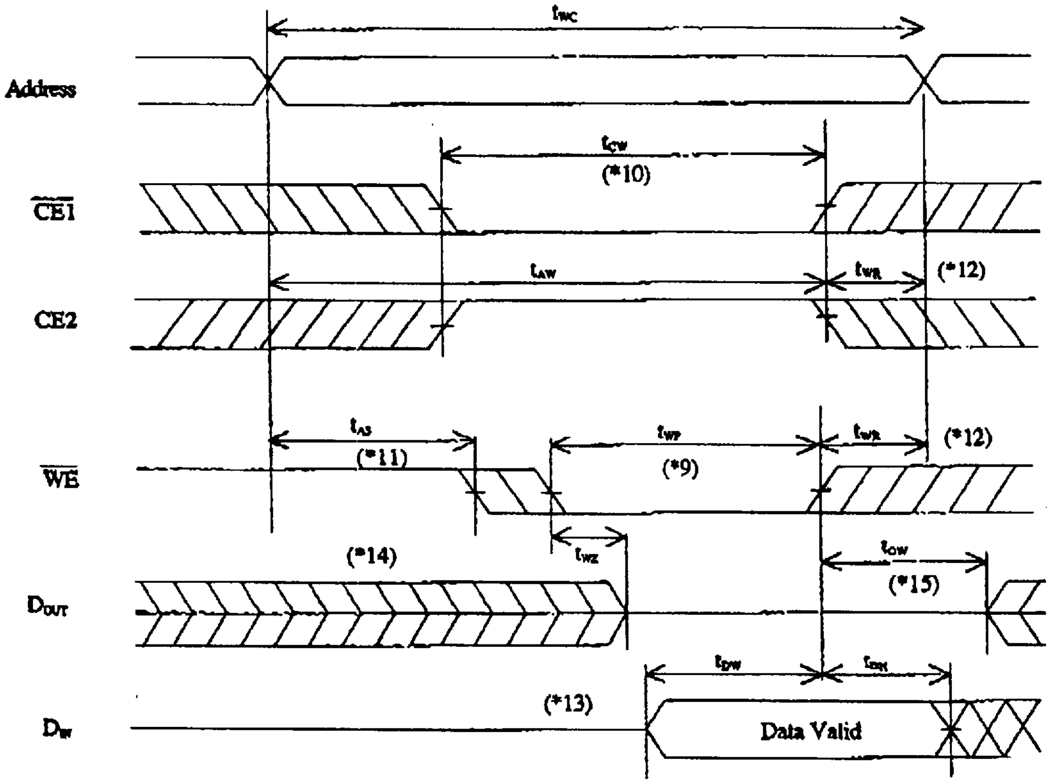
Note

*8. $\overline{WE}$ is high for Read cycle.

Write cycle timing chart ($\overline{OE}$ Controlled)



Write cycle timing chart ($\overline{OE}$ Low fixed)



Note)

* 9. A write occurs during the overlap of a low $\overline{CE1}$, a high CE2 and a low $\overline{WE}$.
A write begins at the latest transition among $\overline{CE1}$ going low, CE2 going high and $\overline{WE}$ going low.
A write ends at the earliest transition among $\overline{CE1}$ going high, CE2 going low and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.

* 10. t_{CW} is measured from the later of $\overline{CE1}$ going low or CE2 going high to the end of write.

* 11. t_{AS} is measured from the address valid to the beginning of write.

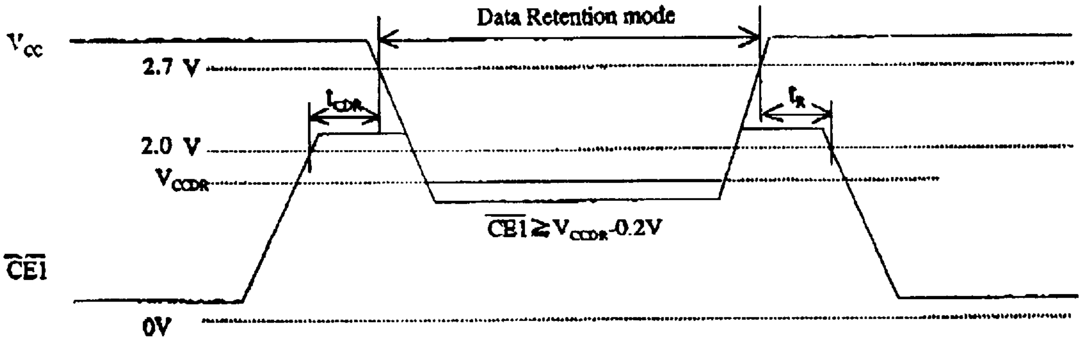
* 12. t_{WR} is measured from the end of write to the address change. t_{WR1} applies in case a write ends at $\overline{CE1}$ or $\overline{WE}$ going high. t_{WR2} applies in case a write ends at CE2 going low.

* 13. During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.

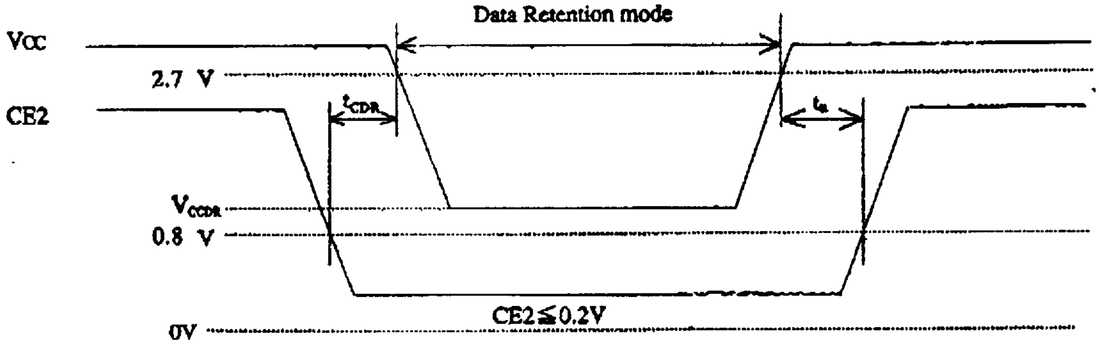
* 14. If $\overline{CE1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.

* 15. If $\overline{CE1}$ goes high simultaneously with $\overline{WE}$ going high or before $\overline{WE}$ going high, the outputs remain in high impedance state.

Data Retention timing chart ($\overline{\text{CE1}}$ Control) (*16)



(CE2 Control)



Note) * 16. To control the data retention mode at $\overline{\text{CE1}}$, fix the input level of CE2 between V_{CCDR} and V_{CCDR}-0.2V or 0V and 0.2V during the data retention mode.

Flash Memory Data Protection

Noises having a level exceeding the limit specified in the specification may be generated under specific operating conditions on some systems.
Such noises, when induced onto $\overline{\text{WE}}$ signal or power supply may be interpreted as false commands, causing undesired memory updating.
To protect the data stored in the flash memory against unwanted overwriteing, systems operating with the flash memory should have the following write protect designs, as appropriate:

1) Protecting data in specific block
When a lock bit is set,the corresponding block is protected against overwriting.By using the feature,the flash memory space can be divided into the program section and data section.The master lock bit can be used to restrict block bit setting
By controlling $\overline{\text{RP}}$,desired blocks can be locked/unlocked through the software.
For further information on setting/resetting block bit and controlling of $\overline{\text{RP}}$,refer to the specification.(See chapter 4.9.4.10 and 6.2.7.)

2) Data protection through Vpp
When the level of Vpp is lower than VPPLK(lockout voltage), write operation on the flash memory is disabled. All blocks are locked and the data in the blocks are completely write protected.
For the lockout voltage, refer to the specifation.(See chapter 4.9 and 6.2.3.)

Data protection during voltage transion
1) Data protection thorough $\overline{\text{RP}}$
When the $\overline{\text{RP}}$ is kept low during power up and power down sequence, write operation on the flash memory is disabled, write protecting all blocks.
For the details of $\overline{\text{RP}}$ control, refer to the specification.(See chapter 5.6 and 6.2.7.)