

# M5M4V64S30ATP-8A,-8L,-8, -10L, -10

64M (4-BANK x 2097152-WORD x 8-BIT) Synchronous DRAM

Some of contents are subject to change without notice.

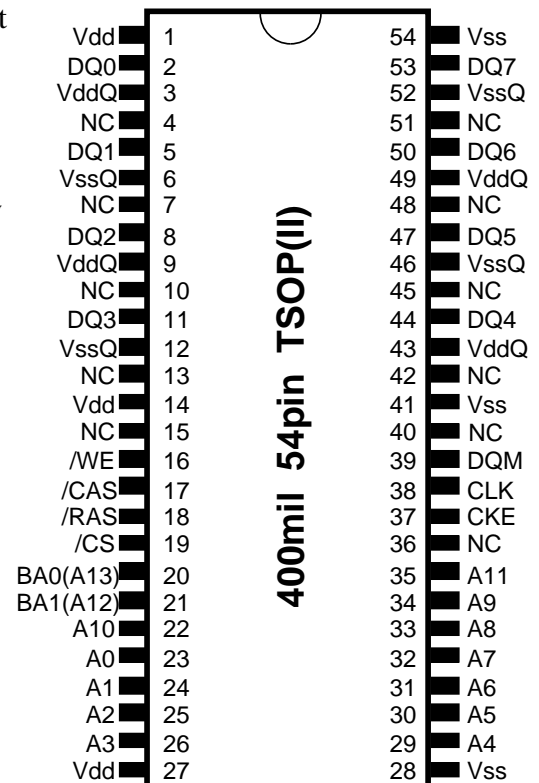
## DESCRIPTION

The M5M4V64S30ATP is a 4-bank x 2097152-word x 8-bit Synchronous DRAM, with LVTTTL interface. All inputs and outputs are referenced to the rising edge of CLK. The M5M4V64S30ATP achieves very high speed data rate up to 125MHz, and is suitable for main memory or graphic memory in computer systems.

## FEATURES

- Single 3.3v±0.3v power supply
- Clock frequency 125MHz /100MHz
- Fully synchronous operation referenced to clock rising edge
- 4 bank operation controlled by BA0, BA1 (Bank Address)
- /CAS latency- 2/3 (programmable)
- Burst length- 1/2/4/8/Full Page (programmable)
- Burst type- sequential / interleave (programmable)
- Column access - random
- Burst Write / Single Write (programmable)
- Auto precharge / All bank precharge controlled by A10
- Auto refresh and Self refresh
- 4096 refresh cycles /64ms
- Column address A0-A8
- LVTTTL Interface
- 400-mil, 54-pin Thin Small Outline Package (TSOP II) with 0.8mm lead pitch

## PIN CONFIGURATION (TOP VIEW)

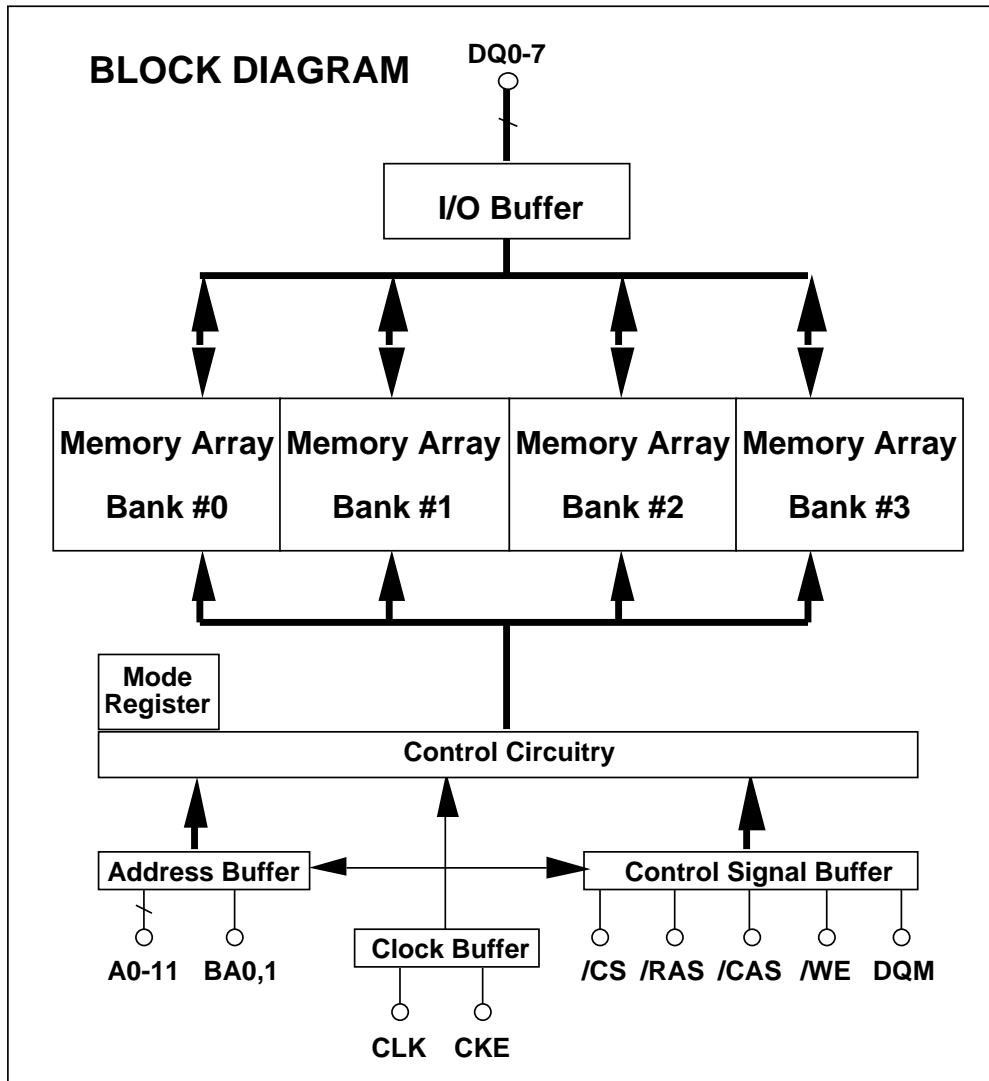


- CLK** : Master Clock
- CKE** : Clock Enable
- /CS** : Chip Select
- /RAS** : Row Address Strobe
- /CAS** : Column Address Strobe
- /WE** : Write Enable
- DQ0-7** : Data I/O
- DQM** : Output Disable/ Write Mask
- A0-11** : Address Input
- BA0,1** : Bank Address
- Vdd** : Power Supply
- VddQ** : Power Supply for Output
- Vss** : Ground
- VssQ** : Ground for Output

	Max. Frequency	CLK Access Time
M5M4V64S30ATP-8A	125MHz	6ns
M5M4V64S30ATP-8	100MHz	6ns
M5M4V64S30ATP-10	100MHz	8ns

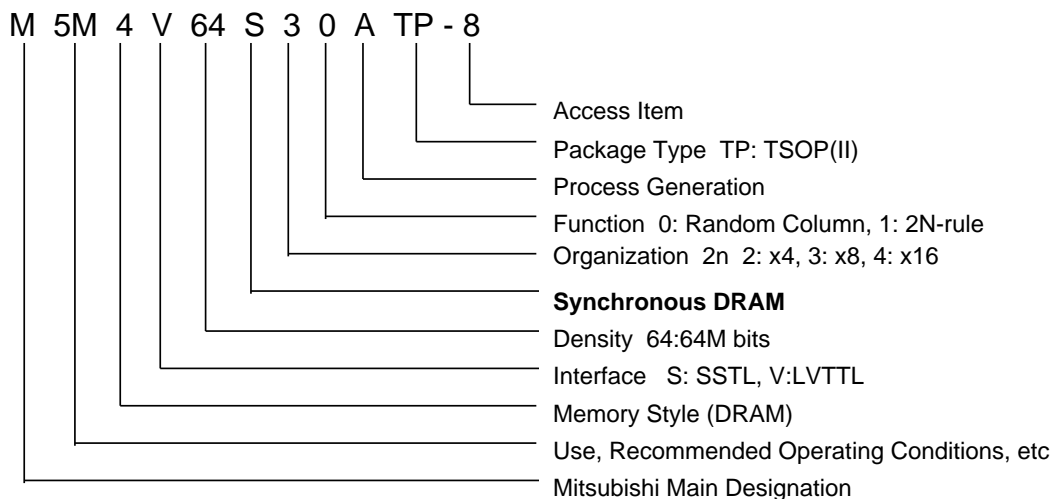
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## Type Designation Code

This rule is applied to only Synchronous DRAM family.



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## PIN FUNCTION

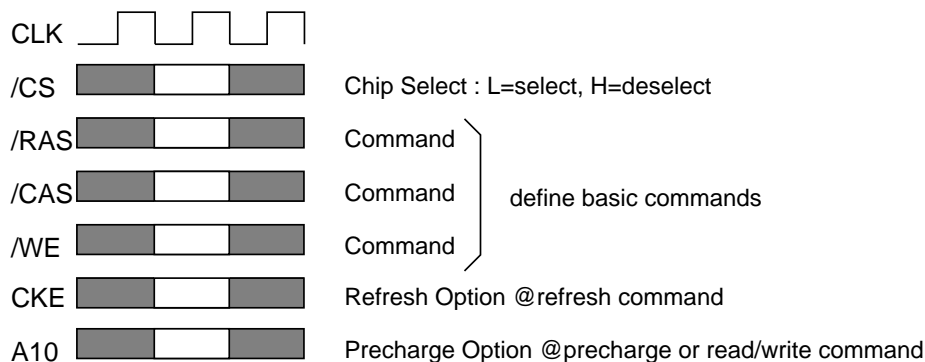
CLK	Input	Master Clock: All other inputs are referenced to the rising edge of CLK.
CKE	Input	Clock Enable: CKE controls internal clock. When CKE is low, internal clock for the following cycle is ceased. CKE is also used to select auto / self refresh. After self refresh mode is started, CKE becomes asynchronous input. Self refresh is maintained as long as CKE is low.
/CS	Input	Chip Select: When /CS is high, any command means No Operation.
/RAS, /CAS, /WE	Input	Combination of /RAS, /CAS, /WE defines basic commands.
A0-11	Input	A0-11 specify the Row / Column Address in conjunction with BA0,1. The Row Address is specified by A0-11. The Column Address is specified by A0-8 . A10 is also used to indicate precharge option. When A10 is high at a read / write command, an auto precharge is performed. When A10 is high at a precharge command, all banks are precharged.
BA0,1	Input	Bank Address: BA0,1 specifies one of four banks to which a command is applied. BA0,1 must be set with ACT, PRE, READ, WRITE commands.
DQ0-7	Input / Output	Data In and Data out are referenced to the rising edge of CLK.
DQM	Input	Din Mask / Output Disable: When DQM is high in burst write, Din for the current cycle is masked. When DQM is high in burst read, Dout is disabled at the next but one cycle.
Vdd, Vss	Power Supply	Power Supply for the memory array and peripheral circuitry.
VddQ, VssQ	Power Supply	VddQ and VssQ are supplied to the Output Buffers only.

## BASIC FUNCTIONS

The M5M4V64S30ATP provides basic functions, bank (row) activate, burst read / write, bank (row) precharge, and auto / self refresh.

Each command is defined by control signals of /RAS, /CAS and /WE at CLK rising edge. In addition to 3 signals, /CS, CKE and A10 are used as chip select, refresh option, and precharge option, respectively.

To know the detailed definition of commands, please see the command truth table.



### Activate (ACT) [/RAS =L, /CAS =/WE =H]

ACT command activates a row in an idle bank indicated by BA.

### Read (READ) [/RAS =H, /CAS =L, /WE =H]

READ command starts burst read from the active bank indicated by BA. First output data appears after /CAS latency. When A10 =H at this command, the bank is deactivated after the burst read (auto-precharge, **READA**).

### Write (WRITE) [/RAS =H, /CAS =/WE =L]

WRITE command starts burst write to the active bank indicated by BA. Total data length to be written is set by burst length. When A10 =H at this command, the bank is deactivated after the burst write (auto-precharge, **WRITEA**).

### Precharge (PRE) [/RAS =L, /CAS =H, /WE =L]

PRE command deactivates the active bank indicated by BA. This command also terminates burst read / write operation. When A10 =H at this command, both banks are deactivated (precharge all, **PREA**).

### Auto-Refresh (REFA) [/RAS =/CAS =L, /WE =CKE =H]

REFA command starts auto-refresh cycle. Refresh address including bank address are generated internally. After this command, the banks are precharged automatically.

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**COMMAND TRUTH TABLE**

COMMAND	MNEMONIC	CKE <sub>n-1</sub>	CKE <sub>n</sub>	/CS	/RAS	/CAS	/WE	BA0,1	A11	A10	A0-9
Deselect	DESEL	H	X	H	X	X	X	X	X	X	X
No Operation	NOP	H	X	L	H	H	H	X	X	X	X
Row Address Entry & Bank Activate	ACT	H	X	L	L	H	H	V	V	V	V
Single Bank Precharge	PRE	H	X	L	L	H	L	V	X	L	X
Precharge All Banks	PREA	H	X	L	L	H	L	X	X	H	X
Column Address Entry & Write	WRITE	H	X	L	H	L	L	V	X	L	V
Column Address Entry & Write with Auto-Precharge	WRITEA	H	X	L	H	L	L	V	X	H	V
Column Address Entry & Read	READ	H	X	L	H	L	H	V	X	L	V
Column Address Entry & Read with Auto-Precharge	READA	H	X	L	H	L	H	V	X	H	V
Auto-Refresh	REFA	H	H	L	L	L	H	X	X	X	X
Self-Refresh Entry	REFS	H	L	L	L	L	H	X	X	X	X
Self-Refresh Exit	REFSX	L	H	H	X	X	X	X	X	X	X
		L	H	L	H	H	H	X	X	X	X
Burst Terminate	TBST	H	X	L	H	H	L	X	X	X	X
Mode Register Set	MRS	H	X	L	L	L	L	L	L	L	V*1

H=High Level, L=Low Level, V=Valid, X=Don't Care, n=CLK cycle number

NOTE:

1. A7-A9 =0, A0-A6 =Mode Address

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**FUNCTION TRUTH TABLE**

Current State	/CS	/RAS	/CAS	/WE	Address	Command	Action
IDLE	H	X	X	X	X	DESEL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	BA	TBST	ILLEGAL*2
	L	H	L	X	BA, CA, A10	READ / WRITE	ILLEGAL*2
	L	L	H	H	BA, RA	ACT	Bank Active, Latch RA
	L	L	H	L	BA, A10	PRE / PREA	NOP*4
	L	L	L	H	X	REFA	Auto-Refresh*5
	L	L	L	L	Op-Code, Mode-Add	MRS	Mode Register Set*5
ROW ACTIVE	H	X	X	X	X	DESEL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	BA	TBST	NOP
	L	H	L	H	BA, CA, A10	READ / READA	Begin Read, Latch CA, Determine Auto-Precharge
	L	H	L	L	BA, CA, A10	WRITE / WRITEA	Begin Write, Latch CA, Determine Auto-Precharge
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL*2
	L	L	H	L	BA, A10	PRE / PREA	Precharge / Precharge All
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
READ	H	X	X	X	X	DESEL	NOP (Continue Burst to END)
	L	H	H	H	X	NOP	NOP (Continue Burst to END)
	L	H	H	L	BA	TBST	Terminate Burst
	L	H	L	H	BA, CA, A10	READ / READA	Terminate Burst, Latch CA, Begin New Read, Determine Auto-Precharge*3
	L	H	L	L	BA, CA, A10	WRITE / WRITEA	Terminate Burst, Latch CA, Begin Write, Determine Auto- Precharge*3
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL*2
	L	L	H	L	BA, A10	PRE / PREA	Terminate Burst, Precharge
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

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**FUNCTION TRUTH TABLE(continued)**

Current State	/CS	/RAS	/CAS	/WE	Address	Command	Action
WRITE	H	X	X	X	X	DESEL	NOP (Continue Burst to END)
	L	H	H	H	X	NOP	NOP (Continue Burst to END)
	L	H	H	L	BA	TBST	Terminate Burst
	L	H	L	H	BA, CA, A10	READ / READA	Terminate Burst, Latch CA, Begin Read, Determine Auto-Precharge*3
	L	H	L	L	BA, CA, A10	WRITE / WRITEA	Terminate Burst, Latch CA, Begin Write, Determine Auto-Precharge*3
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL*2
	L	L	H	L	BA, A10	PRE / PREA	Terminate Burst, Precharge
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
READ with AUTO PRECHARGE	H	X	X	X	X	DESEL	NOP (Continue Burst to END)
	L	H	H	H	X	NOP	NOP (Continue Burst to END)
	L	H	H	L	BA	TBST	ILLEGAL
	L	H	L	H	BA, CA, A10	READ / READA	ILLEGAL
	L	H	L	L	BA, CA, A10	WRITE / WRITEA	ILLEGAL
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL*2
	L	L	H	L	BA, A10	PRE / PREA	ILLEGAL*2
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
WRITE with AUTO PRECHARGE	H	X	X	X	X	DESEL	NOP (Continue Burst to END)
	L	H	H	H	X	NOP	NOP (Continue Burst to END)
	L	H	H	L	BA	TBST	ILLEGAL
	L	H	L	H	BA, CA, A10	READ / READA	ILLEGAL
	L	H	L	L	BA, CA, A10	WRITE / WRITEA	ILLEGAL
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL*2
	L	L	H	L	BA, A10	PRE / PREA	ILLEGAL*2
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

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**FUNCTION TRUTH TABLE(continued)**

Current State	/CS	/RAS	/CAS	/WE	Address	Command	Action
PRE - CHARGING	H	X	X	X	X	DESEL	NOP (Idle after tRP)
	L	H	H	H	X	NOP	NOP (Idle after tRP)
	L	H	H	L	BA	TBST	ILLEGAL*2
	L	H	L	X	BA, CA, A10	READ / WRITE	ILLEGAL*2
	L	L	H	H	BA, RA	ACT	ILLEGAL*2
	L	L	H	L	BA, A10	PRE / PREA	NOP*4 (Idle after tRP)
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
ROW ACTIVATING	H	X	X	X	X	DESEL	NOP (Row Active after tRCD)
	L	H	H	H	X	NOP	NOP (Row Active after tRCD)
	L	H	H	L	BA	TBST	ILLEGAL*2
	L	H	L	X	BA, CA, A10	READ / WRITE	ILLEGAL*2
	L	L	H	H	BA, RA	ACT	ILLEGAL*2
	L	L	H	L	BA, A10	PRE / PREA	ILLEGAL*2
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
WRITE RE- COVERING	H	X	X	X	X	DESEL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	BA	TBST	ILLEGAL*2
	L	H	L	X	BA, CA, A10	READ / WRITE	ILLEGAL*2
	L	L	H	H	BA, RA	ACT	ILLEGAL*2
	L	L	H	L	BA, A10	PRE / PREA	ILLEGAL*2
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL



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**64M (4-BANK x 2097152-WORD x 8-BIT) Synchronous DRAM**

**FUNCTION TRUTH TABLE(continued)**

Current State	/CS	/RAS	/CAS	/WE	Address	Command	Action
RE-FRESHING	H	X	X	X	X	DESEL	NOP (Idle after tRC)
	L	H	H	H	X	NOP	NOP (Idle after tRC)
	L	H	H	L	BA	TBST	ILLEGAL
	L	H	L	X	BA, CA, A10	READ / WRITE	ILLEGAL
	L	L	H	H	BA, RA	ACT	ILLEGAL
	L	L	H	L	BA, A10	PRE / PREA	ILLEGAL
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
MODE REGISTER SETTING	H	X	X	X	X	DESEL	NOP (Idle after tRSC)
	L	H	H	H	X	NOP	NOP (Idle after tRSC)
	L	H	H	L	BA	TBST	ILLEGAL
	L	H	L	X	BA, CA, A10	READ / WRITE	ILLEGAL
	L	L	H	H	BA, RA	ACT	ILLEGAL
	L	L	H	L	BA, A10	PRE / PREA	ILLEGAL
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

ABBREVIATIONS:

H=High Level, L=Low Level, X=Don't Care

BA=Bank Address, RA=Row Address, CA=Column Address, NOP=No OPERATION

NOTES:

1. All entries assume that CKE was High during the preceding clock cycle and the current clock cycle.
2. ILLEGAL to bank in specified state; function may be legal in the bank indicated by BA, depending on the state of that bank.
3. Must satisfy bus contention, bus turn around, write recovery requirements.
4. NOP to bank precharging or in idle state. May precharge bank indicated by BA.
5. ILLEGAL if any bank is not idle.

ILLEGAL = Device operation and/or data-integrity are not guaranteed.

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## FUNCTION TRUTH TABLE for CKE

Current State	CKE n-1	CKE n	/CS	/RAS	/CAS	/WE	Add	Action
SELF- REFRESH*1	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exit Self-Refresh (Idle after tRC)
	L	H	L	H	H	H	X	Exit Self-Refresh (Idle after tRC)
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP (Maintain Self-Refresh)
POWER DOWN	H	X	X	X	X	X	X	INVALID
	L	H	X	X	X	X	X	Exit Power Down to Idle
	L	L	X	X	X	X	X	NOP (Maintain Self-Refresh)
ALL BANKS IDLE*2	H	H	X	X	X	X	X	Refer to Function Truth Table
	H	L	L	L	L	H	X	Enter Self-Refresh
	H	L	H	X	X	X	X	Enter Power Down
	H	L	L	H	H	H	X	Enter Power Down
	H	L	L	H	H	L	X	ILLEGAL
	H	L	L	H	L	X	X	ILLEGAL
	H	L	L	L	X	X	X	ILLEGAL
	L	X	X	X	X	X	X	Refer to Current State =Power Down
ANY STATE other than listed above	H	H	X	X	X	X	X	Refer to Function Truth Table
	H	L	X	X	X	X	X	Begin CLK Suspend at Next Cycle*3
	L	H	X	X	X	X	X	Exit CLK Suspend at Next Cycle*3
	L	L	X	X	X	X	X	Maintain CLK Suspend

ABBREVIATIONS:

H=High Level, L=Low Level, X=Don't Care

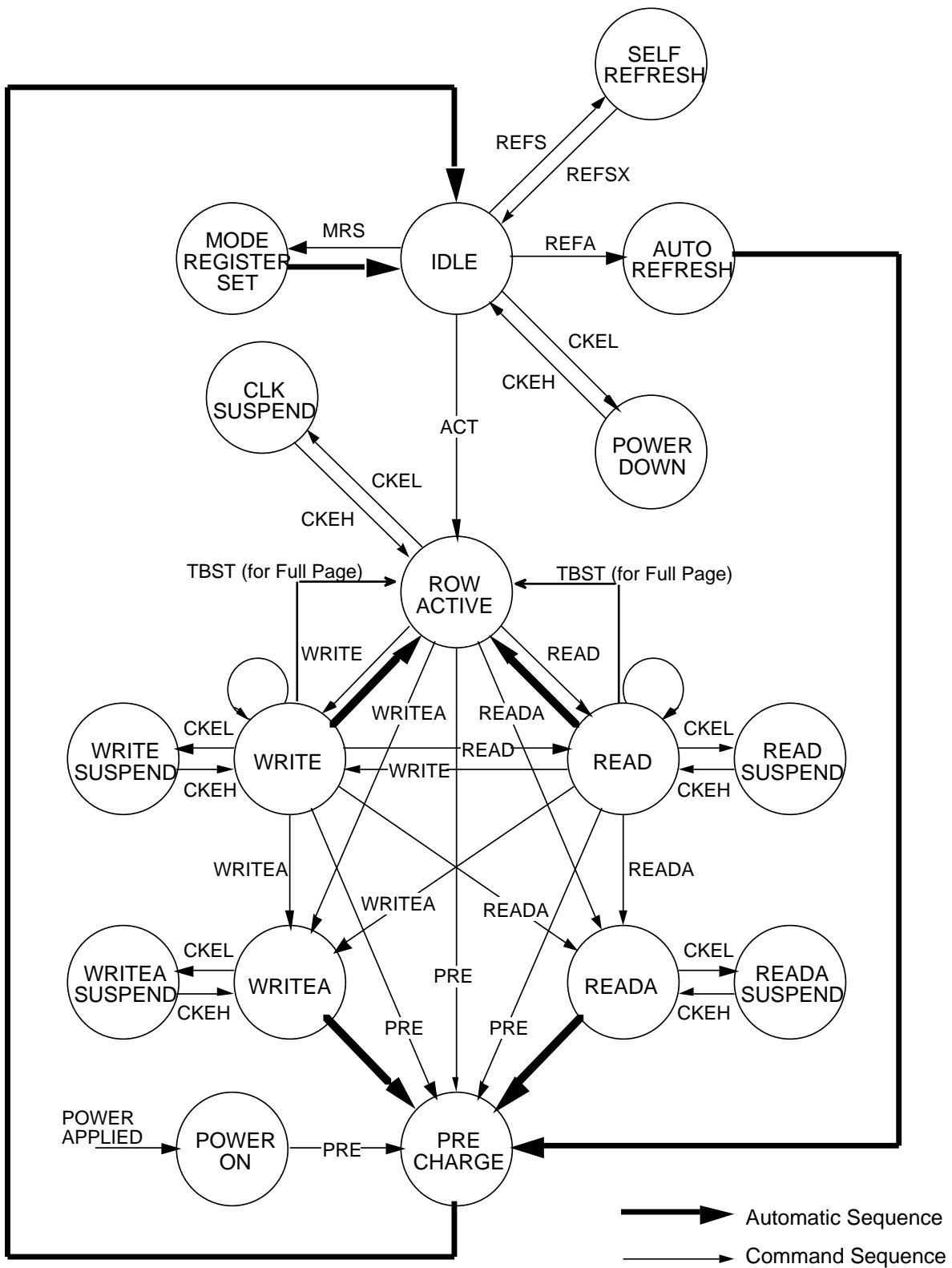
NOTES:

1. CKE Low to High transition will re-enable CLK and other inputs **asynchronously**. A minimum setup time must be satisfied before any command other than EXIT.
2. Power-Down and Self-Refresh can be entered only from the All Banks Idle State.
3. Must be legal command.

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## SIMPLIFIED STATE DIAGRAM



# M5M4V64S30ATP-8A,-8L,-8, -10L, -10

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## POWER ON SEQUENCE

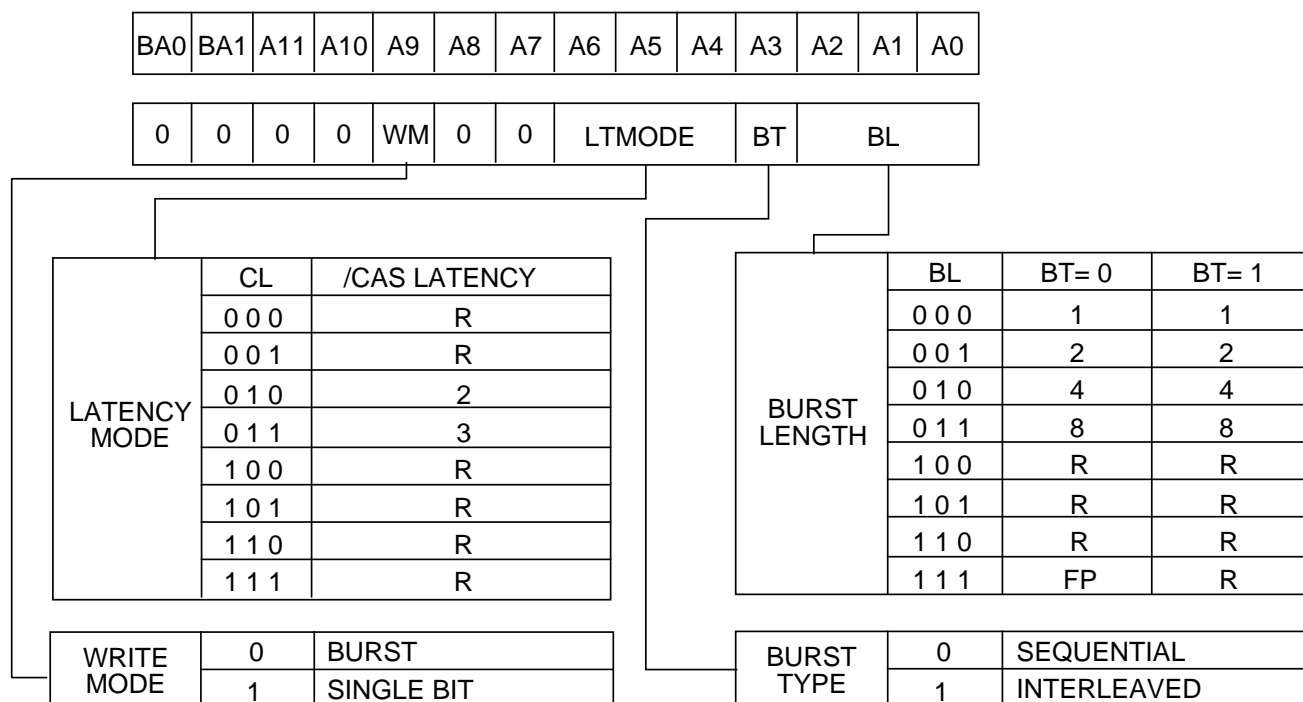
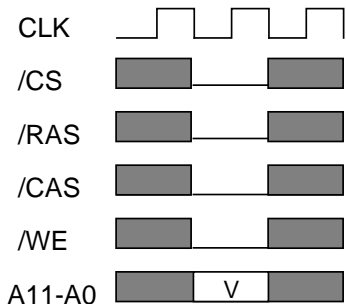
Before starting normal operation, the following power on sequence is necessary to prevent a SDRAM from damaged or malfunctioning.

1. Apply power and start clock. Attempt to maintain CKE high, DQM high and NOP condition at the inputs.
2. Maintain stable power, stable clock, and NOP input conditions for a minimum of 200µs.
3. Issue precharge commands for all banks. (PRE or PREA)
4. After all banks become idle state (after tRP), issue 8 or more auto-refresh commands.
5. Issue a mode register set command to initialize the mode register.

After these sequence, the SDRAM is idle state and ready for normal operation.

## MODE REGISTER

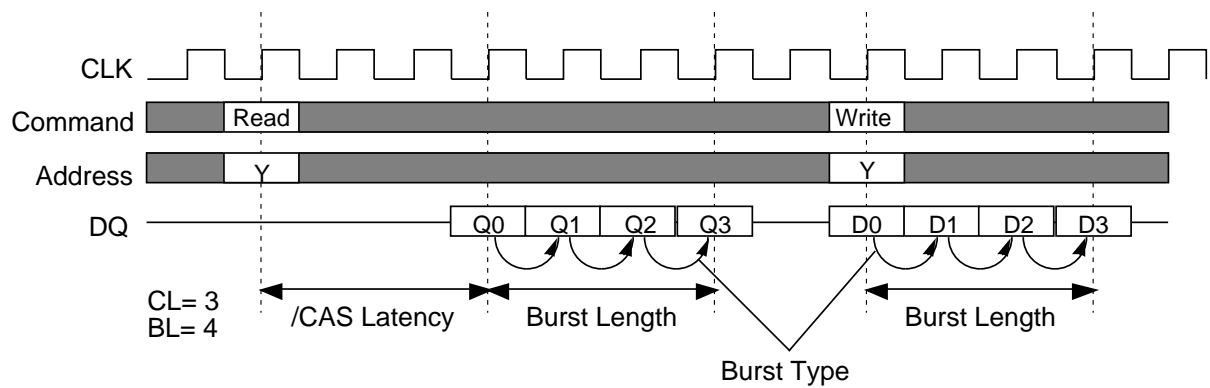
Burst Length, Burst Type and /CAS Latency can be programmed by setting the mode register (MRS). The mode register stores these data until the next MRS command, which may be issued when both banks are in idle state. After tRSC from a MRS command, the SDRAM is ready for new command.



R: Reserved for Future Use  
FP: Full Page

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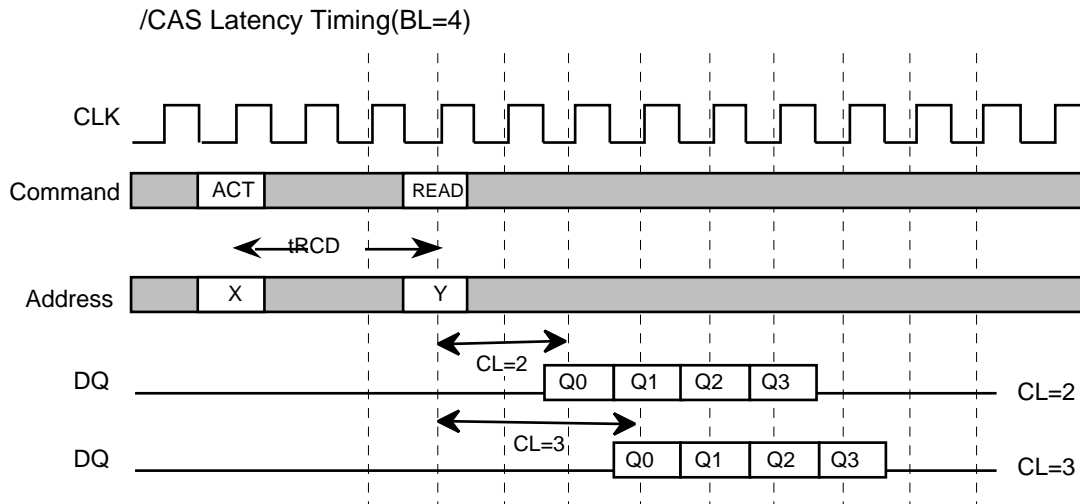
Initial Address			BL	Column Addressing															
A2	A1	A0		Sequential								Interleaved							
0	0	0	8	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
0	0	1		1	2	3	4	5	6	7	0	1	0	3	2	5	4	7	6
0	1	0		2	3	4	5	6	7	0	1	2	3	0	1	6	7	4	5
0	1	1		3	4	5	6	7	0	1	2	3	2	1	0	7	6	5	4
1	0	0		4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3
1	0	1		5	6	7	0	1	2	3	4	5	4	7	6	1	0	3	2
1	1	0		6	7	0	1	2	3	4	5	6	7	4	5	2	3	0	1
1	1	1		7	0	1	2	3	4	5	6	7	6	5	4	3	2	1	0
-	0	0	4	0	1	2	3					0	1	2	3				
-	0	1		1	2	3	0					1	0	3	2				
-	1	0		2	3	0	1					2	3	0	1				
-	1	1		3	0	1	2					3	2	1	0				
-	-	0	2	0	1							0	1						
-	-	1		1	0							1	0						

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## [ /CAS LATENCY ]

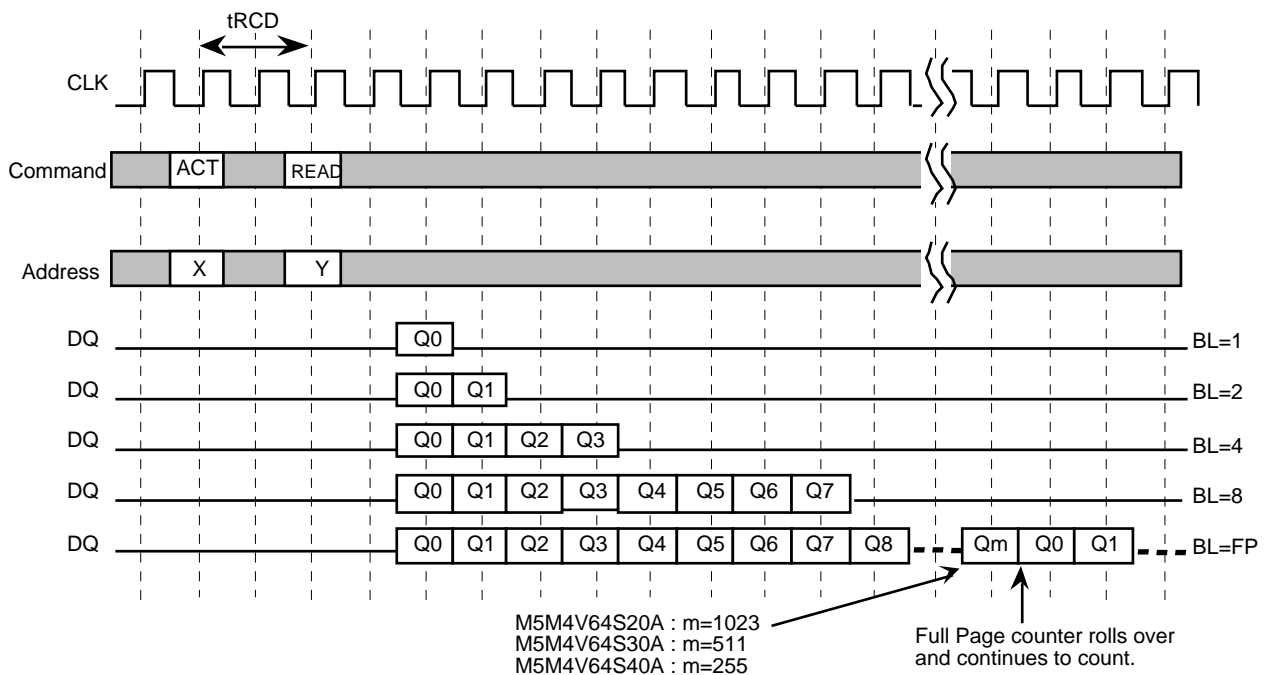
/CAS latency, CL, is used to synchronize the first output data with the CLK frequency, i.e., the speed of CLK determines which CL should be used. First output data is available after CL cycles from READ command.



## [ BURST LENGTH ]

The burst length, BL, determines the number of consecutive writes or reads that will be automatically performed after the initial write or read command. For BL=1,2,4,8, the output data is tristated (Hi-Z) after the last read. For BL=FP (Full Page), the TBST (Burst Terminate) command must be used to stop the output of data.

Burst Length Timing( CL=2 )



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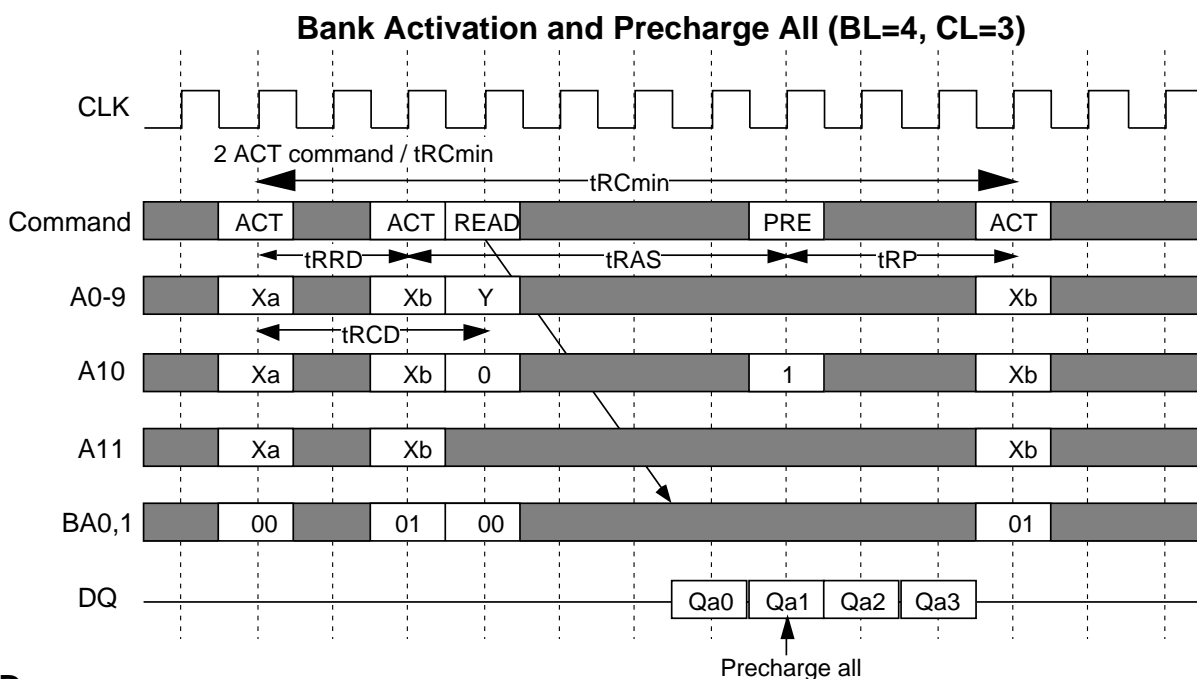
## OPERATIONAL DESCRIPTION

### BANK ACTIVATE

The SDRAM has four independent banks. Each bank is activated by the ACT command with the bank addresses (BA0,1). A row is indicated by the row addresses A11-0. The minimum activation interval between one bank and the other bank is tRRD. *Maximum 2 ACT commands are allowed within tRC*, although the number of banks which are active concurrently is not limited.

### PRECHARGE

The PRE command deactivates the bank indicated by BA0,1. When multiple banks are active, the precharge all command (PREA, PRE + A10=H) is available to deactivate them at the same time. After tRP from the precharge, an ACT command to the same bank can be issued.



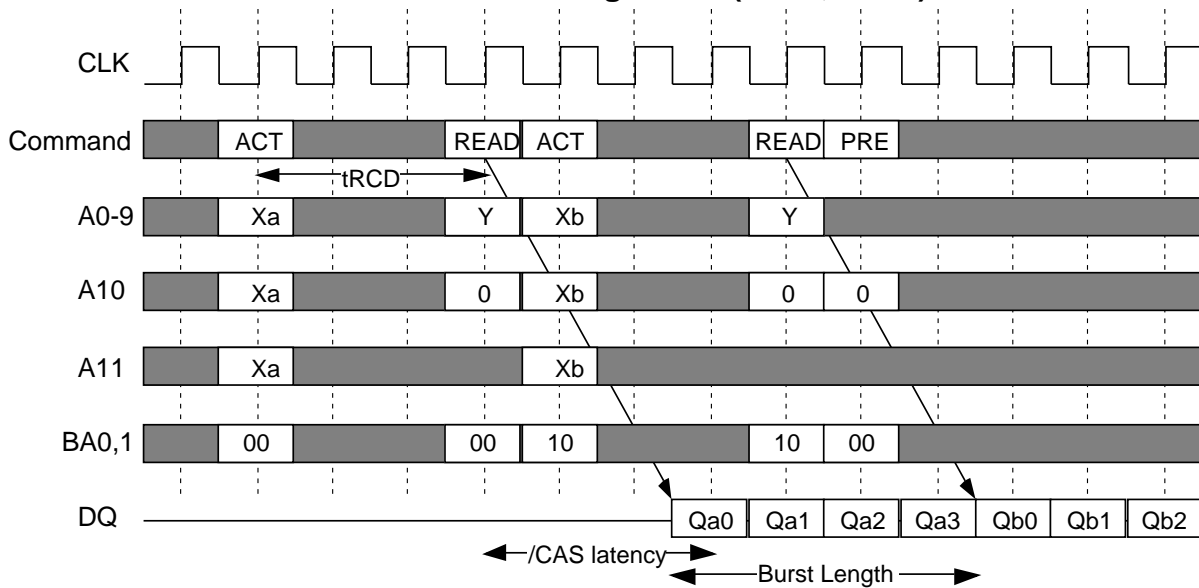
### READ

After tRCD from the bank activation, a READ command can be issued. 1st output data is available after the /CAS Latency from the READ, followed by (BL - 1) consecutive data when the Burst Length is BL. The start address is specified by A8-0(X8), A9-0(X4) and the address sequence of burst data is defined by the Burst Type. A READ command may be applied to any active bank, so the row precharge time (tRP) can be hidden behind continuous output data by interleaving the multiple banks. When A10 is high at a READ command, the auto-precharge (READA) is performed. Any command (READ, WRITE, PRE, ACT) to the same bank is inhibited till the internal precharge is complete. The internal precharge starts at BL after READA. The next ACT command can be issued after (BL + tRP) from the previous READA.

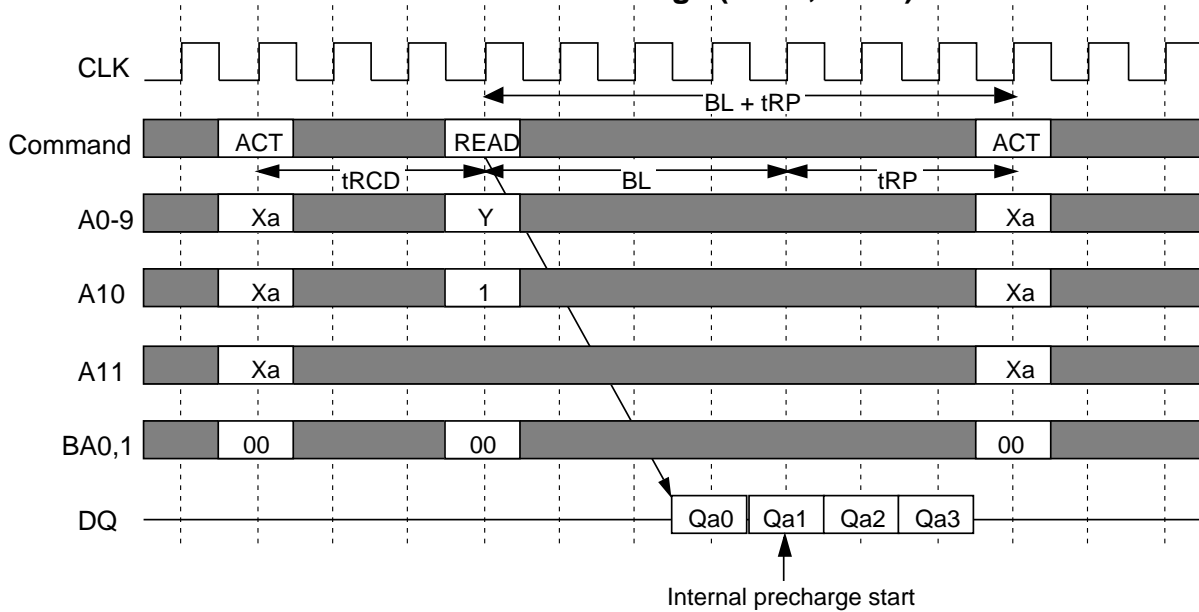
# M5M4V64S30ATP-8A,-8L,-8, -10L, -10

64M (4-BANK x 2097152-WORD x 8-BIT) Synchronous DRAM

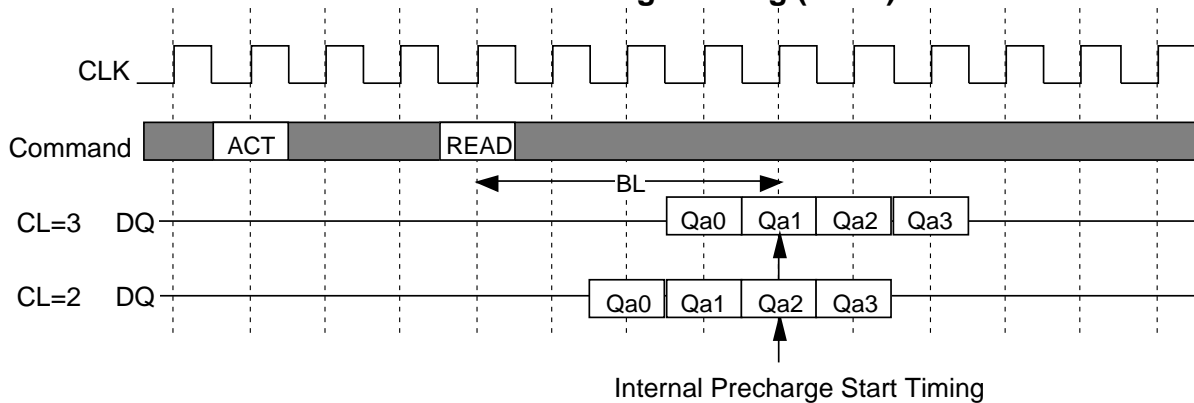
## Multi Bank Interleaving READ (BL=4, CL=3)



## READ with Auto-Precharge (BL=4, CL=3)



## READ Auto-Precharge Timing (BL=4)





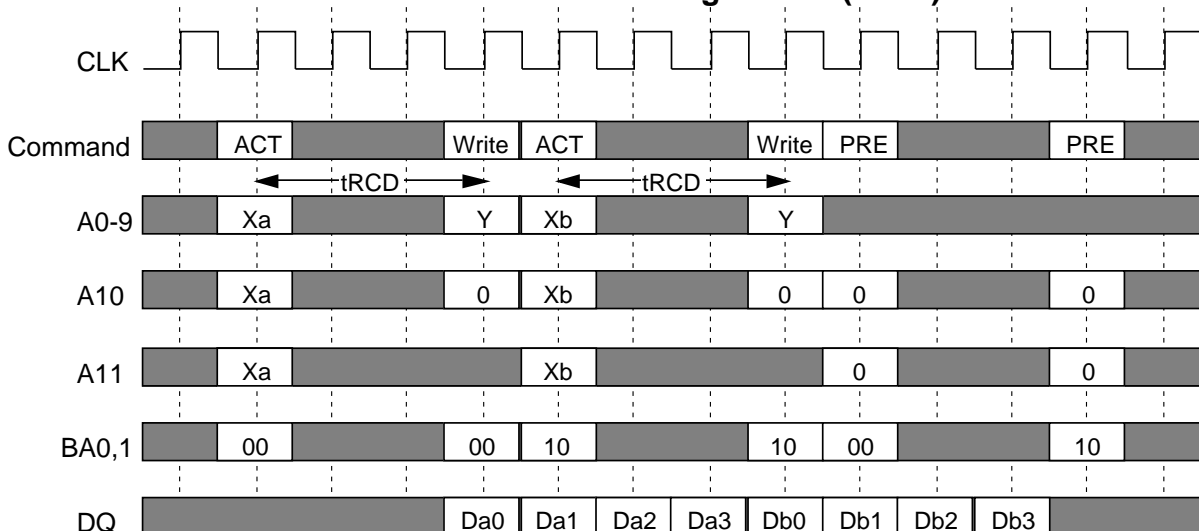
# M5M4V64S30ATP-8A,-8L,-8, -10L, -10

## 64M (4-BANK x 2097152-WORD x 8-BIT) Synchronous DRAM

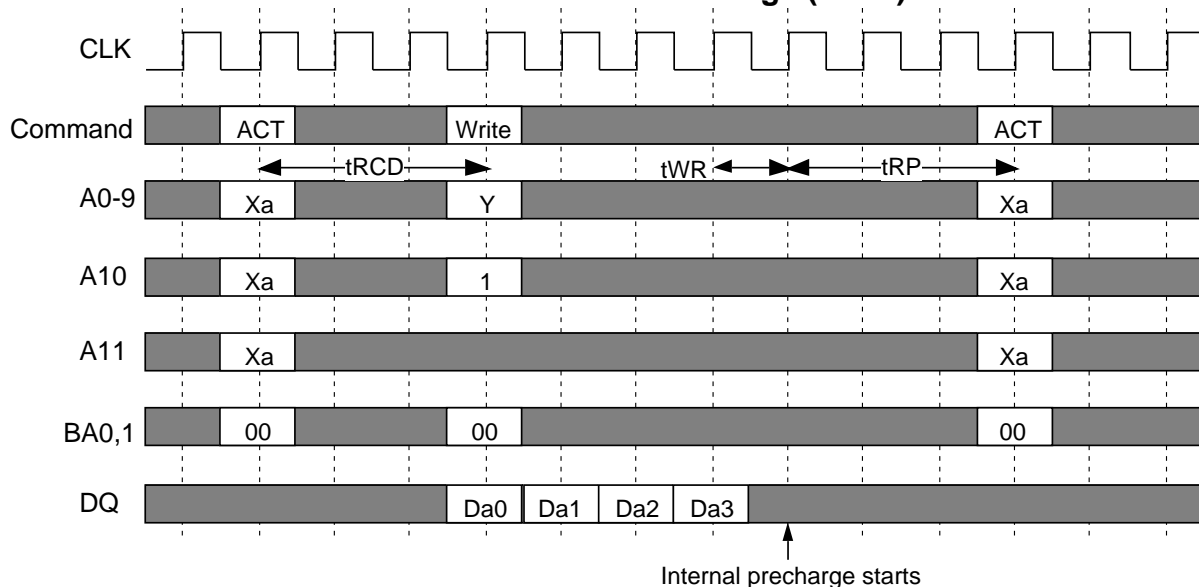
### WRITE

After tRCD from the bank activation, a WRITE command can be issued. 1st input data is set at the same cycle as the WRITE. Following (BL - 1) data are written into the RAM, when the Burst Length is BL. The start address is specified by A8-0 (x 8), A9-0 (x 4), and the address sequence of burst data is defined by the Burst Type. A WRITE command may be applied to any active bank, so the row precharge time (tRP) can be hidden behind continuous input data by interleaving the multiple banks. From the last input data to the PRE command, the write recovery time (tWR) is required. When A10 is high at a WRITE command, the auto-precharge (WRITEEA) is performed. Any command (READ, WRITE, PRE, ACT) to the same bank is inhibited till the internal precharge is complete. The internal precharge begins at tWR after the last input data cycle. The next ACT command can be issued after tRP from the internal precharge timing. The Mode Register can be programmed for burst read and single write. In this mode the write data is only clocked in when the WRITE command is issued and the remaining burst length is ignored. The read data burst length is unaffected while in this mode

#### Multi Bank Interleaving WRITE (BL=4)



#### WRITE with Auto-Precharge (BL=4)

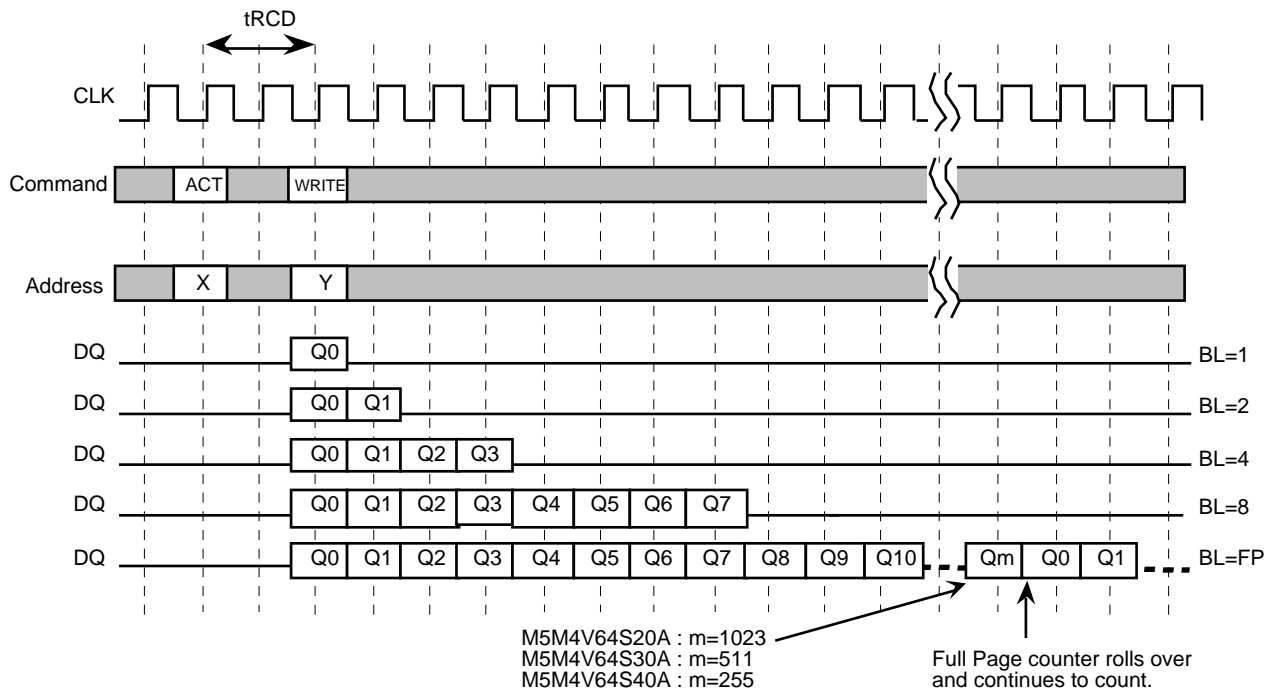


# M5M4V64S30ATP-8A,-8L,-8, -10L, -10

64M (4-BANK x 2097152-WORD x 8-BIT) Synchronous DRAM

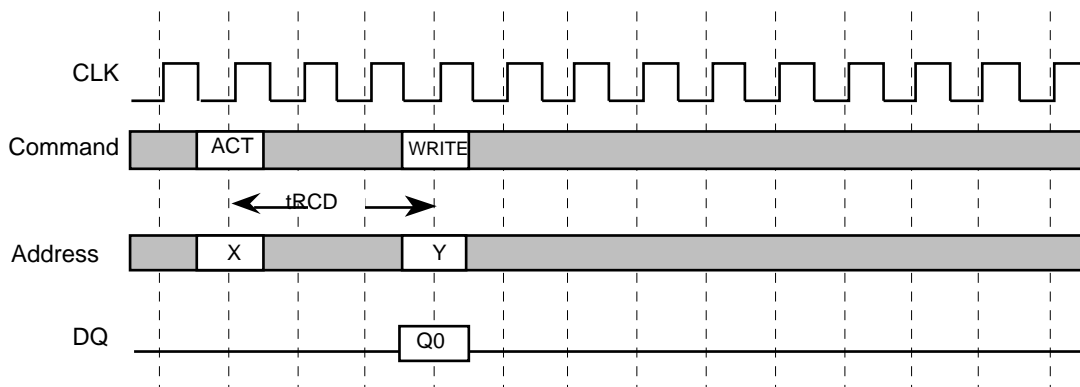
## [ BURST WRITE ]

A burst write operation is enabled by setting A9=0. A burst write starts in the same cycle as a write command set. (The latency of data input is 0.) The burst length can be set to 1,2,4,8, and full-page, like burst read operations.



## [ SINGLE WRITE ]

A single write operation is enabled by setting A9=1. In a single write operation, data is only written to the column address specified by the write command set cycle without regard to the burst length setting. (The latency of data input is 0.)



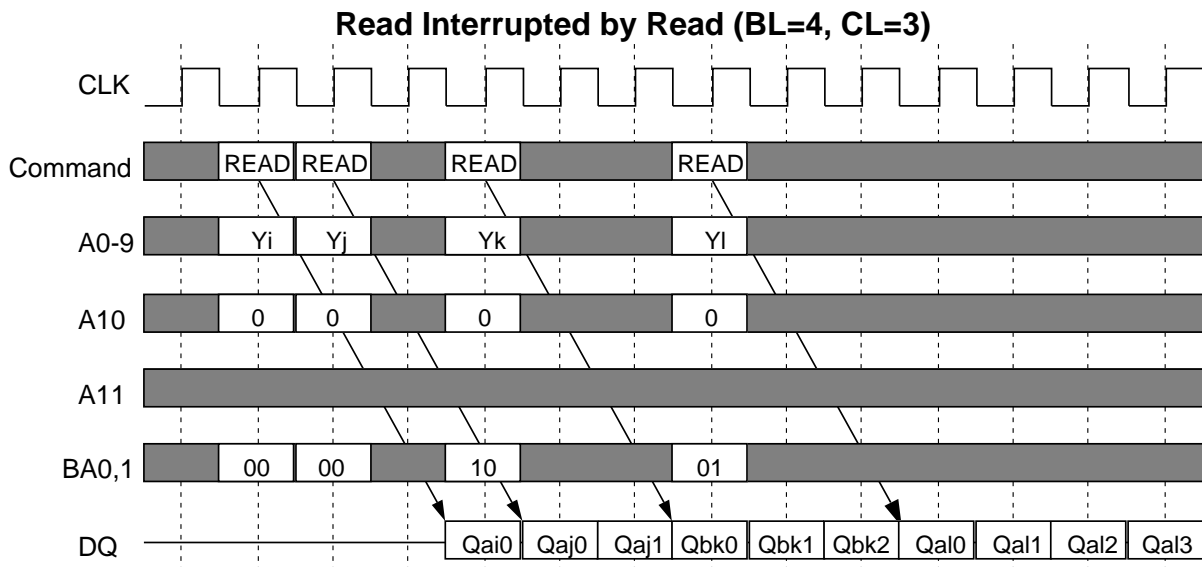
# M5M4V64S30ATP-8A,-8L,-8, -10L, -10

64M (4-BANK x 2097152-WORD x 8-BIT) Synchronous DRAM

## BURST INTERRUPTION

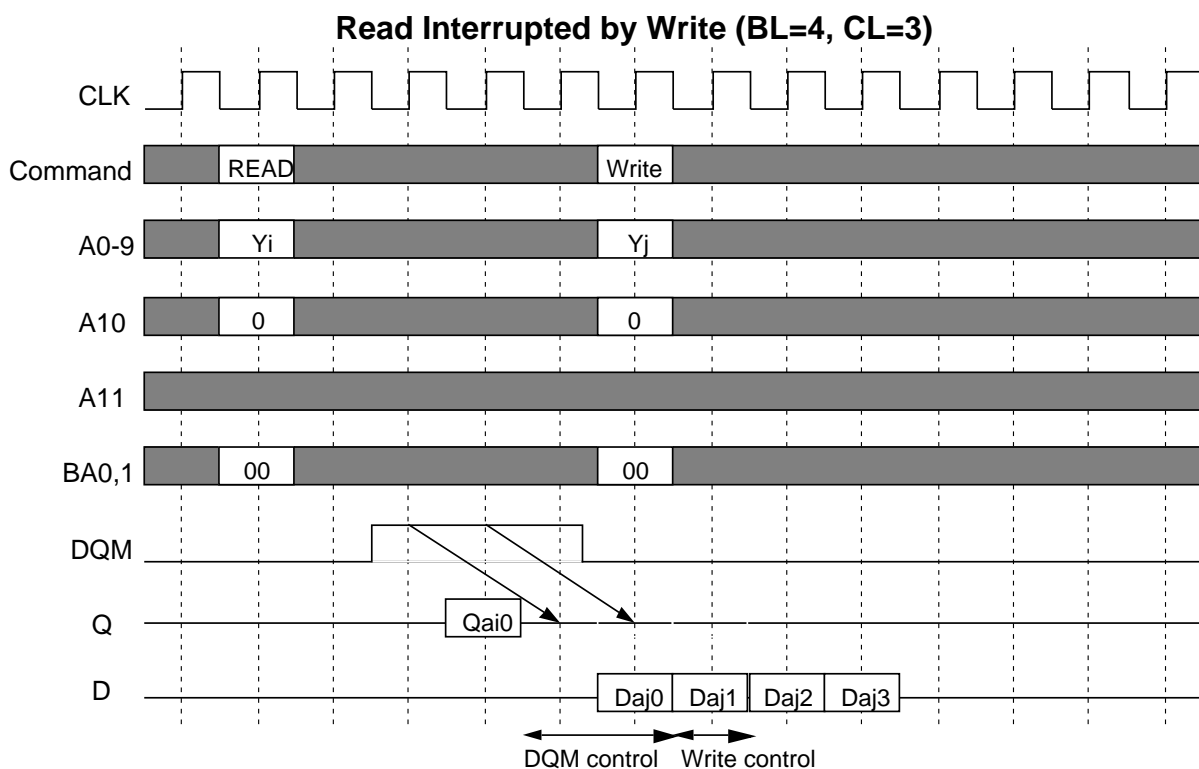
### [ Read Interrupted by Read ]

Burst read operation can be interrupted by new read of any bank. Random column access is allowed. READ to READ interval is minimum 1 CLK.



### [ Read Interrupted by Write ]

Burst read operation can be interrupted by write of any bank. Random column access is allowed. In this case, the DQ should be controlled adequately by using the DQM to prevent the bus contention. The output is disabled automatically 1 cycle after WRITE assertion.

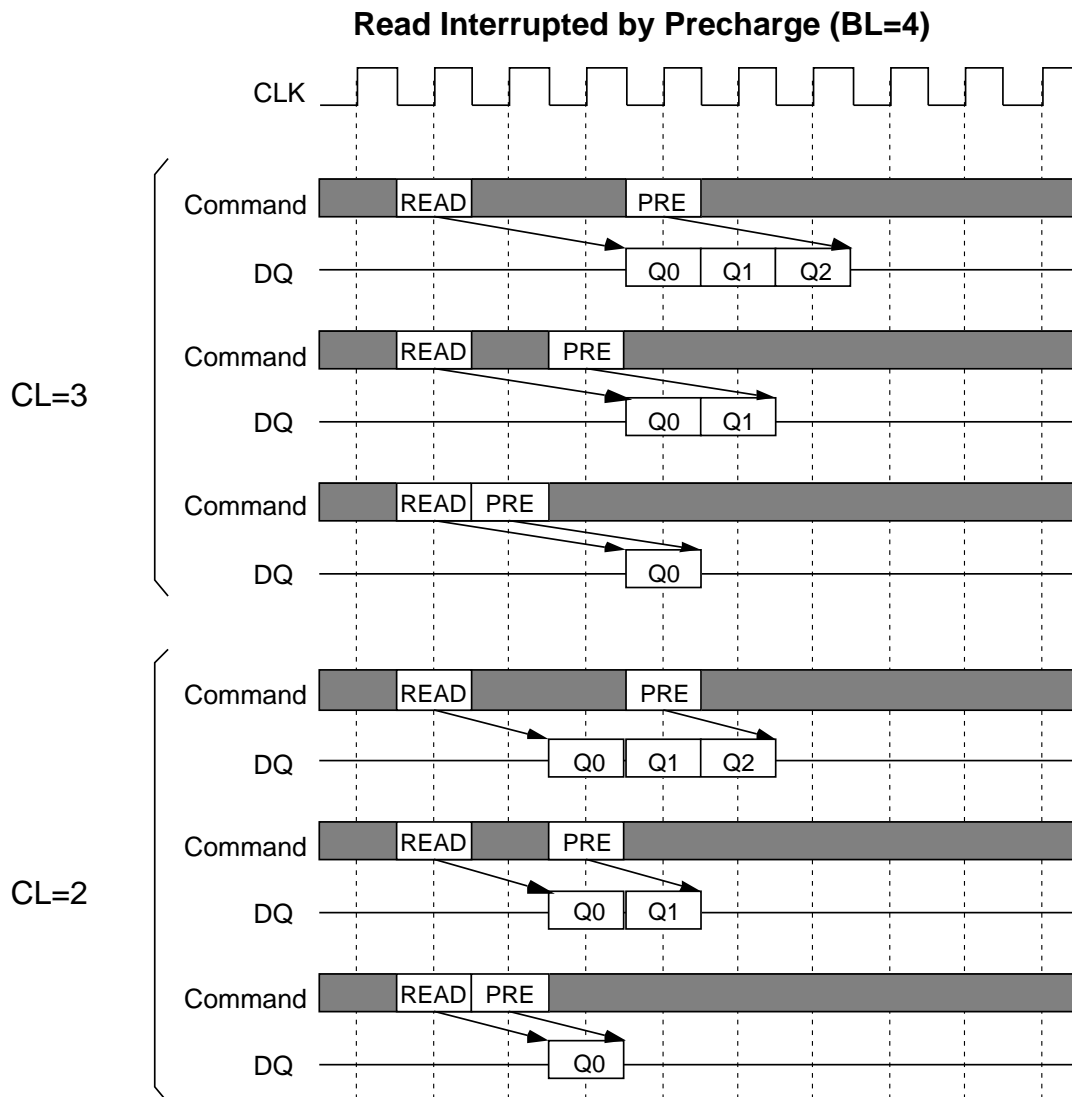


# M5M4V64S30ATP-8A,-8L,-8, -10L, -10

64M (4-BANK x 2097152-WORD x 8-BIT) Synchronous DRAM

## [ Read Interrupted by Precharge ]

Burst read operation can be interrupted by precharge of *the same bank*. READ to PRE interval is minimum 1 CLK. A PRE command to output disable latency is equivalent to the /CAS Latency. As a result, READ to PRE interval determines valid data length to be output. The figure below shows examples of BL=4.

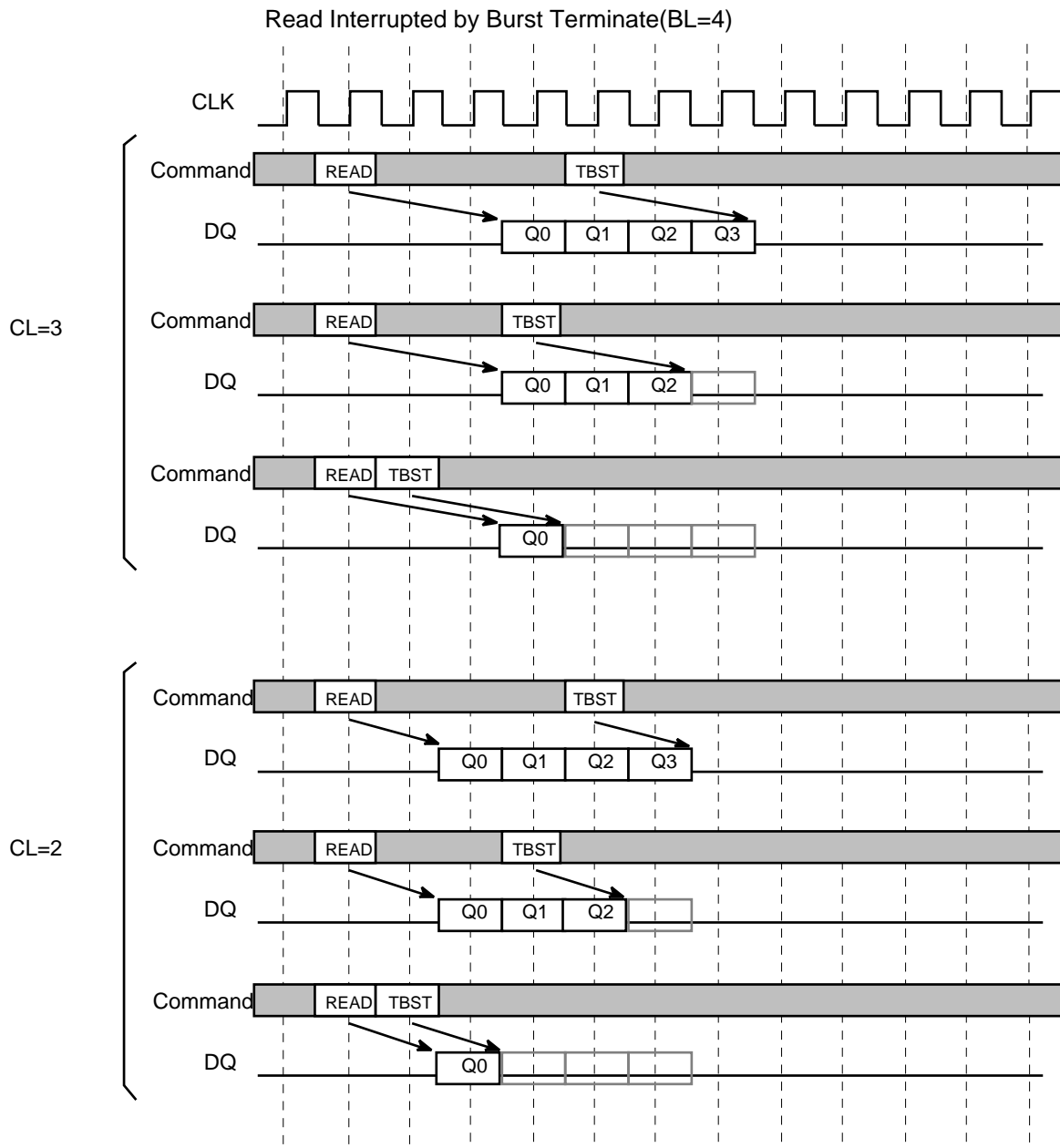


# M5M4V64S30ATP-8A,-8L,-8, -10L, -10

64M (4-BANK x 2097152-WORD x 8-BIT) Synchronous DRAM

## [ Read Interrupted by Burst Terminate ]

Similar to a precharge, the burst terminate command, TBST, can interrupt the burst read operation and disable the data output. The READ to TBST interval is a minimum of one CLK. TBST is mainly used to interrupt FP bursts. The figures below show examples, of how the output data is terminated with TBST.



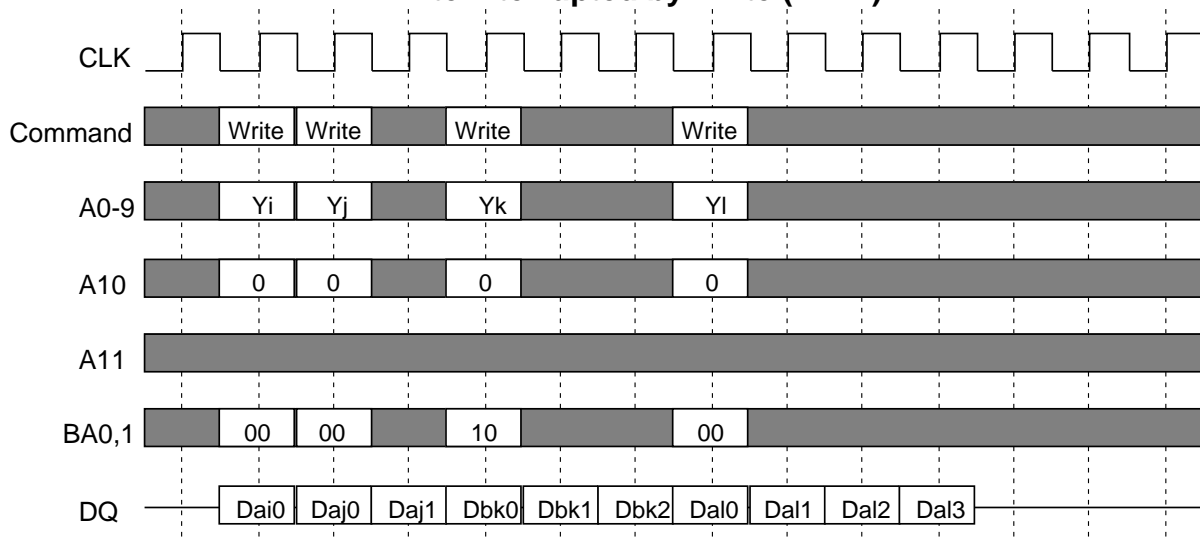
# M5M4V64S30ATP-8A,-8L,-8, -10L, -10

64M (4-BANK x 2097152-WORD x 8-BIT) Synchronous DRAM

## [ Write Interrupted by Write ]

Burst write operation can be interrupted by new write of any bank. Random column access is allowed. WRITE to WRITE interval is minimum 1 CLK.

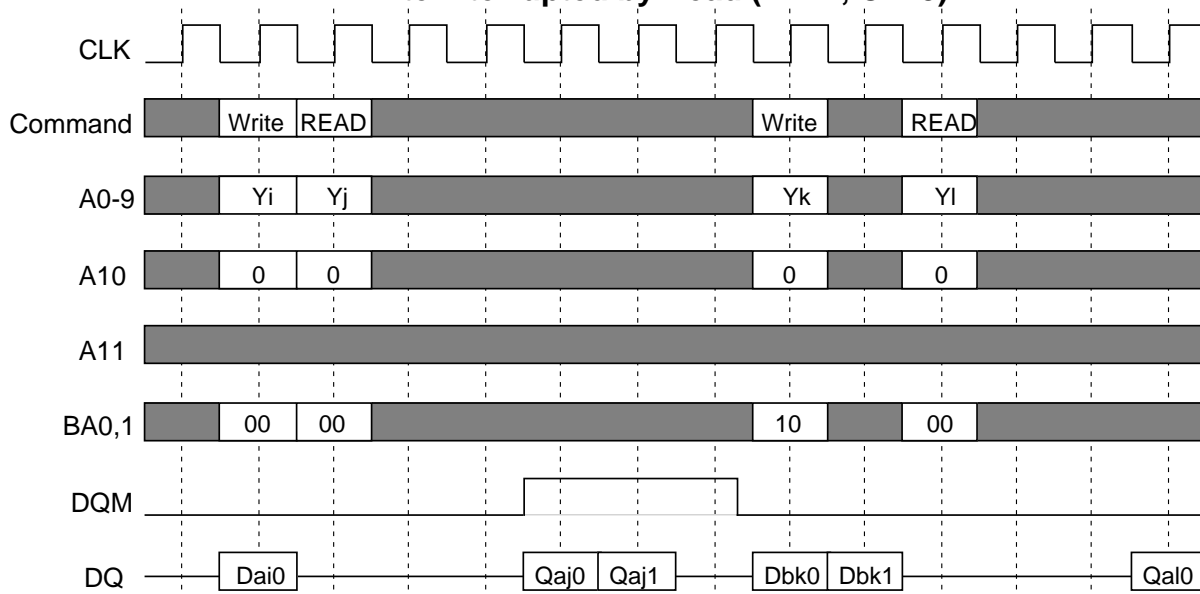
Write Interrupted by Write (BL=4)



## [ Write Interrupted by Read ]

Burst write operation can be interrupted by read of the same or the other bank. Random column access is allowed. WRITE to READ interval is minimum 1 CLK. The input data on DQ at the interrupting READ cycle is "don't care".

Write Interrupted by Read (BL=4, CL=3)

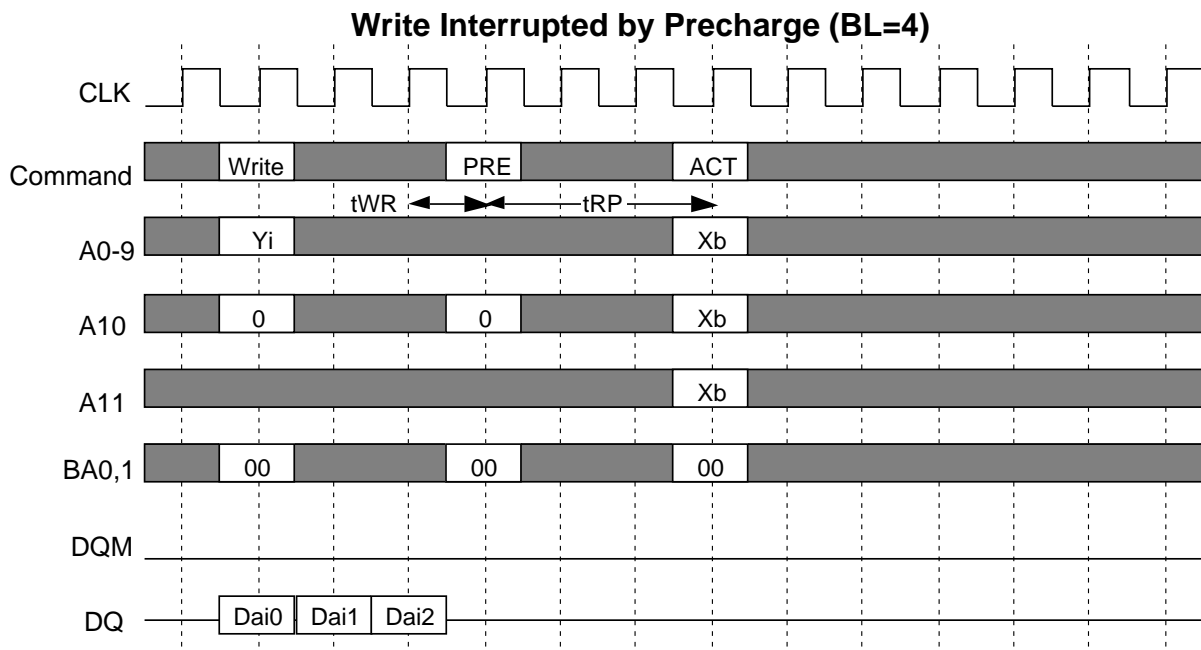


# M5M4V64S30ATP-8A,-8L,-8, -10L, -10

64M (4-BANK x 2097152-WORD x 8-BIT) Synchronous DRAM

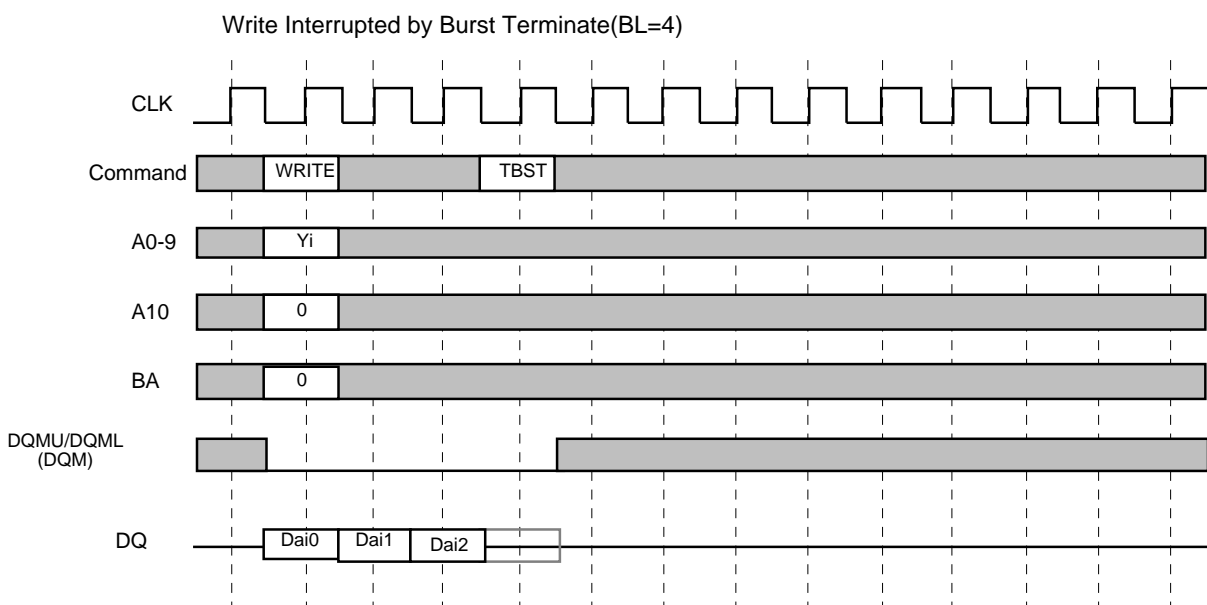
## [ Write Interrupted by Precharge ]

Burst write operation can be interrupted by precharge of *the same bank*. Random column access is allowed. Write recovery time ( $t_{WR}$ ) is required from the last data to PRE command.



## [ Write Interrupted by Burst Terminate ]

A burst terminate command TBST can be used to terminate a burst write operation. In this case, the write recovery time is not required and the bank remains active (Please see the waveforms below). The WRITE to TBST minimum interval is one CLK.

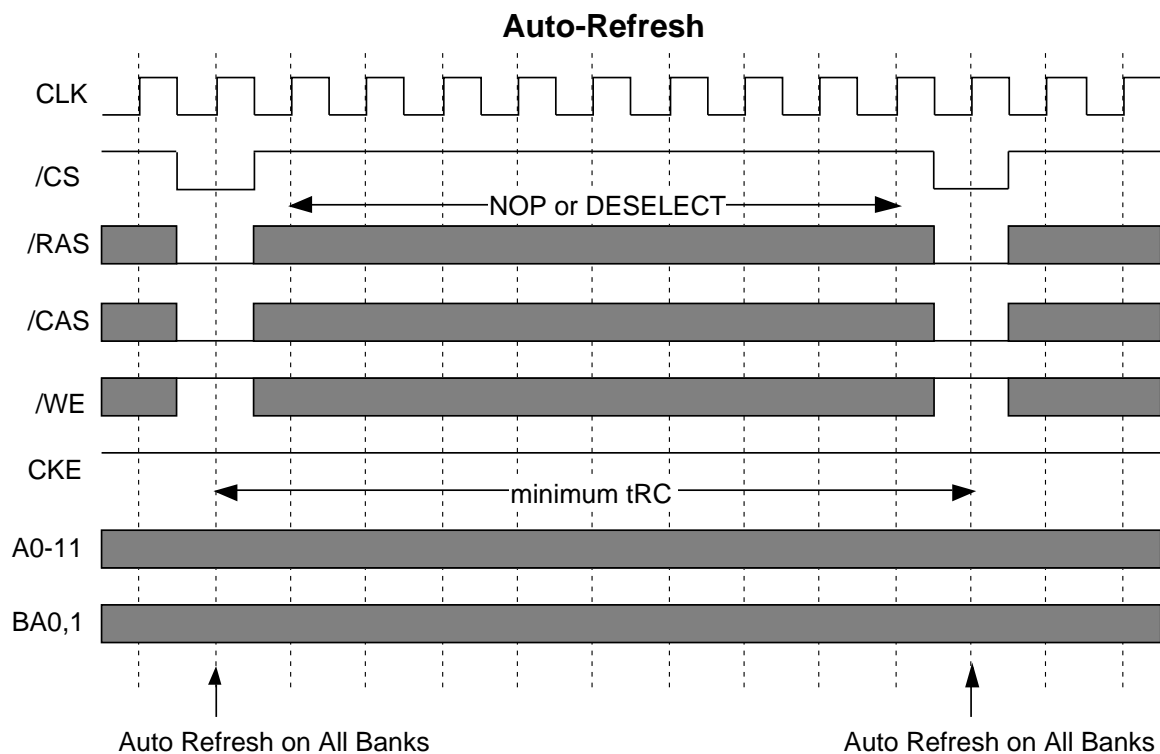


# M5M4V64S30ATP-8A,-8L,-8, -10L, -10

64M (4-BANK x 2097152-WORD x 8-BIT) Synchronous DRAM

## AUTO REFRESH

Single cycle of auto-refresh is initiated with a REFA (/CS= /RAS= /CAS= L, /WE= /CKE= H) command. The refresh address is generated internally. 4096 REFA cycles within 64ms refresh 64Mbit memory cells. The auto-refresh is performed on 4 banks concurrently. Before performing an auto-refresh, all banks must be in the idle state. Auto-refresh to auto-refresh interval is minimum tRC. Any command must not be supplied to the device before tRC from the REFA command.





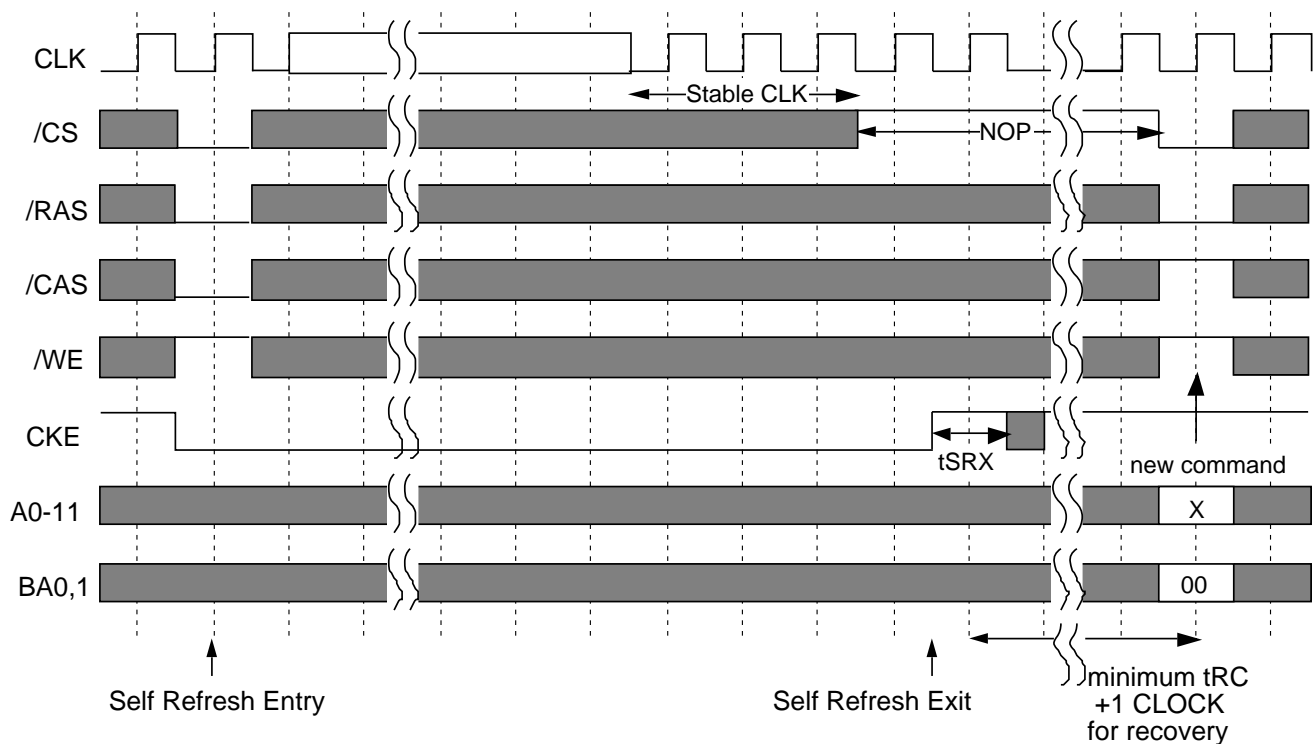
# M5M4V64S30ATP-8A,-8L,-8, -10L, -10

64M (4-BANK x 2097152-WORD x 8-BIT) Synchronous DRAM

## SELF REFRESH

Self-refresh mode is entered by issuing a REFS command ( $\overline{\text{CS}} = \overline{\text{RAS}} = \overline{\text{CAS}} = \text{L}$ ,  $\overline{\text{WE}} = \text{H}$ ,  $\text{CKE} = \text{L}$ ). Once the self-refresh is initiated, it is maintained as long as CKE is kept low. During the self-refresh mode, CKE is asynchronous and the only enabled input, all other inputs including CLK are disabled and ignored, so that power consumption due to synchronous inputs is saved. To exit the self-refresh, supplying stable CLK inputs, asserting DESEL or NOP command and then asserting CKE (REFSX) for longer than  $t_{\text{SRX}}$ . After  $t_{\text{RC}}$  from REFSX all banks are in the idle state and a new command can be issued, but DESEL or NOP commands must be asserted till then.

Self-Refresh

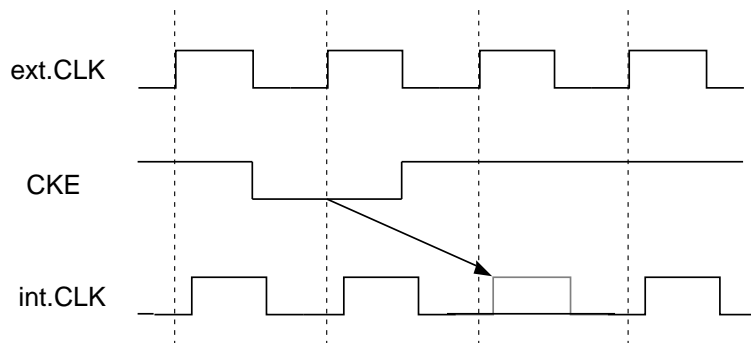


# M5M4V64S30ATP-8A,-8L,-8, -10L, -10

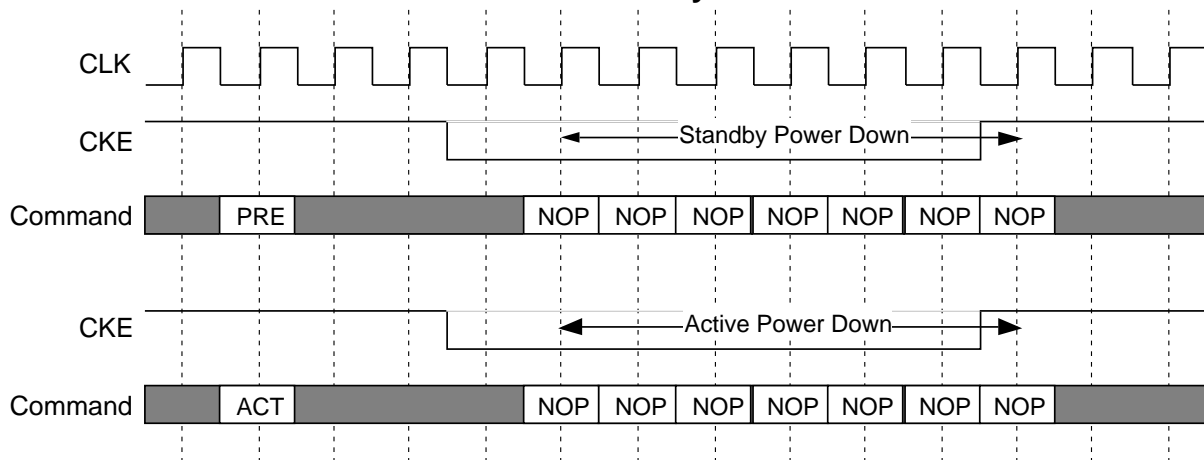
64M (4-BANK x 2097152-WORD x 8-BIT) Synchronous DRAM

## CLK SUSPEND

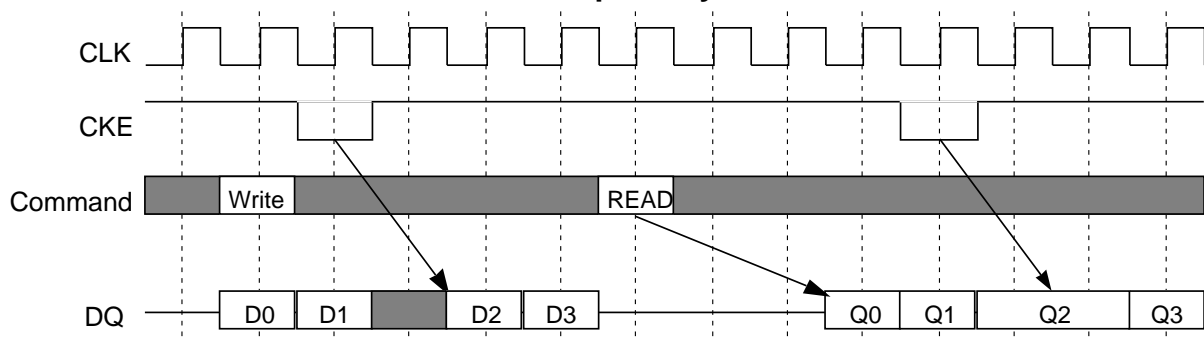
CKE controls the internal CLK at the following cycle. Figure below shows how CKE works. By negating CKE, the next internal CLK is suspended. The purpose of CLK suspend is power down, output suspend or input suspend. CKE is a synchronous input except during the self-refresh mode. CLK suspend can be performed either when the banks are active or idle. A command at the suspended cycle is ignored.



### Power Down by CKE



### DQ Suspend by CKE



# M5M4V64S30ATP-8A,-8L,-8, -10L, -10

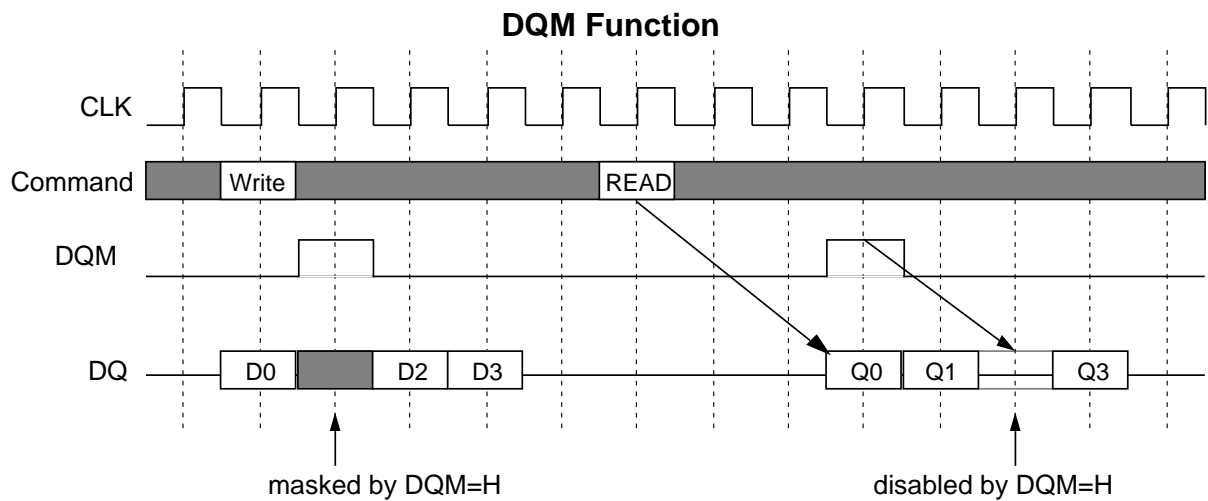
64M (4-BANK x 2097152-WORD x 8-BIT) Synchronous DRAM

## DQM CONTROL

DQM is a dual function signal defined as the data mask for writes and the output disable for reads.

During writes, DQM masks input data word by word. DQM to write mask latency is 0.

During reads, DQM forces output to Hi-Z word by word. DQM to output Hi-Z latency is 2.



**M5M4V64S30ATP-8A,-8L,-8, -10L, -10**

64M (4-BANK x 2097152-WORD x 8-BIT) Synchronous DRAM

**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Conditions	Ratings	Unit
Vdd	Supply Voltage	with respect to Vss	-0.5 ~ 4.6	V
VddQ	Supply Voltage for Output	with respect to VssQ	-0.5 ~ 4.6	V
VI	Input Voltage	with respect to Vss	-0.5 ~ Vdd+0.5	V
VO	Output Voltage	with respect to VssQ	-0.5 ~ VddQ+0.5	V
IO	Output Current		50	mA
Pd	Power Dissipation	Ta = 25 °C	1000	mW
Topr	Operating Temperature		0 ~ 70	°C
Tstg	Storage Temperature		-65 ~ 150	°C

**RECOMMENDED OPERATING CONDITIONS**

(Ta=0 ~ 70°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
Vdd	Supply Voltage	3.0	3.3	3.6	V
Vss	Supply Voltage	0	0	0	V
VddQ	Supply Voltage for Output	3.0	3.3	3.6	V
VssQ	Supply Voltage for Output	0	0	0	V
VIH	High-Level Input Voltage all inputs	2.0		Vdd+0.3	V
VIL	Low-Level Input Voltage all inputs	-0.3		0.8	V

Note:\* VIH (max) = Vdd+2.0V AC for pulse width<=3ns acceptable.  
VIL(min) = -2V AC for pulse width<=3ns acceptable.

**CAPACITANCE**

(Ta=0 ~ 70°C, Vdd = VddQ = 3.3 ± 0.3v, Vss = VssQ = 0v, unless otherwise noted)

Symbol	Parameter	Test Condition	min.	max.	Unit
CI(A)	Input Capacitance, address pin	VI=Vss f=1MHz Vi=25mVrms	2.5	5	pF
CI(C)	Input Capacitance, control pin		2.5	5	pF
CI(K)	Input Capacitance, CLK pin		2.5	4	pF
CI/O	Input Capacitance, I/O pin		4	6.5	pF

SDRAM (Rev.1.3)  
Mar'98

# M5M4V64S30ATP-8A,-8L,-8, -10L, -10

64M (4-BANK x 2097152-WORD x 8-BIT) Synchronous DRAM

## AVERAGE SUPPLY CURRENT from Vdd

(Ta=0 ~ 70°C, Vdd = VddQ = 3.3 ± 0.3v, Vss = VssQ = 0v, Output Open, unless otherwise noted)

Symbol	Parameter	Test Conditions	Limits (max)			Unit	
			-8A	-8L -8	-10L -10		
lcc1s	operating current, single bank	tRC=min, tCLK=min, BL=1, CL=3	110	110	85	mA	
lcc1d	operating current, dual bank	tRC=90ns, tCLK=min, BL=1, CL=3	135	115	115	mA	
lcc2h	standby current, CKE=H	all banks idle, tCLK=min	25	22	22	mA	
lcc2l	standby current, CKE=L	all banks idle, tCLK=min	2	2	2	mA	
lcc3h	active standby current, CKE=H	all banks active, tCLK=min	55	55	45	mA	
lcc3l	active standby current, CKE=L	all banks active, tCLK=min	5	5	2	mA	
lcc4	burst current	all banks active, tCLK=min, BL=4, CL=3	135	115	115	mA	
lcc5	auto-refresh current	tRC=min, tCLK=min	150	150	115	mA	
lcc6	self-refresh current	CKE <0.2v	-8A,-8,-10	1	1	1	mA
			-8L,-10L	—	0.5	0.5	mA

## AC OPERATING CONDITIONS AND CHARACTERISTICS

(Ta=0 ~ 70°C, Vdd = VddQ = 3.3 ± 0.3v, Vss = VssQ = 0v, unless otherwise noted)

Symbol	Parameter	Test Conditions	Limits		Unit
			Min.	Max.	
VOH (DC)	High-Level Output Voltage (DC)	IOH=-2mA	2.4		V
VOL (DC)	Low-Level Output Voltage (DC)	IOL= 2mA		0.4	V
IOZ	Off-state Output Current	Q floating VO=0 ~ VddQ	-5	5	µA
I <sub>II</sub>	Input Current	VIH = 0 ~ VddQ+0.3V	-5	5	µA

SDRAM (Rev.1.3)  
Mar'98

# M5M4V64S30ATP-8A,-8L,-8, -10L, -10

64M (4-BANK x 2097152-WORD x 8-BIT) Synchronous DRAM

## AC TIMING REQUIREMENTS

( $T_a=0 \sim 70^\circ\text{C}$ ,  $V_{dd} = V_{ddQ} = 3.3 \pm 0.3\text{V}$ ,  $V_{ss} = V_{ssQ} = 0\text{V}$ , unless otherwise noted)

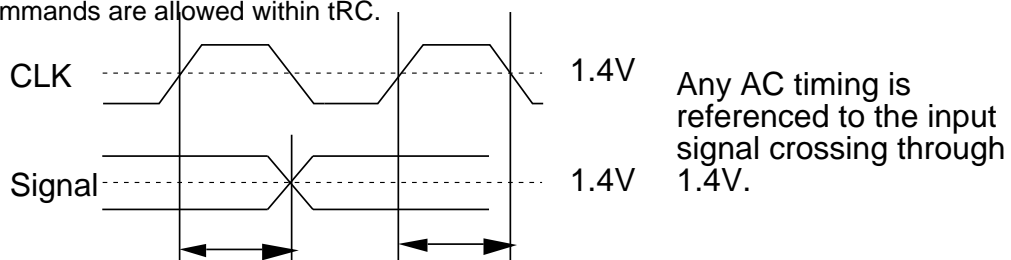
Input Pulse Levels: 0.8V to 2.0V

Input Timing Measurement Level: 1.4V

Symbol	Parameter		Limits						Unit	note
			-8A		-8L,-8		-10L, -10			
			Min.	Max.	Min.	Max.	Min.	Max.		
tCLK	CLK cycle time	CL=2	12		15		15		ns	
		CL=3	8		10		10		ns	
tCH	CLK High pulse width		3		3		4		ns	1
tCL	CLK Low pulse width		3		3		4		ns	1
tT	Transition time of CLK		1	10	1	10	1	10	ns	
tIS	Input Setup time (all inputs)		2		2		3		ns	1
tIH	Input Hold time (all inputs)		1		1		1		ns	1
tRC	Row Cycle time		72		70		90		ns	
tRCD	Row to Column Delay		20		20		30		ns	
tRAS	Row Active time		48	100K	50	100K	60	100K	ns	
tRP	Row Precharge time		20		20		30		ns	
tWR	Write Recovery time		10		10		10		ns	
tRRD	Act to Act Delay time		16		20		20		ns	2
tCCD	Col to Col Delay time		8		10		10		ns	
tRSC	Mode Register Set Cycle time		16		20		20		ns	
tSRX	Self Refresh Exit time		8		10		10		ns	
tREF	Refresh Interval time			64		64		64	ms	

Note:1 The timing requirements are assumed  $t_T=1\text{ns}$ . If  $t_T$  is longer than 1ns,  $(t_T-1)\text{ns}$  should be added to the parameter.

2 2 ACT commands are allowed within tRC.



# M5M4V64S30ATP-8A,-8L,-8, -10L, -10

64M (4-BANK x 2097152-WORD x 8-BIT) Synchronous DRAM

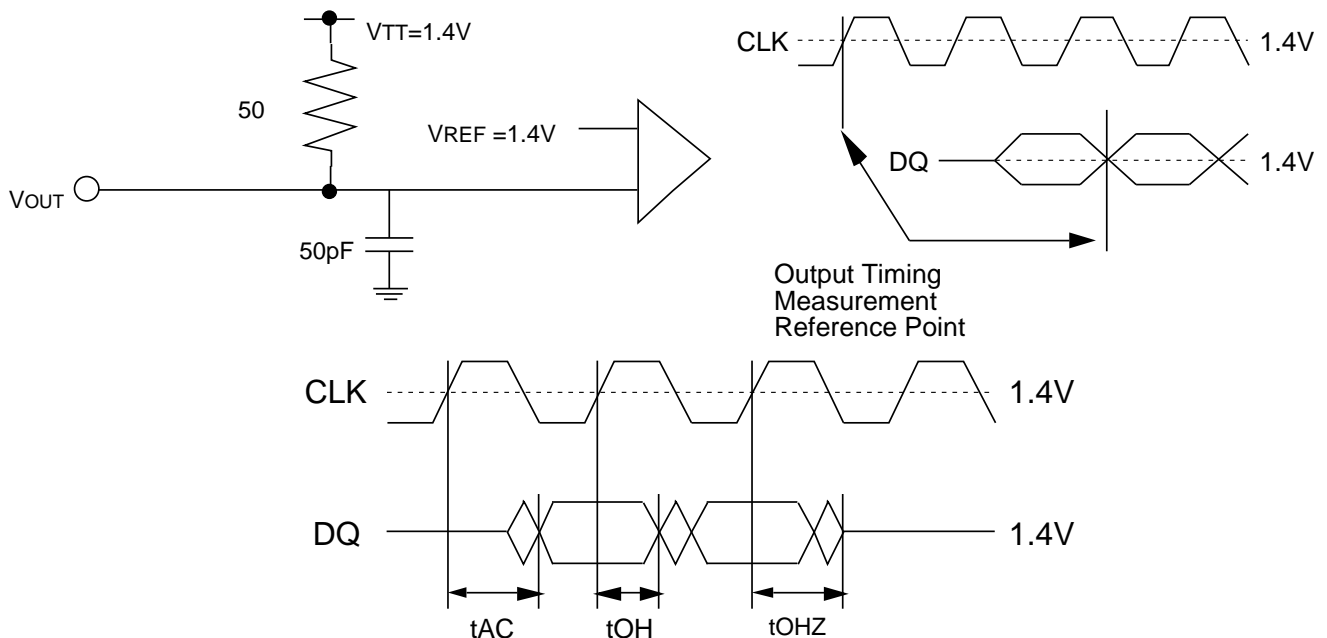
## SWITCHING CHARACTERISTICS

(Ta=0 ~ 70°C, Vdd = VddQ = 3.3 ± 0.3v, Vss = VssQ = 0v, unless otherwise noted see note3)

Symbol	Parameter		Limits						Unit
			-8A		-8L,-8		-10L, -10		
			Min.	Max.	Min.	Max.	Min.	Max.	
tAC	Access time from CLK	CL=2		8		9		9	ns
		CL=3		6		6		8	ns
tOH	Output Hold time from CLK		2.5		3		3		ns
tOLZ	Delay time, output low impedance from CLK		0		0		0		ns
tOHZ	Delay time, output high impedance from CLK		2.5	6	3	6	3	8	ns

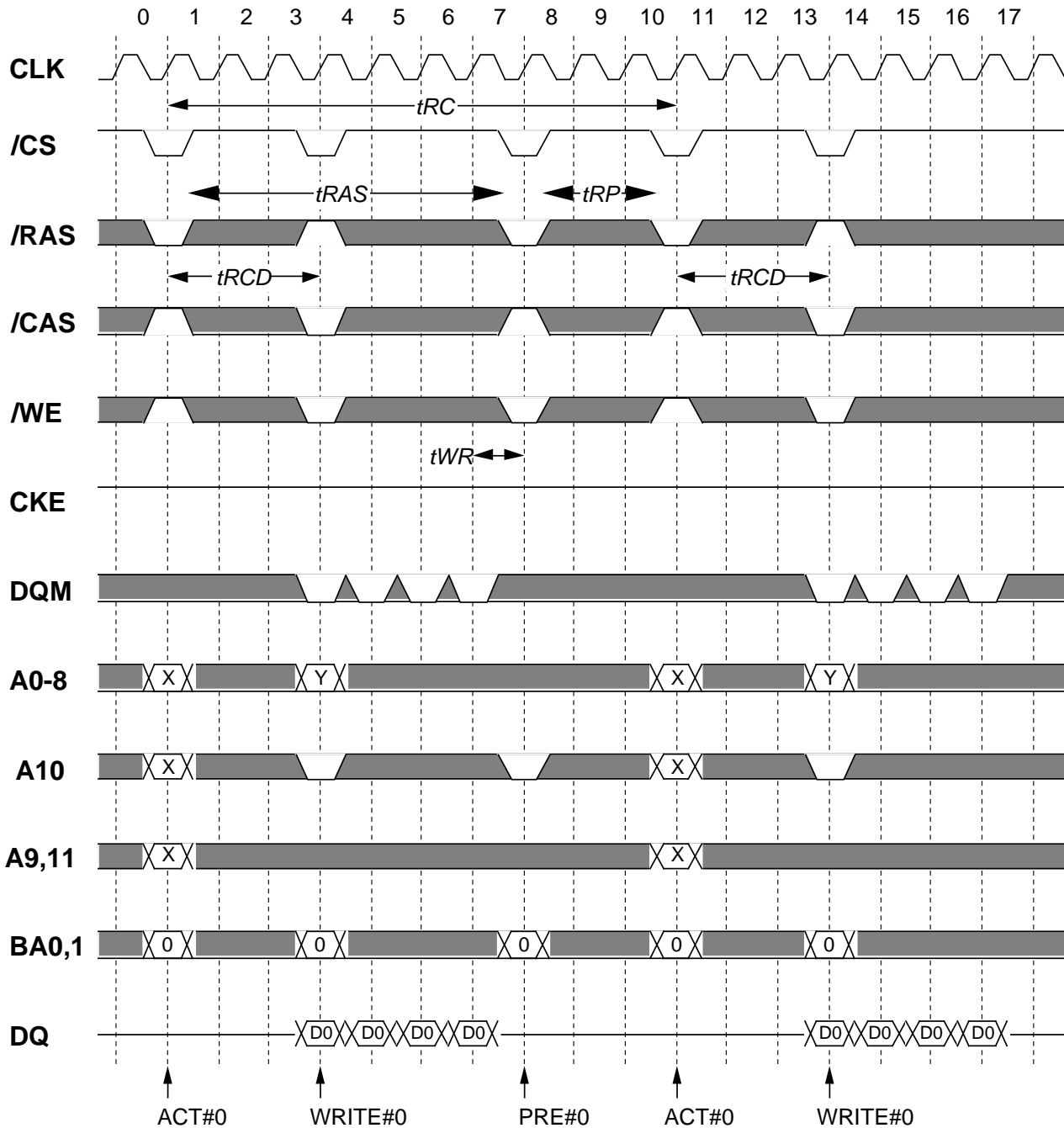
Note:3 If tr(clock rising time) is longer than 1ns, (tT/2-0.5)ns should be added to the parameter.

### Output Load Condition



**M5M4V64S30ATP-8A,-8L,-8, -10L, -10**  
64M (4-BANK x 2097152-WORD x 8-BIT) Synchronous DRAM

**Burst Write (single bank) @BL=4**

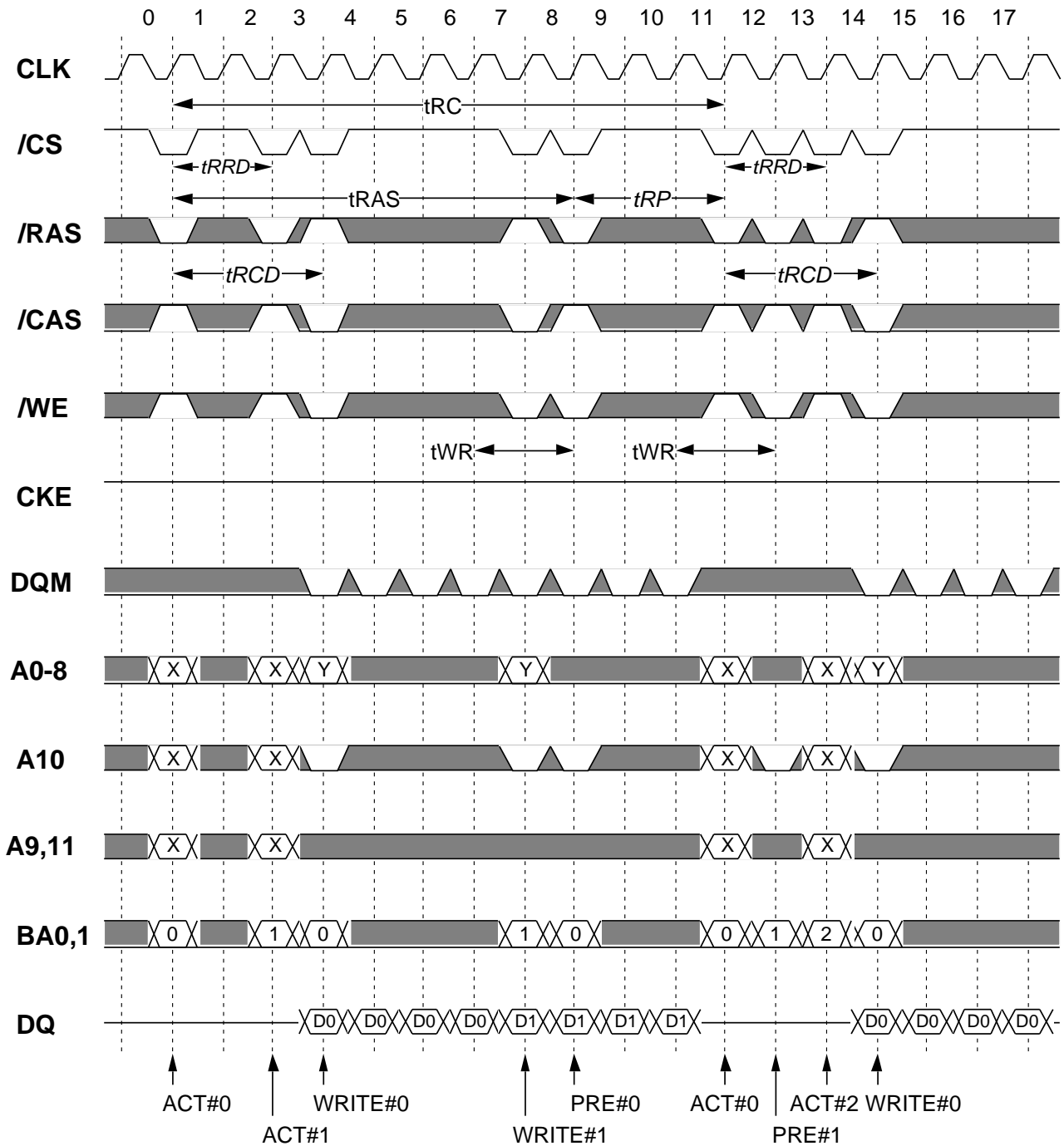


*Italic parameter* indicates minimum case



**M5M4V64S30ATP-8A,-8L,-8, -10L, -10**  
64M (4-BANK x 2097152-WORD x 8-BIT) Synchronous DRAM

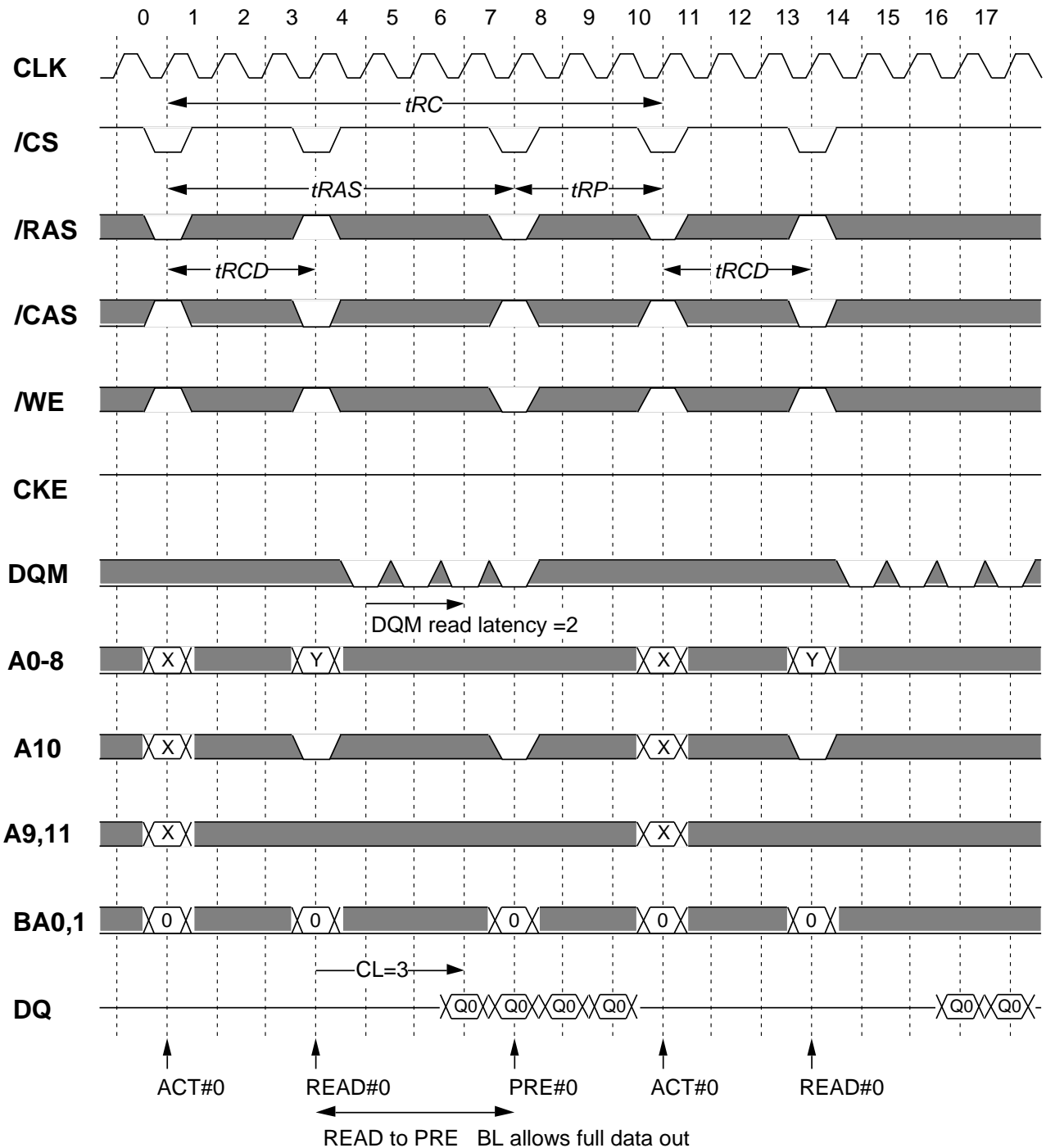
**Burst Write (multi bank) @BL=4**



*Italic parameter* indicates minimum case

**M5M4V64S30ATP-8A,-8L,-8, -10L, -10**  
64M (4-BANK x 2097152-WORD x 8-BIT) Synchronous DRAM

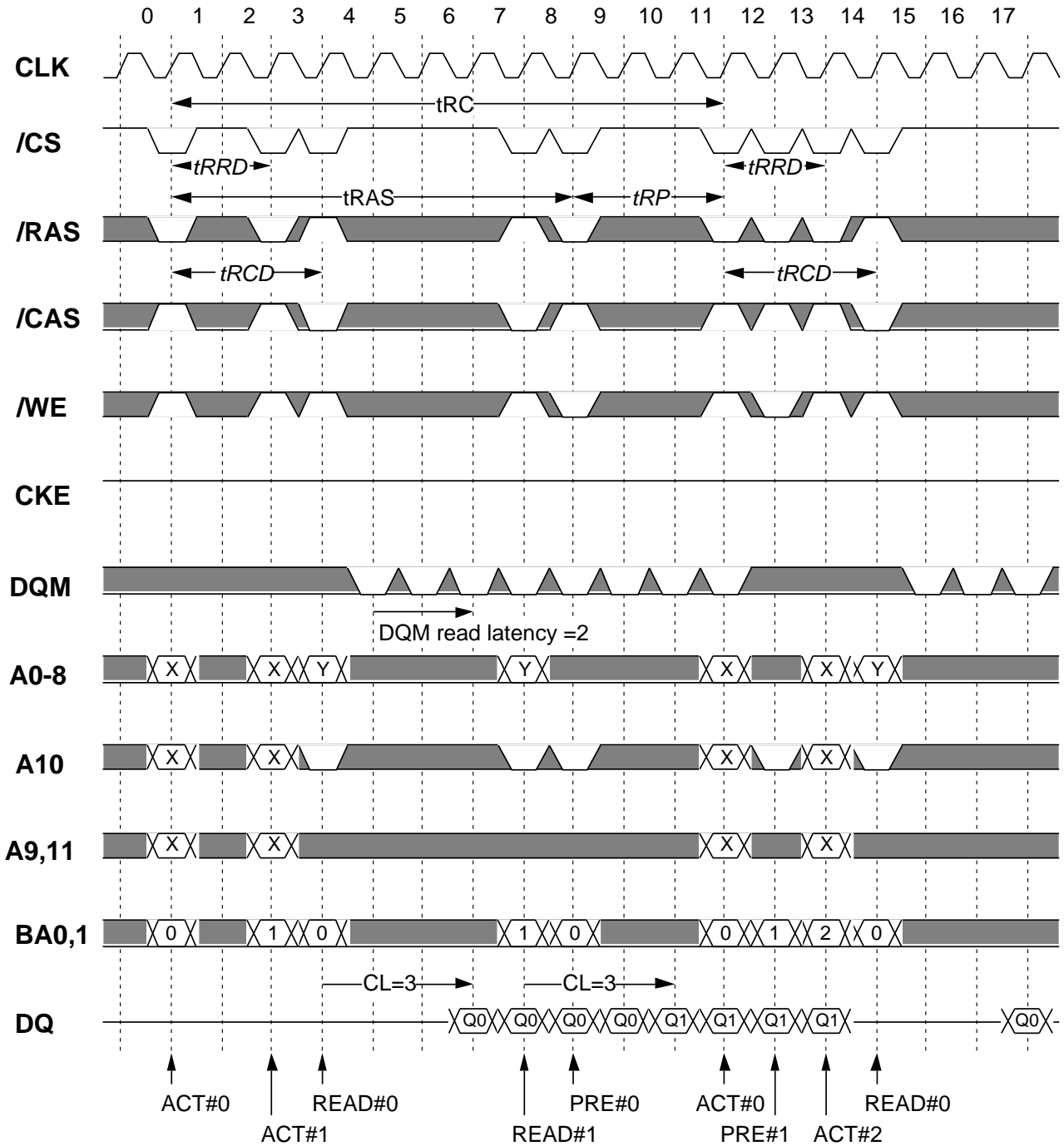
**Burst Read (single bank) @BL=4 CL=3**



*Italic parameter* indicates minimum case

**M5M4V64S30ATP-8A,-8L,-8, -10L, -10**  
64M (4-BANK x 2097152-WORD x 8-BIT) Synchronous DRAM

**Burst Read (multiple bank) @BL=4 CL=3**

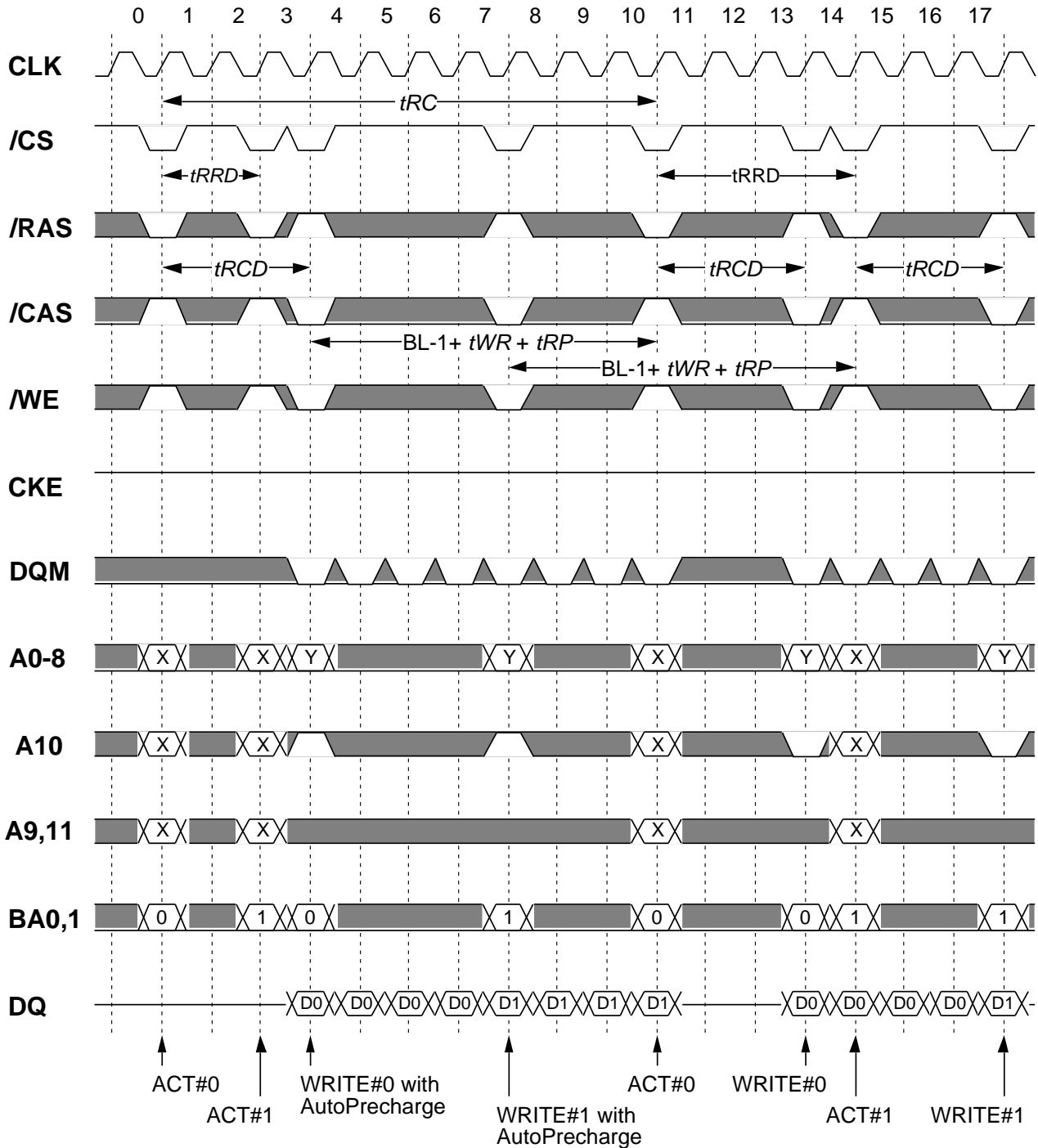


*Italic parameter* indicates minimum case

**M5M4V64S30ATP-8A,-8L,-8, -10L, -10**

64M (4-BANK x 2097152-WORD x 8-BIT) Synchronous DRAM

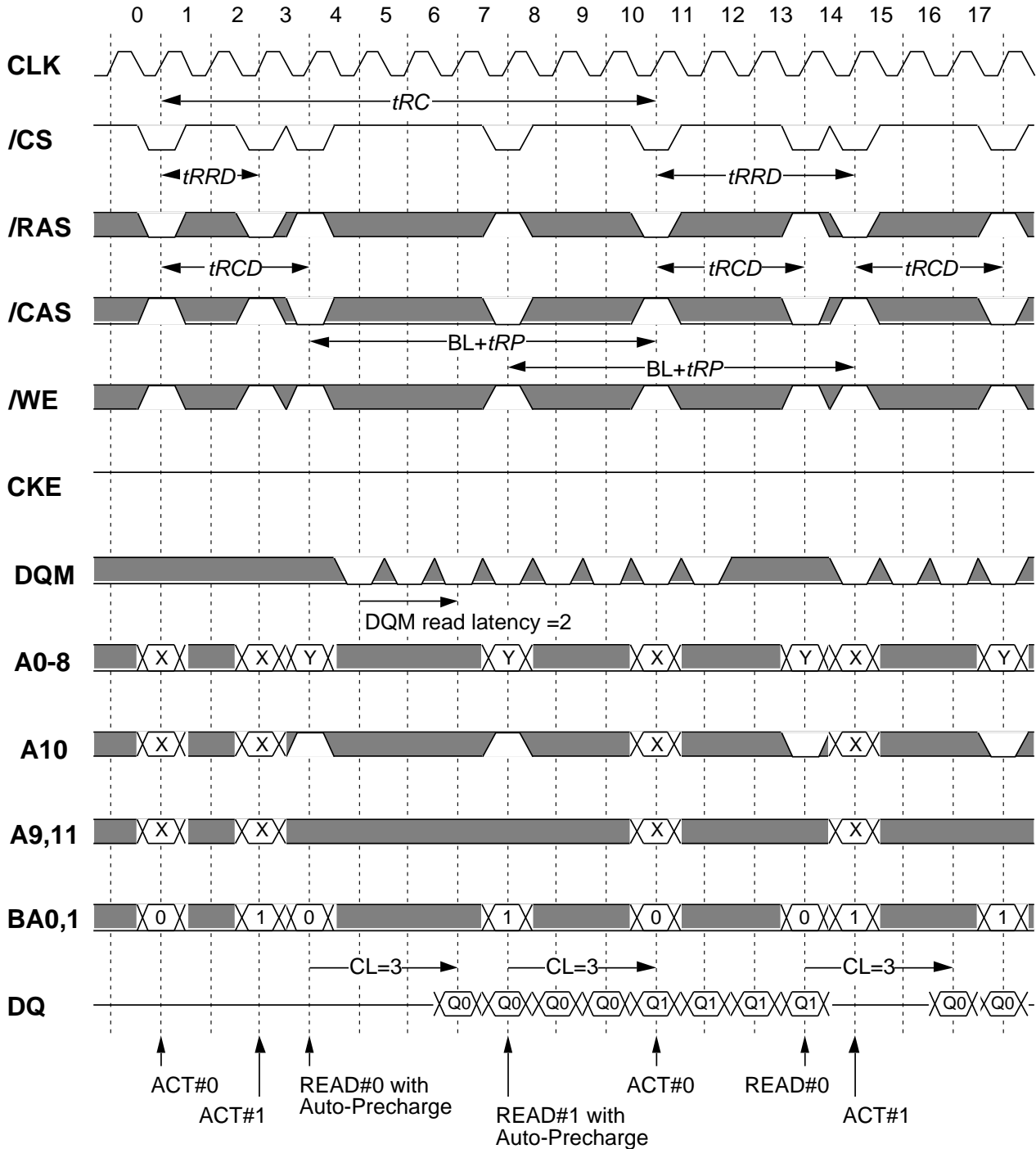
**Burst Write (multi bank) with Auto-Precharge @BL=4**



*Italic parameter* indicates minimum case

**M5M4V64S30ATP-8A,-8L,-8, -10L, -10**  
64M (4-BANK x 2097152-WORD x 8-BIT) Synchronous DRAM

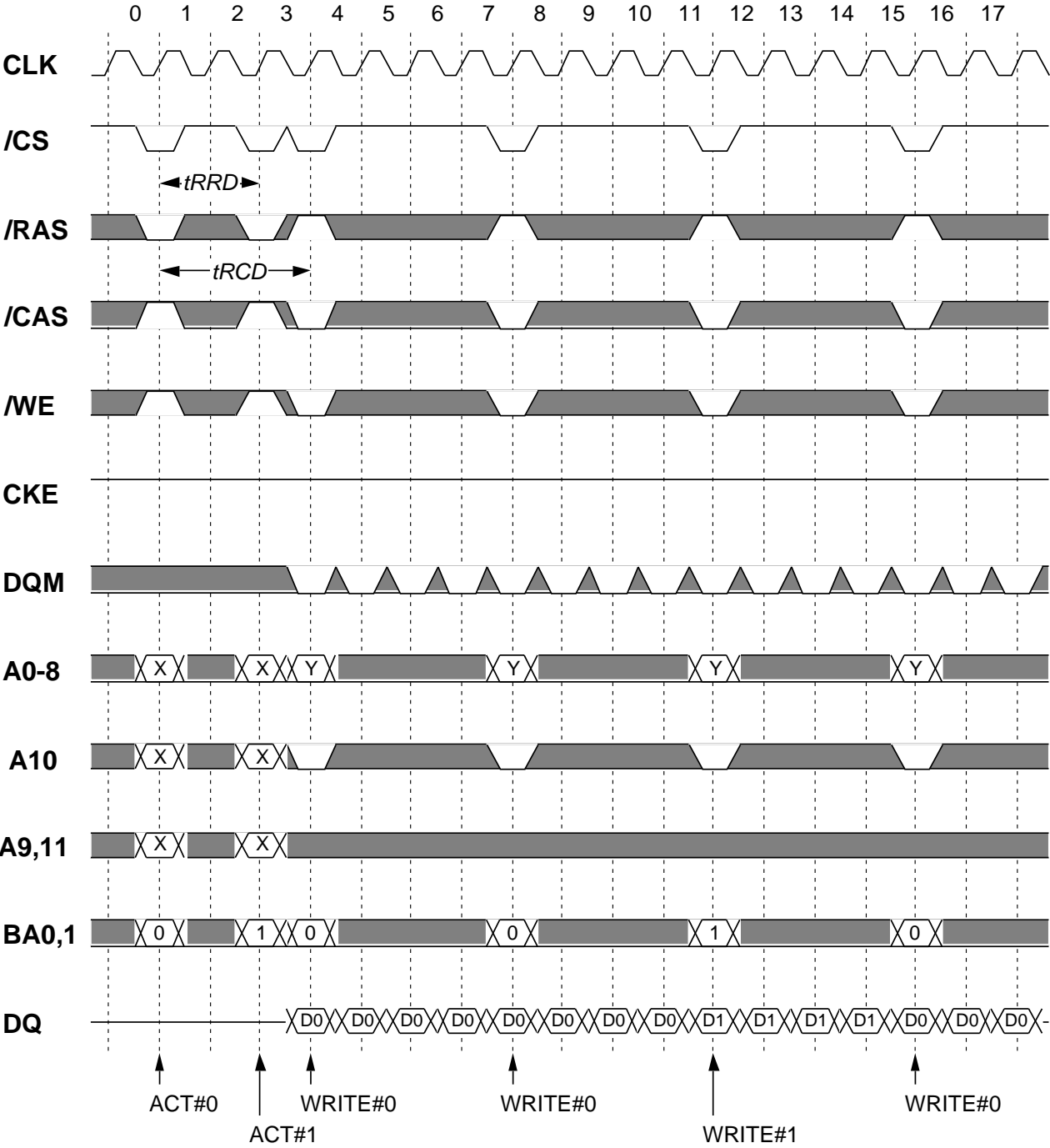
**Burst Read (multiple bank) with Auto-Precharge @BL=4 CL=3**



*Italic parameter* indicates minimum case

**M5M4V64S30ATP-8A,-8L,-8, -10L, -10**  
64M (4-BANK x 2097152-WORD x 8-BIT) Synchronous DRAM

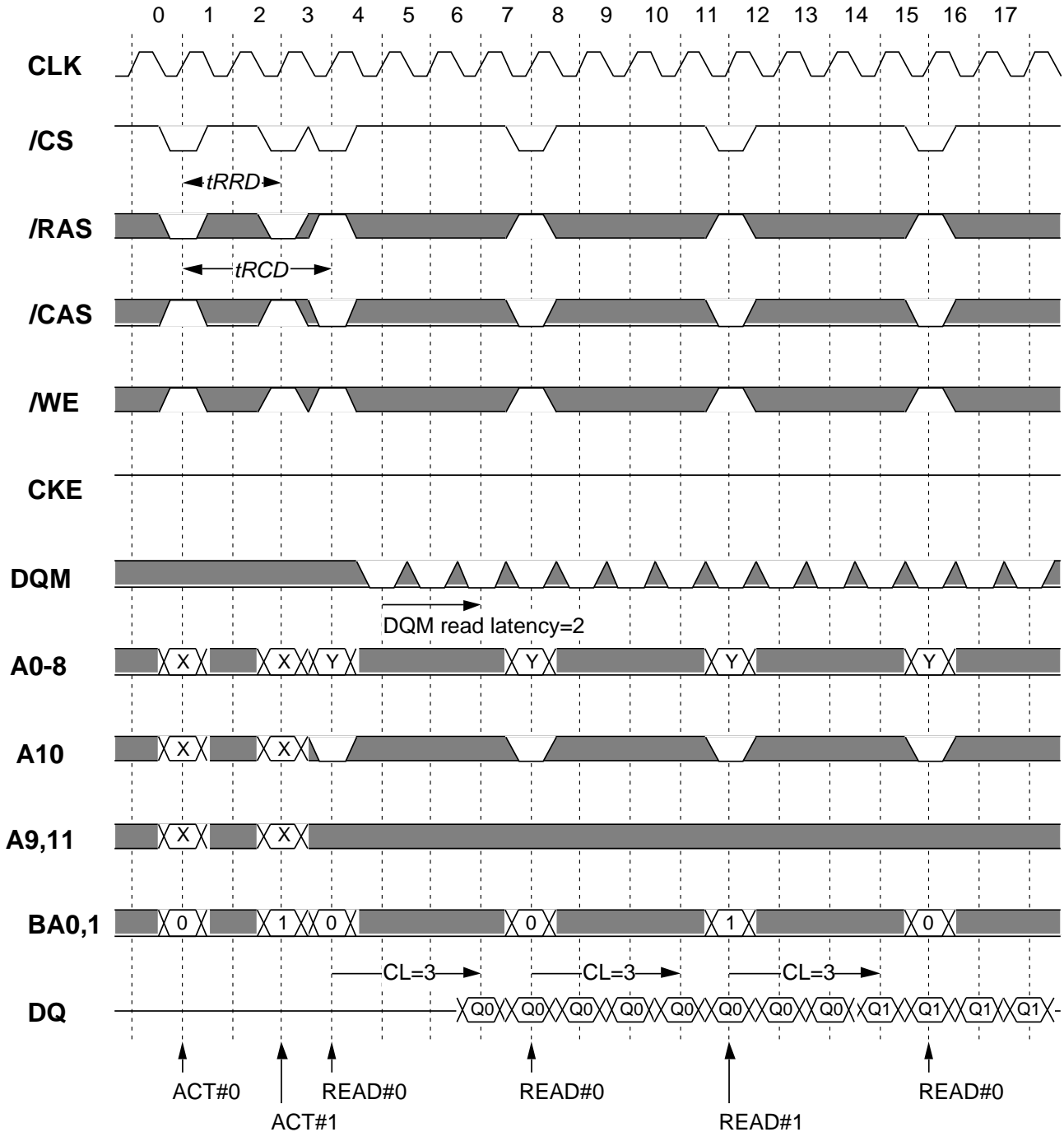
**Page Mode Burst Write (multi bank) @BL=4**



*Italic parameter* indicates minimum case

**M5M4V64S30ATP-8A,-8L,-8, -10L, -10**  
64M (4-BANK x 2097152-WORD x 8-BIT) Synchronous DRAM

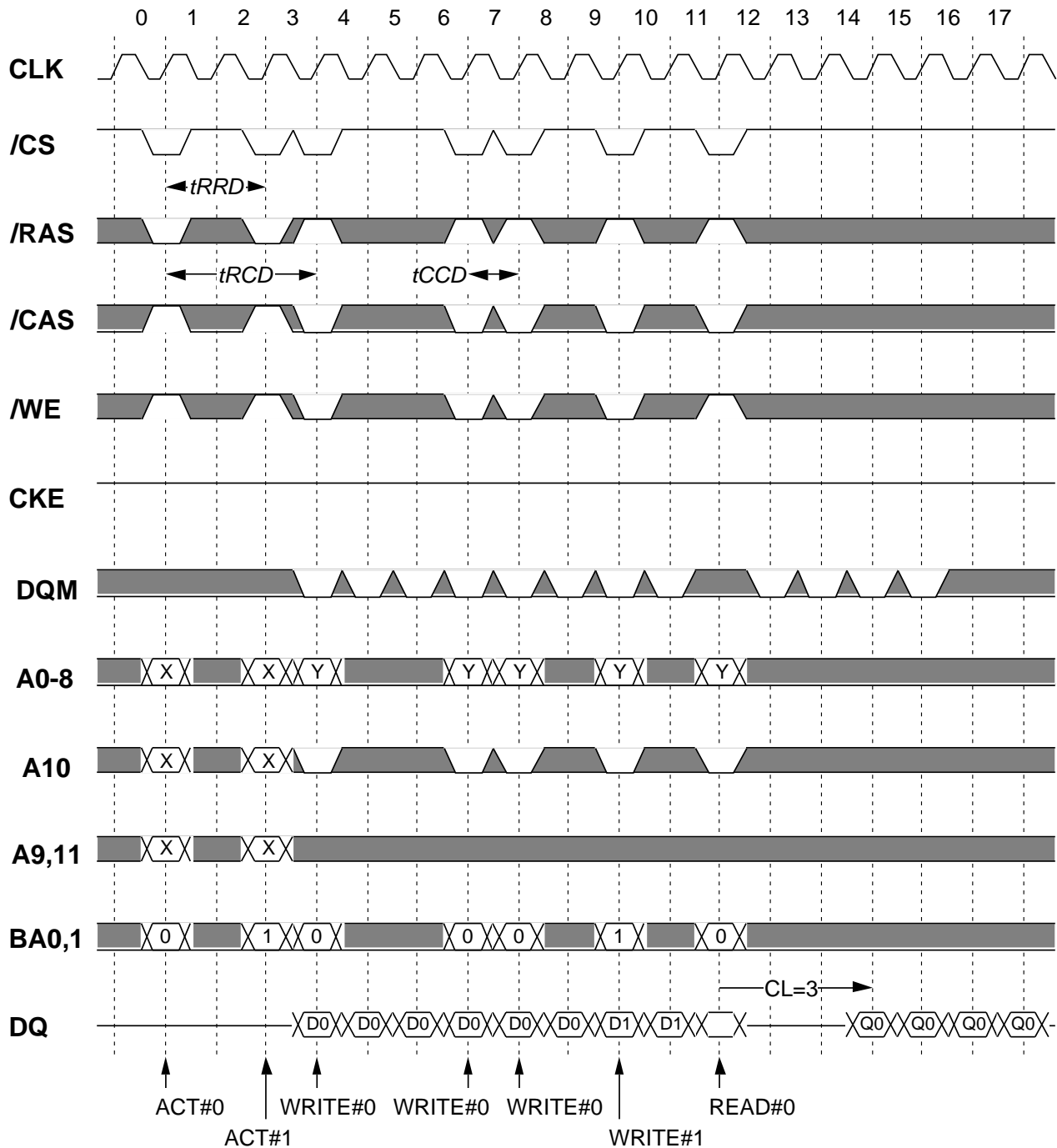
**Page Mode Burst Read (multi bank) @BL=4 CL=3**



*Italic parameter* indicates minimum case

**M5M4V64S30ATP-8A,-8L,-8, -10L, -10**  
64M (4-BANK x 2097152-WORD x 8-BIT) Synchronous DRAM

**Write Interrupted by Write / Read @BL=4**



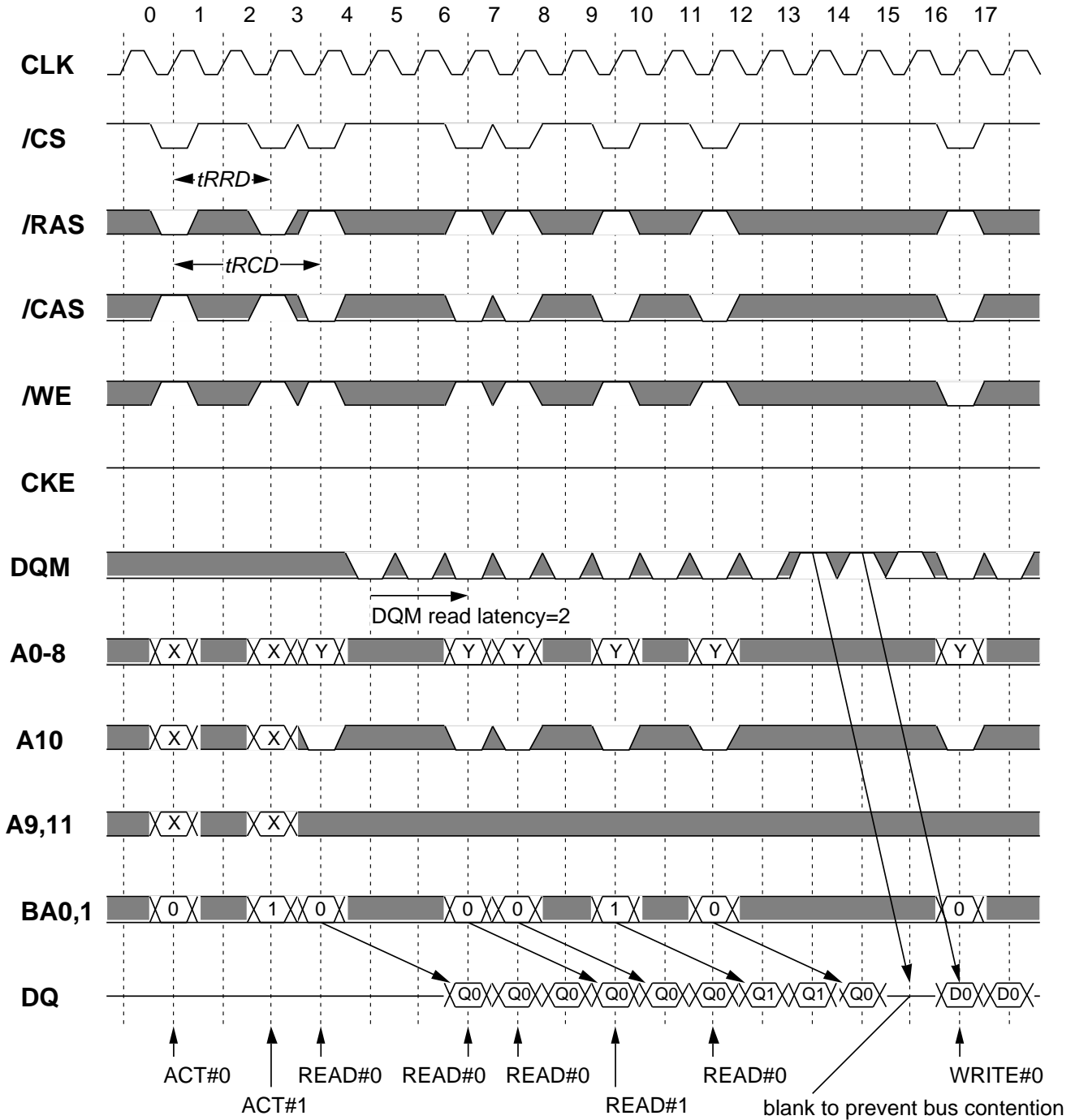
Burst Write can be interrupted by Write or Read of any active bank.

*Italic parameter* indicates minimum case



**M5M4V64S30ATP-8A,-8L,-8, -10L, -10**  
64M (4-BANK x 2097152-WORD x 8-BIT) Synchronous DRAM

**Read Interrupted by Read / Write @BL=4 CL=3**

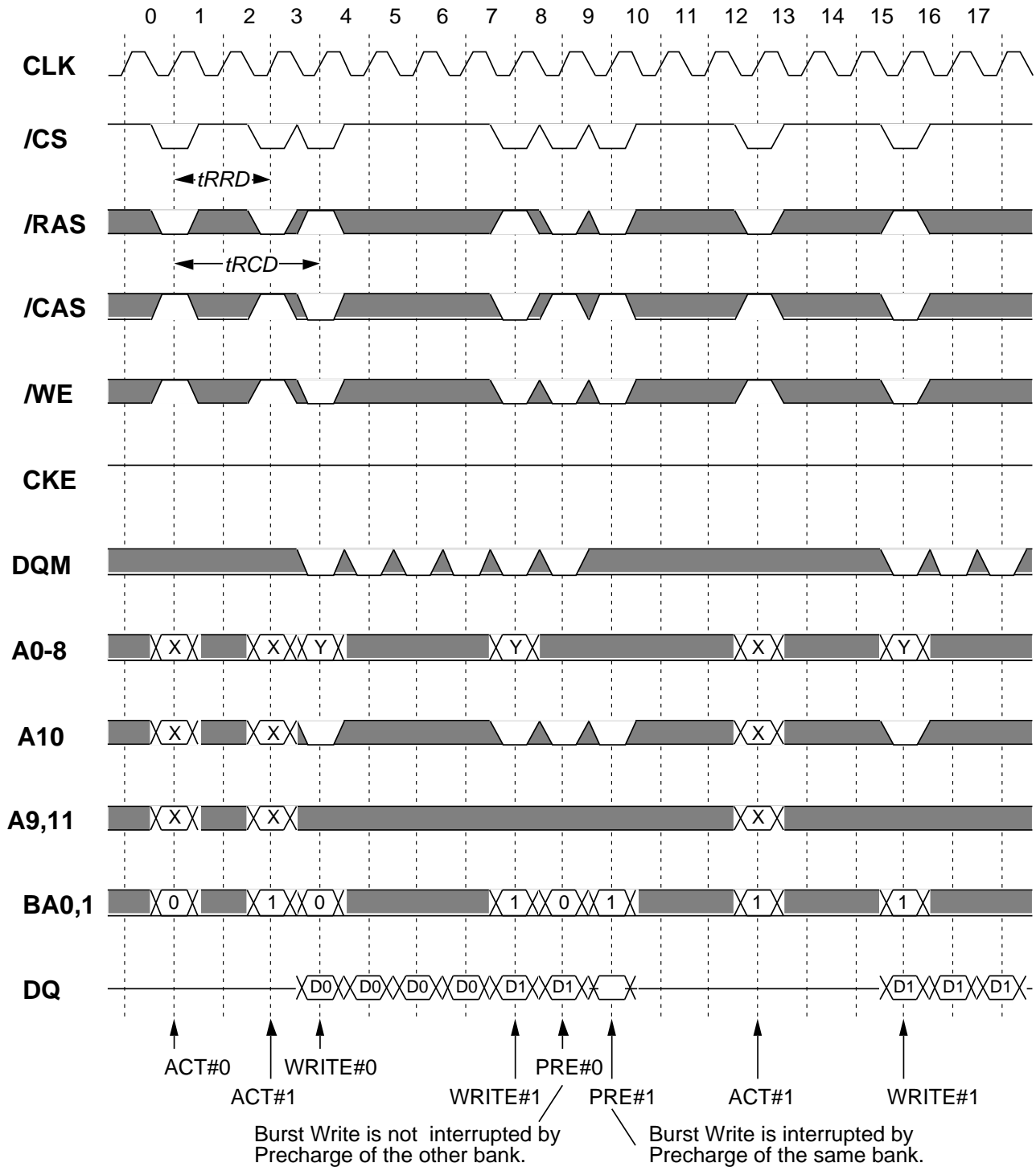


Burst Read can be interrupted by Read or Write of any active bank.

*Italic parameter* indicates minimum case

**M5M4V64S30ATP-8A,-8L,-8, -10L, -10**  
64M (4-BANK x 2097152-WORD x 8-BIT) Synchronous DRAM

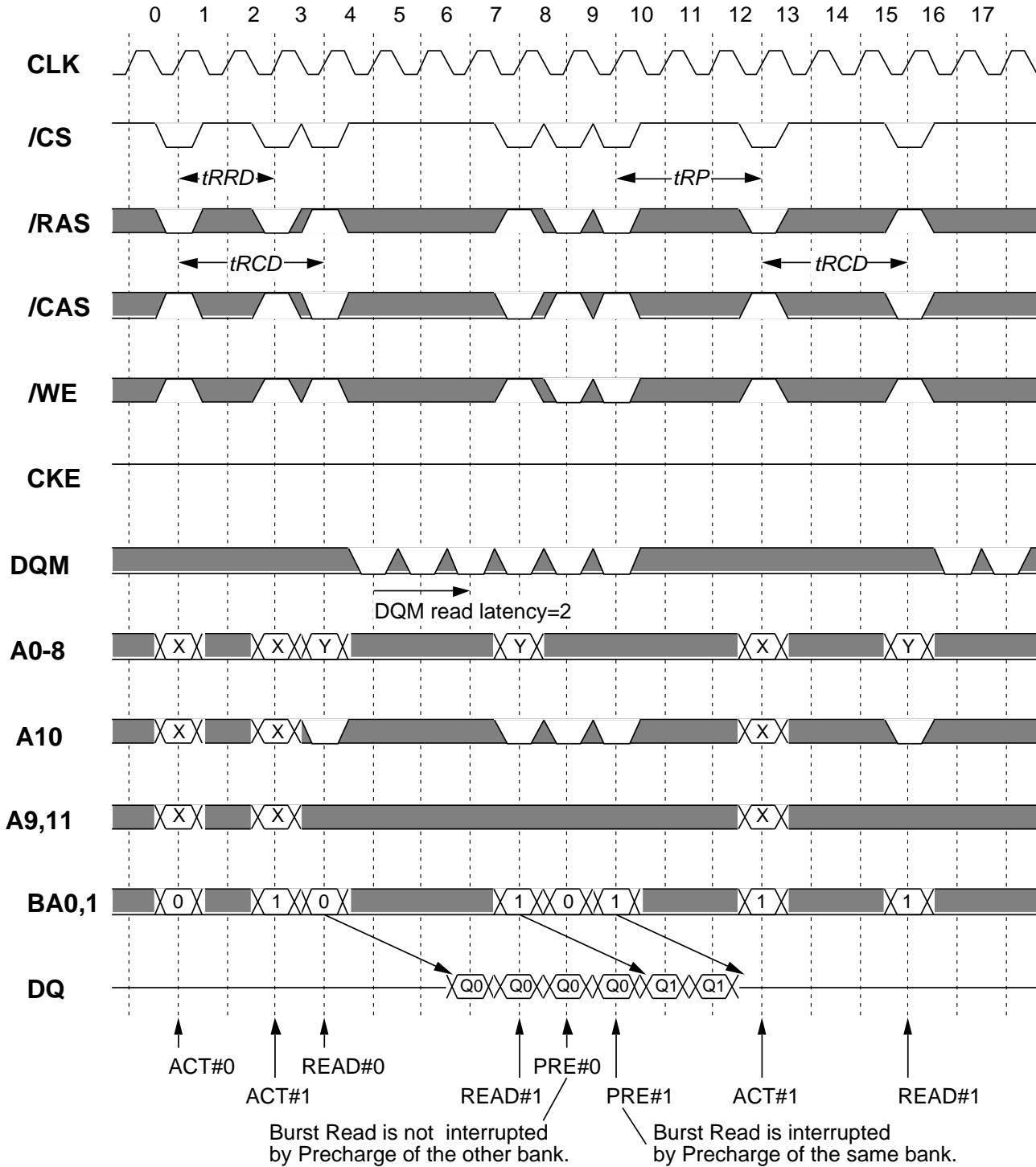
**Write Interrupted by Precharge @BL=4**



*Italic parameter* indicates minimum case

**M5M4V64S30ATP-8A,-8L,-8, -10L, -10**  
64M (4-BANK x 2097152-WORD x 8-BIT) Synchronous DRAM

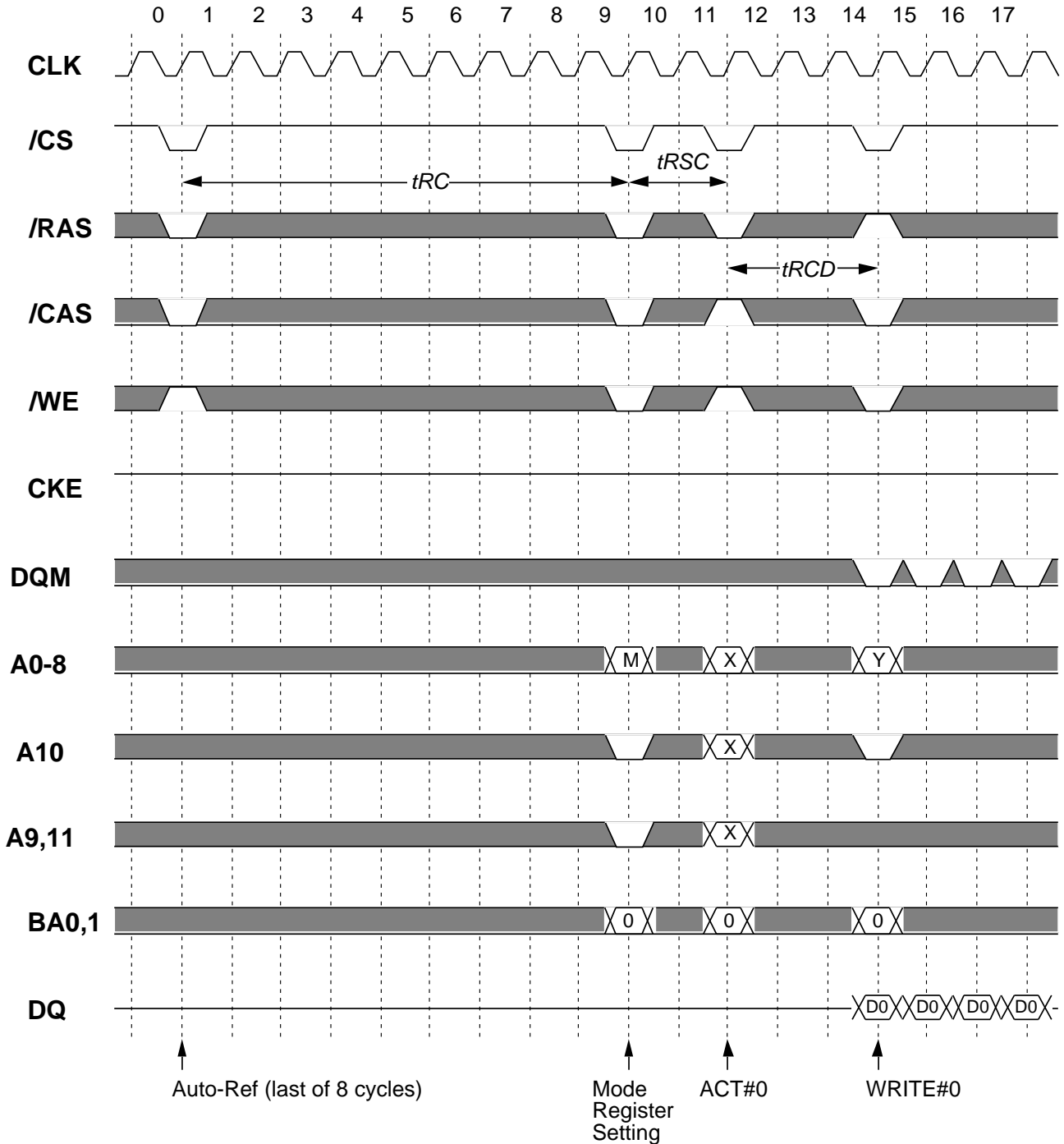
**Read Interrupted by Precharge @BL=4 CL=3**



*Italic parameter* indicates minimum case

**M5M4V64S30ATP-8A,-8L,-8, -10L, -10**  
64M (4-BANK x 2097152-WORD x 8-BIT) Synchronous DRAM

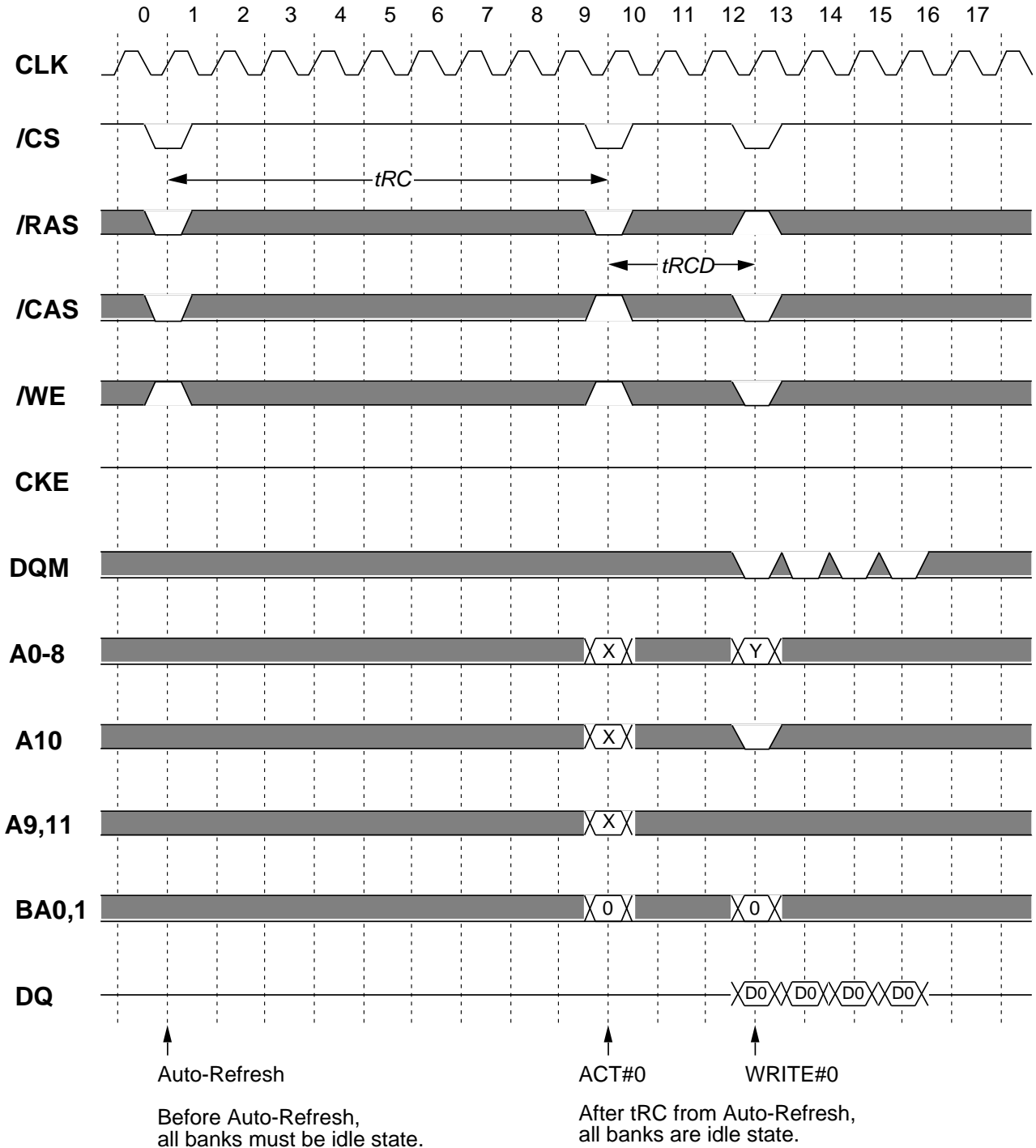
**Mode Register Setting**



*Italic parameter* indicates minimum case

**M5M4V64S30ATP-8A,-8L,-8, -10L, -10**  
64M (4-BANK x 2097152-WORD x 8-BIT) Synchronous DRAM

**Auto-Refresh @BL=4**

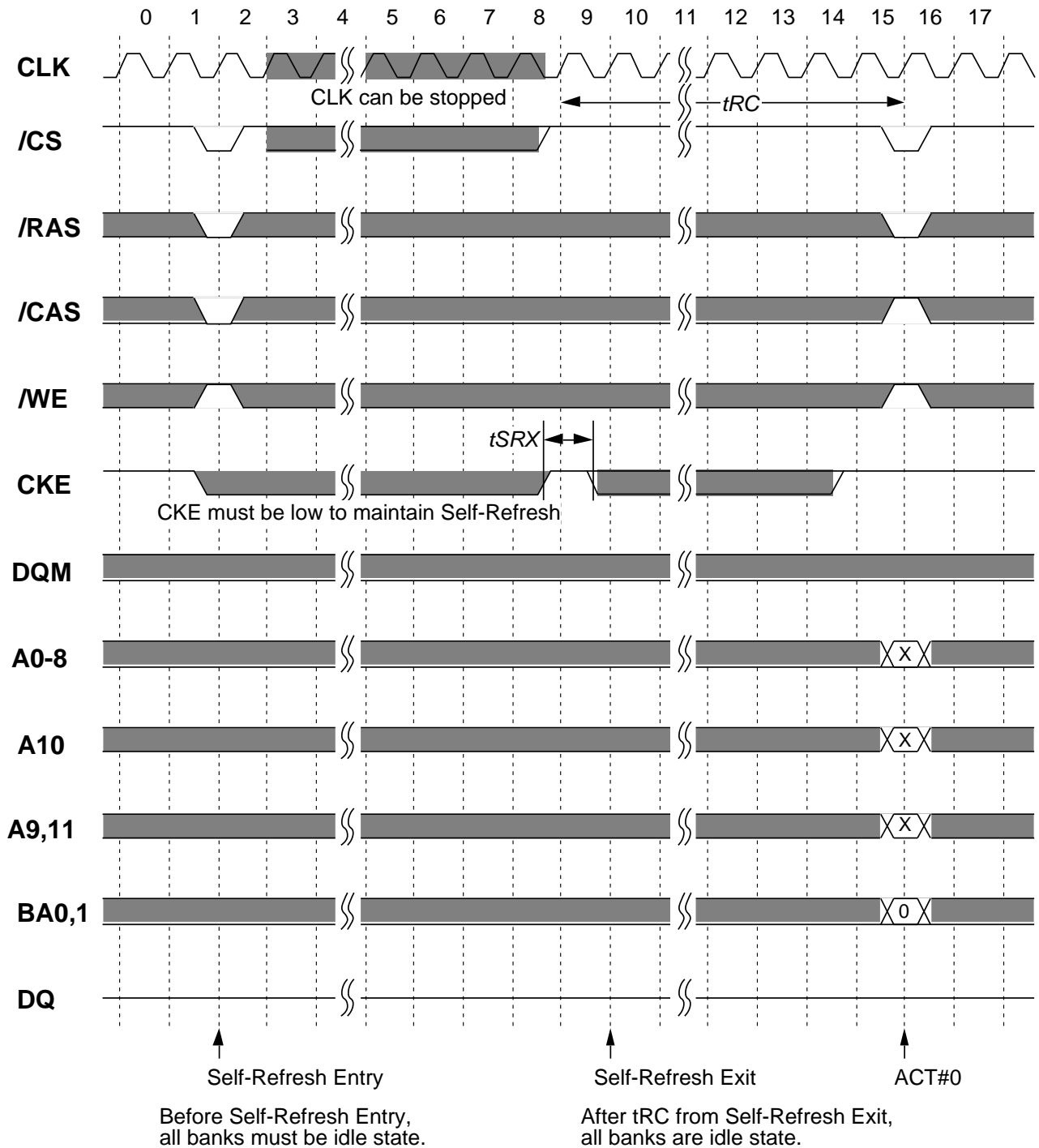


*Italic parameter* indicates minimum case

# M5M4V64S30ATP-8A,-8L,-8, -10L, -10

64M (4-BANK x 2097152-WORD x 8-BIT) Synchronous DRAM

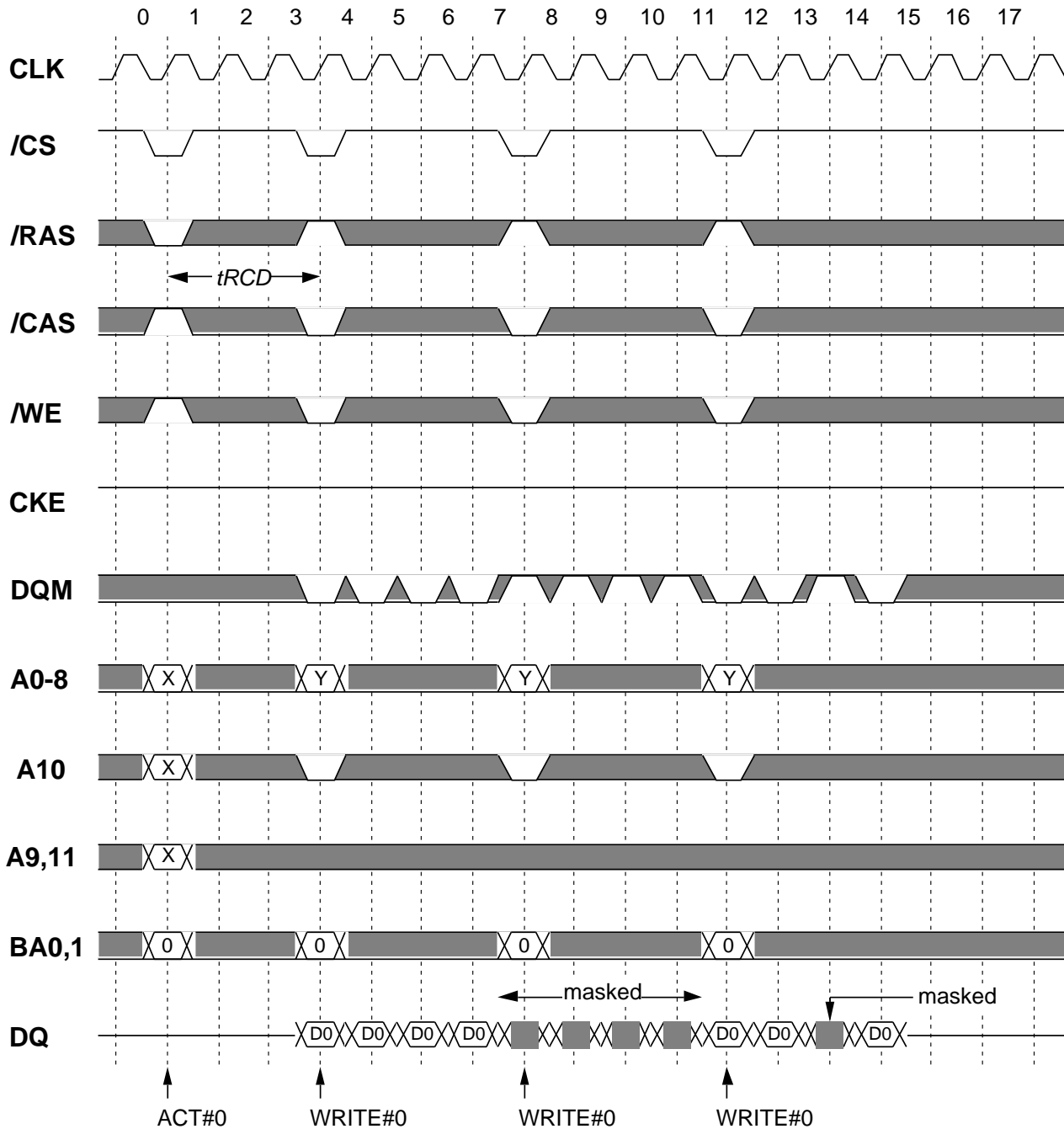
## Self-Refresh



*Italic parameter* indicates minimum case

**M5M4V64S30ATP-8A,-8L,-8, -10L, -10**  
64M (4-BANK x 2097152-WORD x 8-BIT) Synchronous DRAM

**DQM Write Mask @BL=4**

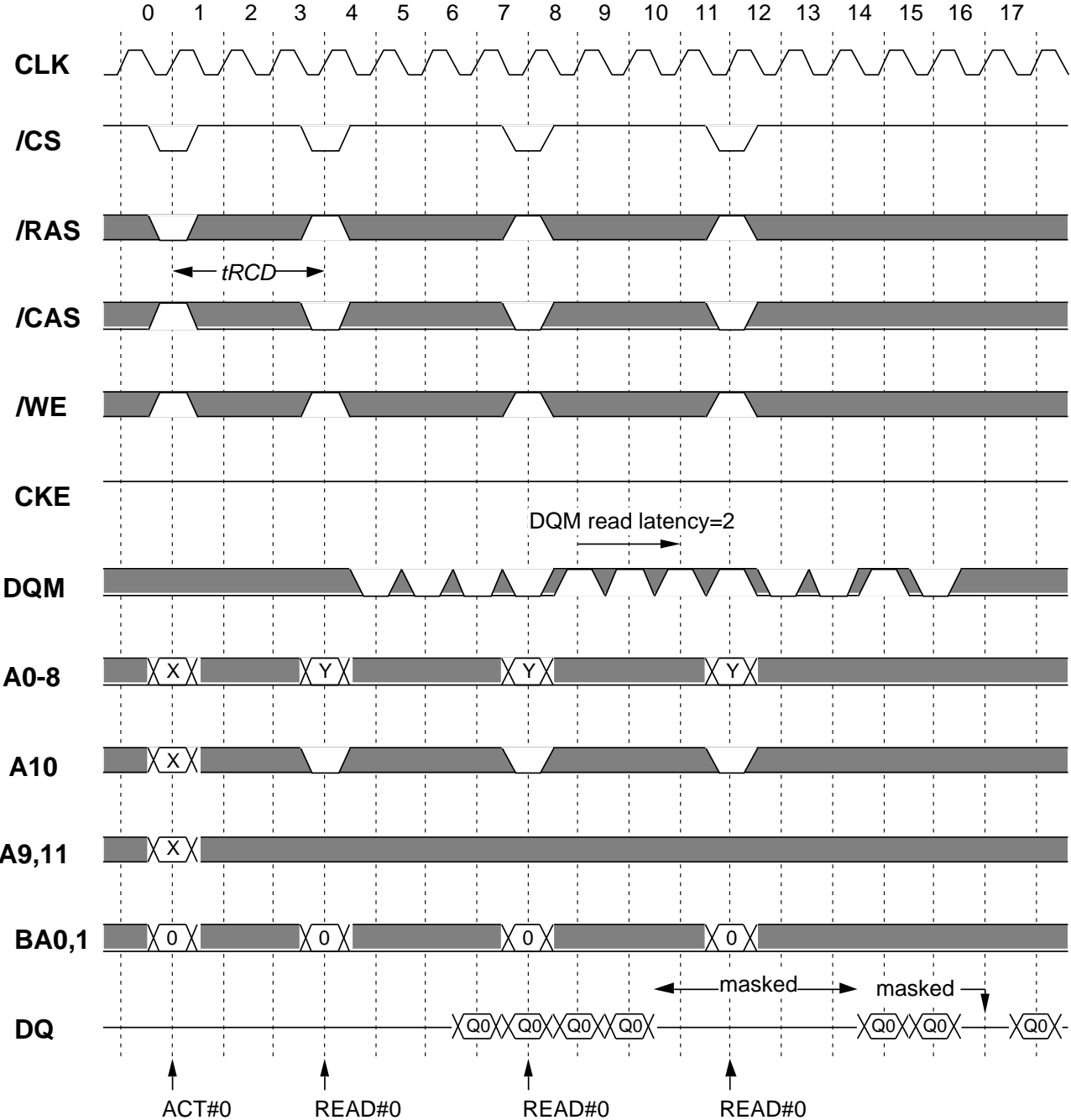


*Italic parameter* indicates minimum case

# M5M4V64S30ATP-8A,-8L,-8, -10L, -10

64M (4-BANK x 2097152-WORD x 8-BIT) Synchronous DRAM

## DQM Read Mask @BL=4 CL=3

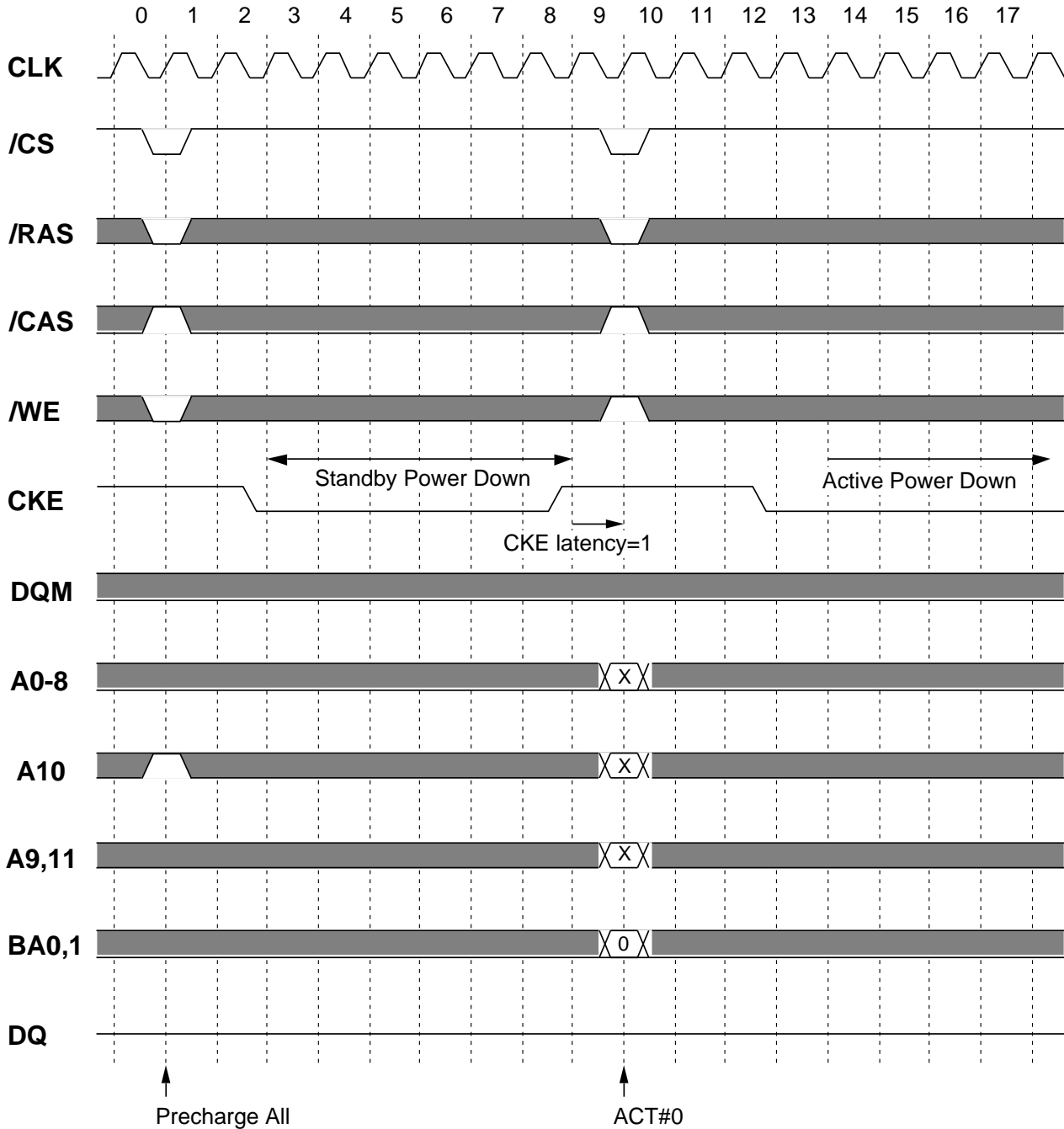


*Italic parameter* indicates minimum case



**M5M4V64S30ATP-8A,-8L,-8, -10L, -10**  
64M (4-BANK x 2097152-WORD x 8-BIT) Synchronous DRAM

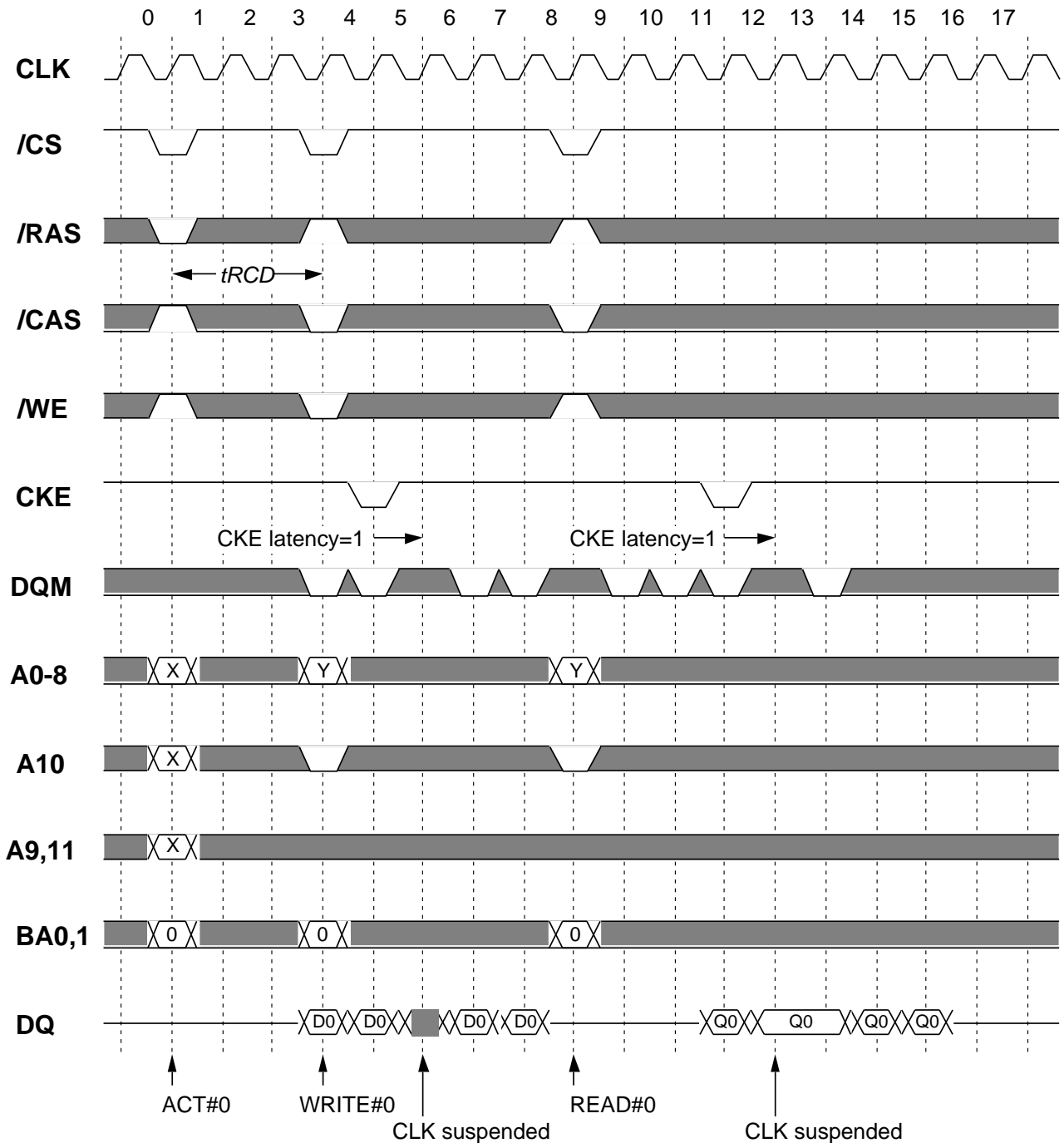
**Power Down**



*Italic parameter* indicates minimum case

**M5M4V64S30ATP-8A,-8L,-8, -10L, -10**  
64M (4-BANK x 2097152-WORD x 8-BIT) Synchronous DRAM

**CLK Suspend @BL=4 CL=3**



*Italic parameter* indicates minimum case

## M5M4V64S30ATP-8A,-8L,-8, -10L, -10 64M (4-BANK x 2097152-WORD x 8-BIT) Synchronous DRAM

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