MN6152U

PLL LSI with Built-In Prescaler

■ Overview

The MN6152U is a CMOS LSI for a phase-locked loop (PLL) frequency synthesizer with serial data input.

It consists of a two-coefficient prescaler, variable frequency divider, phase comparator, and charge pump.

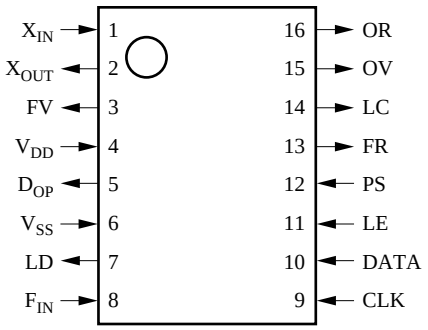
It offers high-speed operation on a low power supply voltage (1.8 to 2.5 V) and low power consumption (5 mW for V_{DD}=2.0 V, F_{IN}=100 MHz).

Other features include intermittent operation by the power save (PS) control signal and high-speed pull-in that rapidly corrects the phase differences occurring at the start of operation.

■ Features

- Low power supply voltage: V_{DD}=1.8 to 2.5V
- Low power consumption: 5mW (V_{DD}=2.0V, F_{IN}=100MHz)
- High-speed operation: F_{IN}=175MHz
- Frequency dividing ratios in reference frequency dividing stage: 5 to 131,071
- Frequency dividing ratios in comparator stage: 272 to 262,143
- Lock detector output pin
- Two types of phase comparator output
  - Internal charge pump output
  - Output for external charge pump
- Output monitor pins for both comparator and reference frequency dividing stages

■ Pin Assignment



(TOP VIEW)

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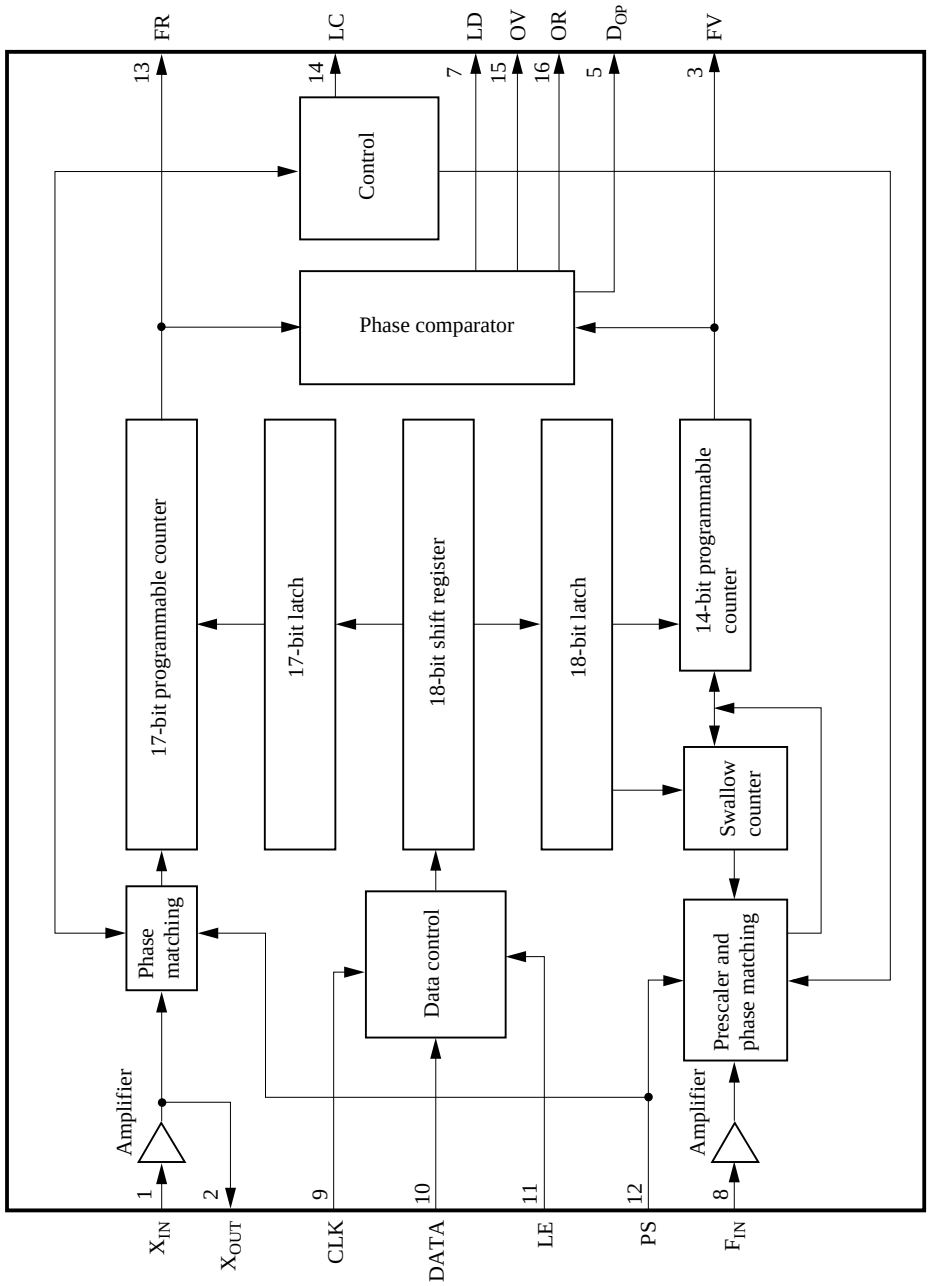
■ Block Diagram



■ Pin Descriptions

Pin No.	Symbol	Function Description
1	X_{IN}	Crystal oscillator connection pins: X_{IN} =Oscillator circuit input pin; X_{OUT}=Oscillator circuit output pin.
2	X_{OUT}	
3	FV	Frequency divider output signal in comparator stage. Phase comparator input monitor.
4	V_{DD}	Power supply
5	D_{OP}	Low-pass filter connection pin. Use a passive filter.
6	V_{SS}	Ground
7	LD	Phase comparator output pin: "H" level for locked; "L"level for unlocked.
8	F_{IN}	Frequency divider input pin in comparating stage.
9	CLK	Shift register clock input pin. The chip latches data at the rising edge of the CLK signal.
10	DATA	Shift register data input pin. The final two bits in the data select the write latch: "11" for R-latch; "01" for N-latch.
11	LE	Load enable signal input pin. This is the latch-write-enable signal. It is at "H" level for write.
12	PS	Power save control signal input pin. "H" level input starts the frequency divider and places the chip in operational mode. "L" level input places the chip in standby mode, which saves power. The chip switches the internal charge pump output to the H-z state and the loop is opened.
13	FR	Reference frequency divider output signal. Phase comparator input monitor.
14	LC	Charge pump control signal output pin. When frequency divider operation is stopped, this pin is at "L" level, the internal charge pump output is in the high-impedance state, and the loop is opened.
15	OV	Phase comparator output pin for external charge pump.
16	OR	

■ MN6152 Frequency Dividing Data Settings

The following formula shows frequency divider operation.

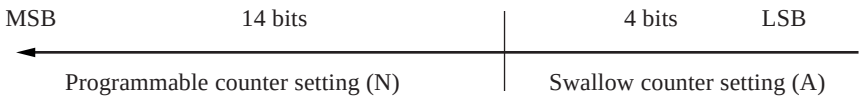
$F_{IN} = \{ (16 \times N) + A \} \times (X_{IN} \div R)$

where

F_{IN} : VCO output frequency
N : Setting for 14-bit programmable counter on comparator side
A : Setting for 4-bit swallow counter on comparator side
X_{IN} : Reference oscillator frequency
R : Setting for 17-bit programmable counter on reference side

Note that N should be greater than A.

- N-Side Latch Data



■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Power supply voltage	V_{DD}	– 0.3 to +3.5	V
Input pin voltage	V_I	V_{SS} – 0.3 to V_{DD} +0.3	
Output pin voltage	V_O	V_{SS} – 0.3 to V_{DD} +0.3	
Power dissipation	P_D	20	mW
Operating ambient temperature	T_{opr}	–20 to +60	˚C
Storage temperature	T_{stg}	–55 to +125	

■ Operating Conditions

V_{SS}=0V, Ta=–20 to +60˚C

Parameter	Symbol	Test Conditions	min	typ	max	Unit
Power supply voltage	V_{DD}		1.8	2.0	2.5	V

■ Electric Characteristics

V_{DD}=2V, Ta=–20 to +60˚C

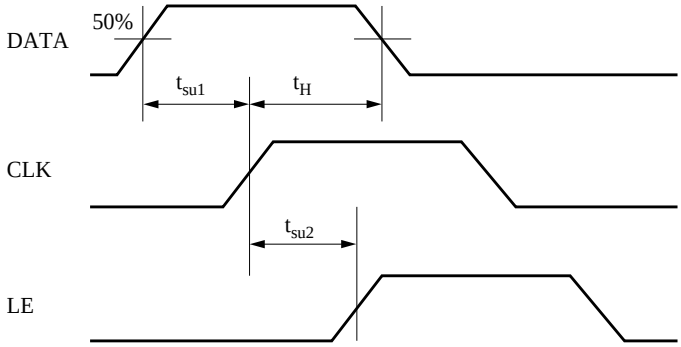
Parameter	Symbol	Test Conditions	min	typ	max	Unit
Power supply voltage	I_{DD}	F_{IN}=100MHz, X_{IN}=20MHz, PS="H"			2.5	mA
	I_{Dstop}	PS ="L" (at power save operation)			10	µA
Input Pins CLK, DATA, LE, and PS	V_{DD}=1.8 to 2.5V					
"H" level input voltage	V_{IH}		V_{DD} – 0.2		V_{DD}	V
"L" level input voltage	V_{IL}		V_{SS}		0.2	
Input leakage current	I_{LI}				±1.0	µA
Input Pin F_{IN} V_{DD}=1.8 to 2.5V						
Input voltage	V_{IN}		0.4			V_{p-p}
Input current	I_{IF}	Pull-up resistor present (PS="L")	–100			µA
Input leakage current	I_{LIF}	V_{IN}=0 or 2V (PS="H")			±20	µA
Maximum operating frequency	F_{INMAX}	V_{IN}=0.4 V_{p-p}	175			MHz
Minimum operating frequency	F_{INMIN}	V_{IN}=0.4 V_{p-p}			10	MHz
Input Pin X_{IN} V_{DD}=1.8 to 2.5V						
Input voltage	V_{IN}		0.4			V_{p-p}
Input current	I_{IX}	Pull-up resistor present (PS="L")	2.5			mA
Input leakage current	V_{LIX}	V_{IN}=0 or 2V			5.0	µA
Maximum operating frequency	X_{INMAX}	V_{IN}=0.4 V_{p-p}	20			MHz

■ Electrical Characteristics

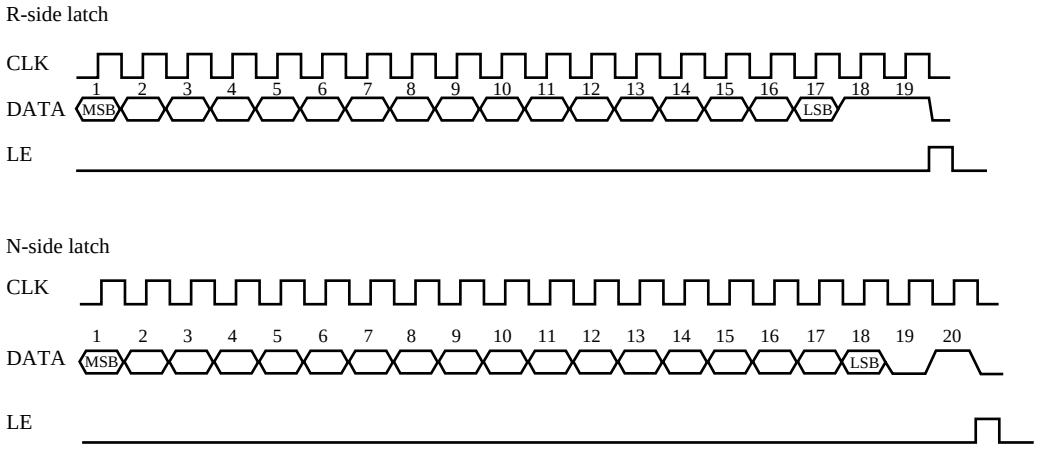
V_{DD}=2V, Ta=–20 to +60˚C

Parameter	Symbol	Test Condition	min	typ	max	Unit
Crystal Oscillator Pins X_{IN}, X_{OUT} V_{DD}=1.8 to 2.5V						
Crystal oscillator frequency	f_{Xtal}		20			MHz
Output Pins FV, FR, LC, OV V_{DD}=1.8 to 2.5V						
"H" level output voltage	V_{OH}	I_{OH}= –100µA	V_{DD}– 0.3		V_{DD}	V
"L" level output voltage	V_{OL}	I_{OL}= 100µA	V_{SS}		0.3	
Output Pin X_{OUT} V_{DD}=1.8 to 2.5V						
"H" level output voltage	V_{XOH}	I_{XOH}= –500µA	V_{DD}– 0.3		V_{DD}	V
"L" level output voltage	V_{XOL}	I_{XOL}= 500µA	V_{SS}		0.3	
Output Pin D_{OP} V_{DD}=1.8 to 2.5V						
"H" level output voltage	I_{DOH}	V_{Dop}=1.6V	–100			µA
"L" level output voltage	I_{DOL}	V_{Dop}=0.4V	100			
Output Pin OR V_{DD}=1.8 to 2.5V						
"L" level output voltage	I_{ORL}	V_{OR}=0.4V	100			µA
Setup time *1	t_{sul}		500			ns
	t_{su2}		500			ns
Hold time *1	t_H		500			ns

Note*1: The following timing chart shows the setup and hold times.



■ Frequency Divider Setting



- Input the data MSB first.
- The data is read at the rising edges of the CLK signal.
- Drive the LE pin at "L" level when writing data.

Usage Note

Be particularly careful with this product as it is more sensitive on the static electricity damage than most of our other products.

■ Package Diemnsions (Unit: mm)

SSOP016-P-0225