WaveArtist™ 010, WaveArtist™ 020, and WaveArtist™ 030 Audio System Devices

Introduction

The Rockwell WaveArtist™ 010 (RWA010), WaveArtist™ 020 (RWA020), and WaveArtist™ 030 (RWA030) are audio system devices in small, low profile, PQFP/TQFP packages. These devices provide increasing functionality from FM synthesis (RWA010), to FM and wavetable synthesis (RWA010 and RWA020), to FM and high quality music wavetable synthesis (RWA010 and RWA030). (See Table 1.)

The RWA010 Audio System Controller and Codec supports FM synthesis, 16-bit stereo audio with simultaneous record and playback, and ISA bus Plug-and-Play (PnP) interface with 16-bit (RWA010) or 12-bit (RWA011) address for cost effective, expandable audio and audio/modem system designs. The RWA010 is also compatible with DOS applications that use Sound Blaster Pro, Yamaha OPL3, AdLib, and MPU-401 interfaces. Also supported is a game port with internal timers, and for the RWA011 only, an enhanced IDE CD-ROM interface. General MIDI compatible wavetable synthesis is provided by adding the RWA020 Wavetable Synthesizer (Figure 1) or the RWA030 Music Processor (Figure 2). Unless otherwise noted, all references to the RWA010 also include the RWA011. The RWA010 is packaged in a 144-pin TQFP.

The RWA010, when used with a Rockwell modem, provides seamless integration of high speed data/fax modem, voice/audio, simultaneous voice and data (SVD), and speakerphone functions.

The RWA020 Wavetable Synthesizer, in an 80-pin PQFP, supports lowest cost wavetable designs in either RWA010 or standalone interface configuration. It connects to the RWA010 or other system controller, the host bus, and a 1MB wavetable ROM.

The RWA030 Music Processor, featuring Audio by Kurzweil and special audio effects, in an 80-pin PQFP, supports high quality sound designs in either RWA010 or standalone interface configuration. It connects to the RWA010 or other controller, a 2MB or 1MB wavetable ROM, and an optional downloadable sound sample DRAM (up to 8MB).

Host software, compatible with the Windows Sound System (WSS), is provided for Windows 95, Windows 3.1x, Windows NT, and DirectSound environments. A software utility is also available to configure the PnP interface in an MS-DOS environment.

FCC part 15 and part 68 approved reference hardware designs are available.

Features

- RWA010 Audio System Controller and Codec
  - 16-bit stereo audio in a single mixed-signal device
    - * 16-bit delta sigma codec with >80 dB SNR
    - * Sound Blaster Pro compatible
    - * Simultaneous (full-duplex) record and playback
    - * 8-bit and 16-bit PCM sample record and playback from 4 kHz to 44.1 kHz
    - * Digital sample rate conversion with 0.7 Hz resolution
    - * Integrated OPL3/OPL2 and AdLib compatible FM synthesis with no external DAC required
    - * 5 external analog input channels (4 stereo, 1 mono)
    - * Independent left and right channel mixers each with 5 external inputs and 1 internal input (digitally summed FM, optional wavetable, and PCM signals)
    - * 2 external analog output channels (1 stereo, 1 mono)
    - * Uses single crystal oscillator
  - Integrated hardware interfaces
    - * MPU-401 MIDI UART compatible
    - * Enhanced IDE CD-ROM compatible (RWA011)
    - * Joystick with internal timers (game port compatible)
    - * ISA bus PnP interface
  - Programmable PnP resource data
- RWA020 Wavetable Synthesizer in 80-pin PQFP
  - General MIDI compatible wavetable synthesis supports 32 voices at 44.1 KHz
  - Interface to 1MB wavetable ROM
- RWA030 Music Processor in 80-pin PQFP
  - General MIDI compatible wavetable synthesis supports 32 voices at 44.1 KHz
  - Basic effects for reverb, chorus, and 3D spatialization
  - Treble and bass equalization
  - Interface to 2MB or 1MB wavetable ROM
  - Interface to sound sample DRAM (up to 8MB)
- Low profile, small footprint packages
  - RWA010: 144-pin TQFP
  - RWA020 and RWA030: 80-pin PQFP
- Power management
- Applications
  - Integrated audio/telephony cards
  - Motherboards, notebooks, add-on cards
  - PC audio/games
  - Windows Sound System (WSS) and DirectSound

Table 1. Models and Functions

Functions	Required Devices		
	RWA010 (Note 1)/ RWA011 (Note 2)	RWA020 and RWA021 ROM[3]	RWA030, and RWA031/RWA032 ROM[4]
FM Synthesis	X	—	—
Wavetable Synthesis	—	X	—
High Quality Wavetable Synthesis	—	—	X
3D Spatialization	—	—	X
Effects (Reverb and Chorus)	—	—	X
Equalization (Treble and Bass)	—	—	X

Notes:

1. RWA010 supports 16-bit PnP address but not CD-ROM interface.
2. RWA011 supports 12-bit PnP address and CD-ROM interface.
3. RWA021 is the optional 1MB wavetable ROM for the RWA020.
4. RWA031/RWA032 is the optional 1MB/2MB wavetable ROM for the RWA030.

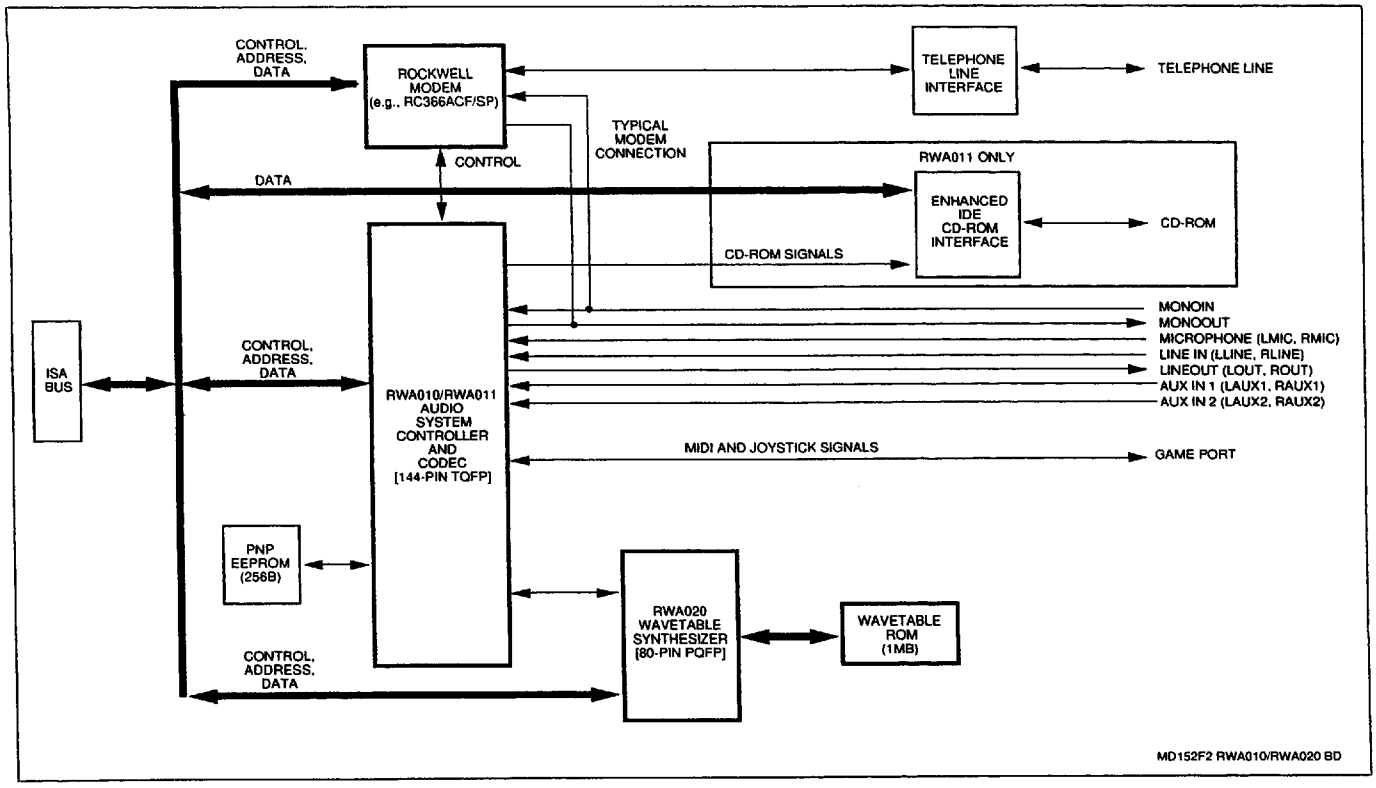

Figure 1. RWA010 with RWA020 Block Diagram

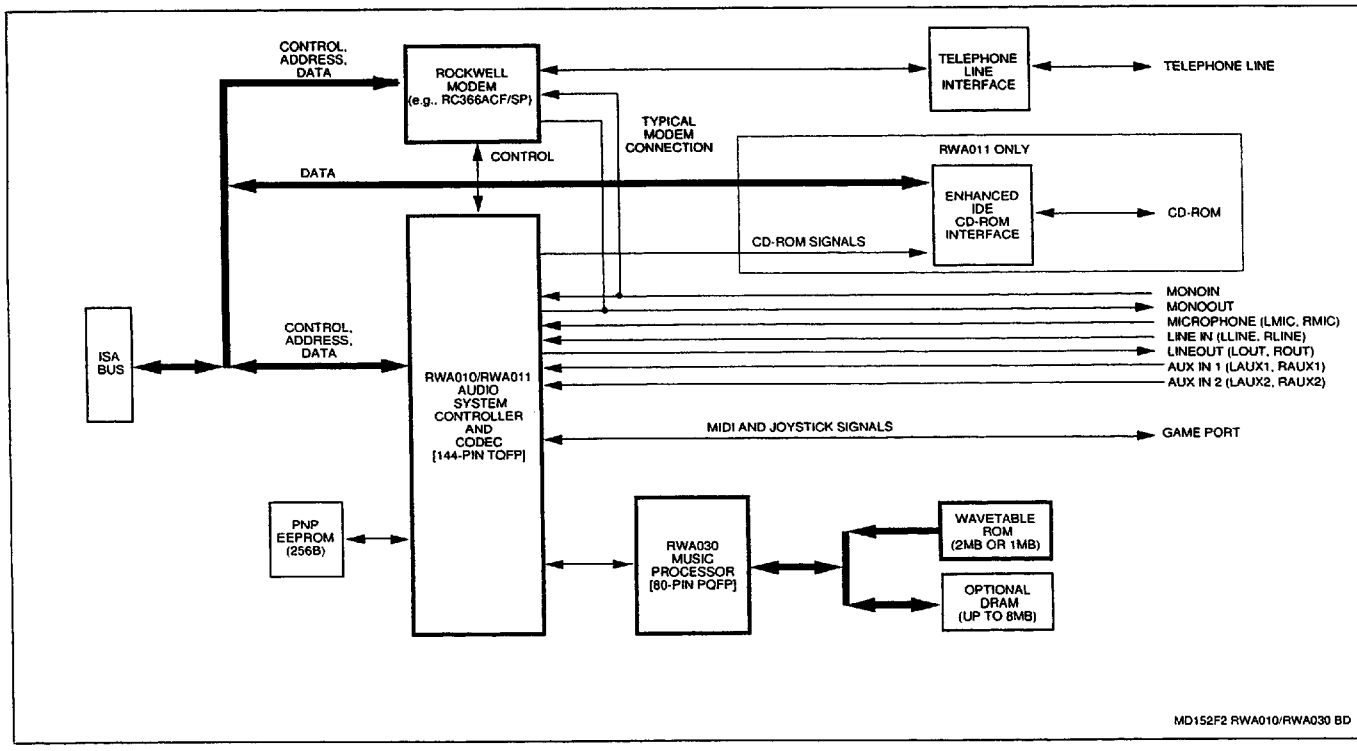

Figure 2. RWA010 with RWA030 Block Diagram

RWA010 Description

General

Sample Rate Conversion

Analog inputs and outputs are sampled at 44.1 kHz. The internal sample rate converter converts PCM samples to sample rates ranging from 4 kHz to 44.1 kHz.

The sample rate converter eliminates the need for an external DAC for the FM synthesis. It also allows the use of a single crystal to support all PCM sample rates.

FM Synthesis

The internal OPL3 and OPL2 compatible FM synthesis engine can operate in either 2-operator or 4-operator mode.

Address, data, and status registers are provided for compatibility with the AdLib/Sound Blaster Pro interfaces.

Stereo Codec/Mixer

An integrated 16-bit delta sigma stereo codec simultaneously mixes, records, and plays with high fidelity.

The record multiplexer for the stereo ADC input selects from four external stereo inputs, one external mono input, or the internal mixer. The mixer combines the external inputs into one stereo input for the record multiplexer.

For playback, separate stereo and mono outputs are provided. The PCM samples are digitally mixed with FM and wavetable synthesizer samples, then converted to analog outputs.

Volume controls are provided on all input and output paths.

Host Software

Windows Sound System (WSS) compatible recording and playback of 16-bit and 8-bit PCM audio is supported in Rockwell-provided host driver software which controls the WaveArtist using the WaveArtist command/status registers.

Wavetable Synthesis (RWA020 Option)

The RWA020 supports 32-voice polyphony General MIDI wavetable synthesis at 44.1 kHz. An external 1MB ROM is used to store the wavetable sounds.

Music Processor (RWA030 Option)

The RWA030 supports 32-voice polyphony General MIDI wavetable synthesis at 44.1 kHz. It provides several basic audio effects, including reverb, chorus, and 3D sound spatialization. Additionally, treble/bass equalization can be performed on all external inputs [Microphone, Line In, Aux In 1 (CD-ROM) and Aux In 2 (modem)] as well as FM and wavetable synthesis signals. An external 2MB or 1MB ROM is used to store the wavetable sounds.

Sound samples can be loaded into optional external DRAM and played back with the internal synthesis engine. This interface also supports multiple hardware static buffers, allowing games written for DirectSound to playback sounds more efficiently.

Host Hardware and Logical Device Interfaces

Host Full-Duplex Operation

Two DMA channels are used simultaneously to support full-duplex operation (record and playback). If an 8-bit DMA channel is used, supplied drivers will correctly format the data as either 8-bit or 16-bit. Furthermore, the record and playback rates can be independently programmed.

ISA Host Bus Plug and Play (PnP) Interface

The PnP interface supports six logical devices with programmable I/O base address assignments. The logical devices are typically assigned to WaveArtist command/status registers, Sound Blaster Pro, MPU-401, modem, CD-ROM (RWA011 only), and game port. The address assignment, IRQ, DRQ, and DACK signal routing are established by a software driver writing to configuration registers after successful PnP isolation.

Data is transferred between the RWA010 and the host bus on 16 bidirectional data lines.

Control lines supported are: I/O Read (IOR#), I/O Write (IOW#), Address Enable (AEN), Reset (RESET), and System Bus High (SBHE#) inputs, and I/O 16 (IOCS16#) output.

Interrupt servicing is supported by eight Interrupt Request outputs (IRQ[15, 11, 10, 9, 7, 5, 4, 3]).

Direct memory access (DMA) is supported by four DMA Request outputs (DMA[7, 6, 5, 1]) and four DMA Acknowledge inputs (DACK#[7,6,5,1]).

WaveArtist Command/Status Interface

WaveArtist Command/Status registers are supported. These registers are used to control wavetable data I/O, mixer functions, and WaveArtist extended functions such as downloading sound sets or wave files for DirectSound support.

Sound Blaster Pro Compatible Interface

A Sound Blaster Pro compatible ISA host bus interface is provided. DOS games that are Sound Blaster Pro interface compatible can function without modification. For game playback compatibility, Sound Blaster ADPCM (2, 3, and 4 bit) modes are supported.

PnP Serial EEPROM Interface

A 3-line serial interface to a XICOR X24C02 or compatible serial EEPROM is supported. The interface signals are the Data Clock (SCK) and Write Control (WC#) outputs and a bidirectional Serial Data (SDA) line. A DOS utility is available for programming the EEPROM from the host bus.

Audio Interface

Stereophonic signals supported are: Microphone (RMIC, LMIC), Line In (RLINE, LLINE), CD Audio In (RAUX1,

LAUX1), and Auxiliary 2 In (RAUX2, LAUX2) inputs and Audio Out (ROUT, LOUT) outputs. Monophonic signals supported are: Mono In (MONOIN) input and Mono Out (MONOOUT) output.

Enhanced IDE CD-ROM Interface (RWA011 Only)

The supported signals are CD-ROM Select output (CDSEL#), two programmable address chip select outputs (CDSEL0# and CDSEL1#), CD-ROM Interrupt Request output (CDIRQ), CD-ROM DMA Request output (CDDRQ), and CD-ROM DMA Request Acknowledge input (CDDACK#). The address base and the IRQ and DMA assignments are established via the PnP configuration.

MIDI/Joystick (Game Port) Interface

Eight joystick and two MIDI signals are supported which are typically routed to a 15-pin standard PC game port connector. Only a few external resistors and capacitors are required to complete the game port interface circuit.

The joystick interface has four timer input pins (JAX, JAY, JBX, and JBY) and four button input pins (JA1, JA2, JB1, and JB2). The timer input pins can support two joysticks or four paddles. No external timer device is required.

The MIDI serial interface can receive and transmit serial data at TTL logic levels. External hardware is required to connect the two signals, MIDI Receive (MIDI_RX) input and MIDI Transmit (MIDI_TX) output, to interface with other MIDI compatible components. The serial data character format consists of one start bit (logical 0), eight data bits (LSB shifted first), and one stop bit (logical 1). The data rate complies with the standard MIDI specification.

Modem Interface

Supported modem interface signals are: Modem Reset (RESET#) and Modem Chip Select (MSEL#) outputs and Modem Interrupt Request (MIRQ) input. The RWA010 provides the address decoding from the host bus.

RWA020 Wavetable Synthesizer Interface

The RWA010 connects to an optional RWA020 Wavetable Synthesizer using the Clock (XCLK), Left/Right Clock (LRCLK), and Bit Clock (BCLK) control outputs and the Serial Audio Data Out (SADATAO) input.

RWA030 Music Processor Interface

The RWA010 controls the optional RWA030 Music Processor using the Clock (XCLK), Left/Right Clock (LRCLK), Bit Clock (BCLK), and Reset (WRESET#) outputs. Digital audio data is transferred to and from the RWA030 over the Serial Audio Data Out (SADATAO) and Serial Audio Data In (SADATAI) lines. Additional control/status information is transferred to and from the RWA030 over the High Speed Interface Out (HSIFO) and the High Speed Interface In (HSIFI) serial lines. Digital samples of the analog audio input signals are also sent to the RWA030 using the Sampled Data Output (SDOUT) line.

Host Software

Host software is provided for Windows 95, Windows 3.1x (WSS), and Windows NT.

A DOS utility is available to configure the PnP interface for the MS-DOS environment.

Hardware Interface Signals

The RWA010 pin interface signals are shown in Figure 3.

The RWA010 pin assignments for the 144-pin TQFP are shown in Figure 4.

The RWA010 pin signals are described in Table 2.

Additional Information

Additional RWA010 information is described in the WaveArtist 010 Designer's Guide (Order No. 1101).

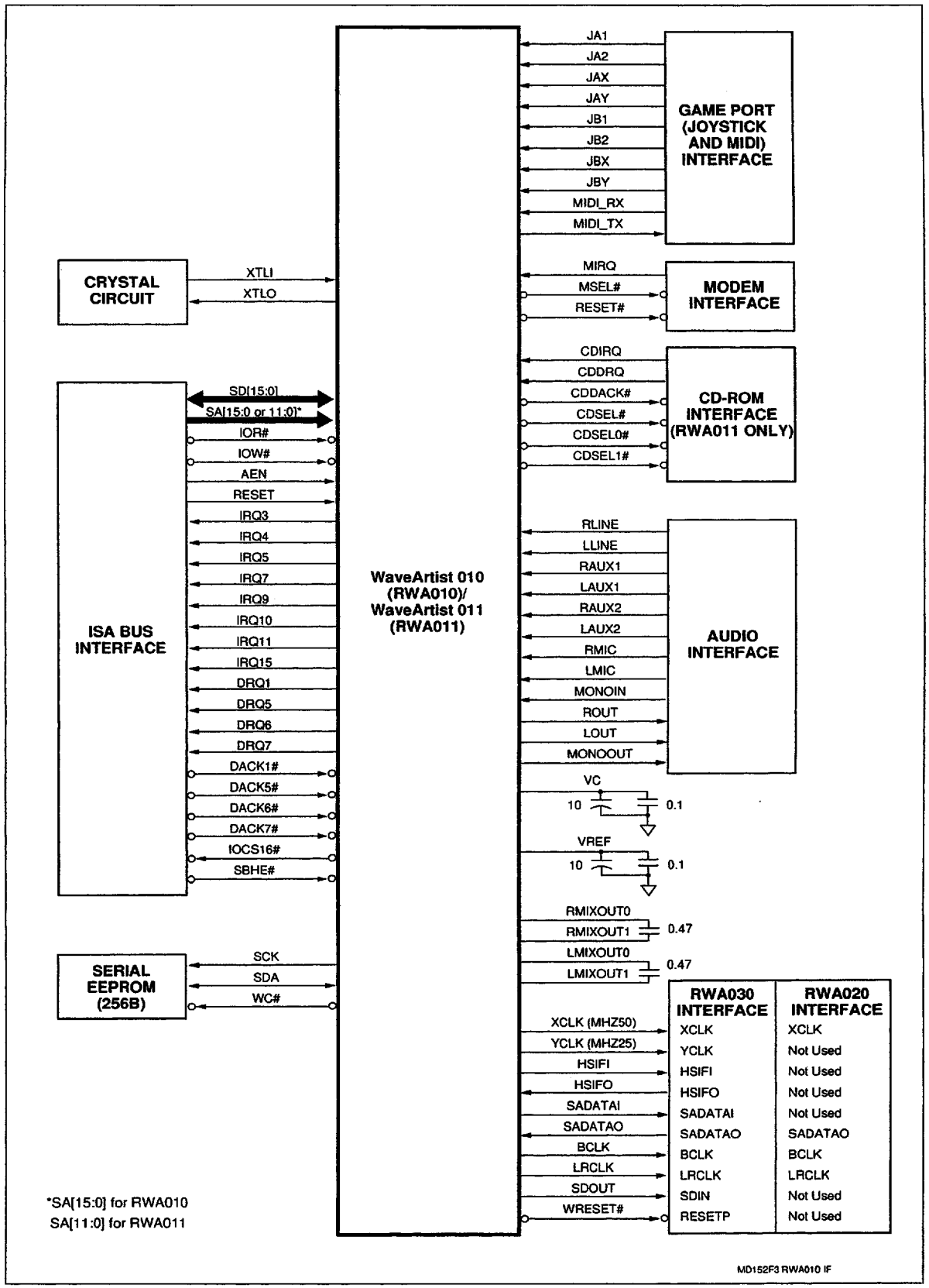

Figure 3. RWA010 Interface Signals

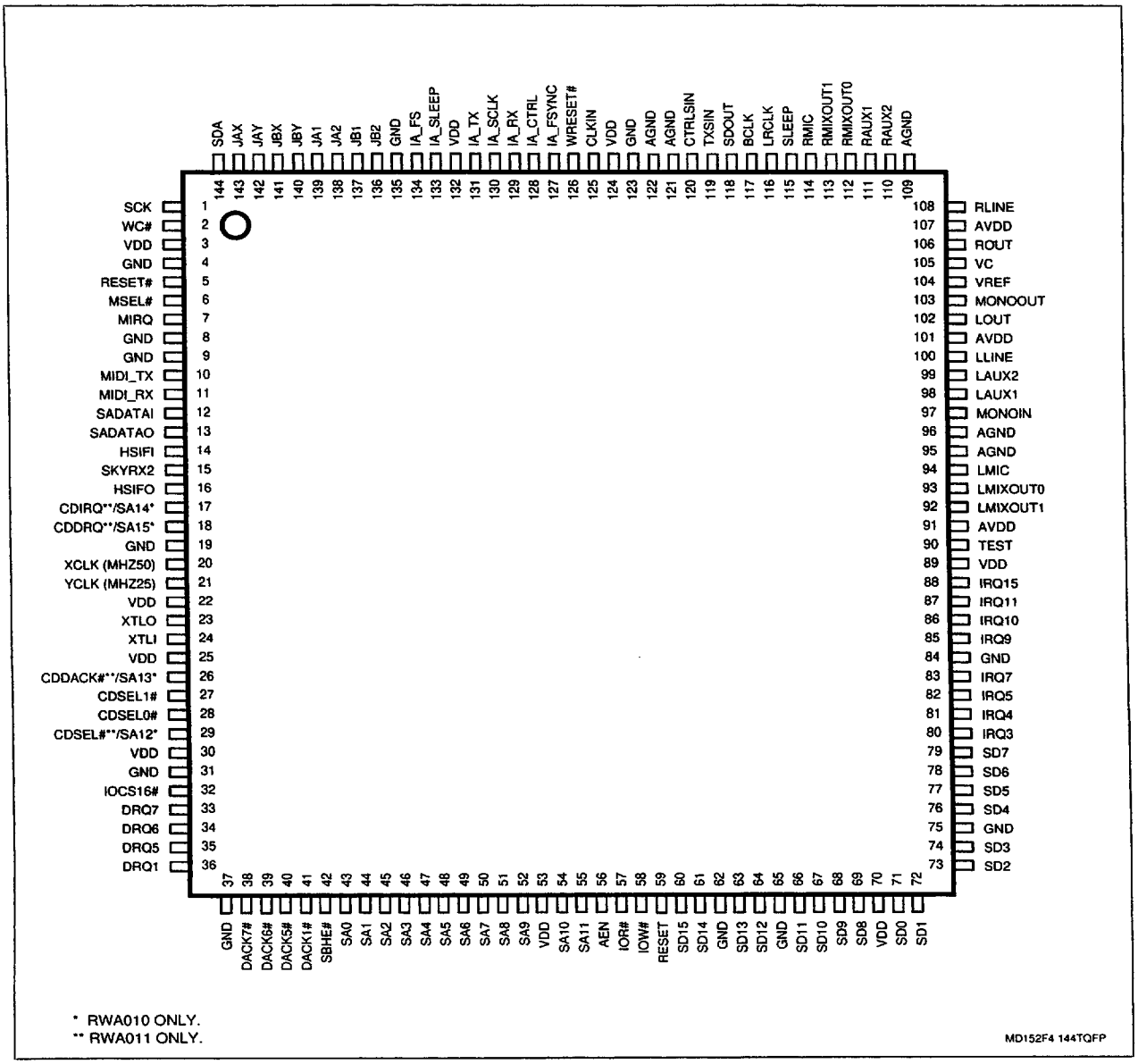

Figure 4. RWA010 Pin Signals - 144-Pin PQFP

Table 2. RWA010 Hardware Interface Signal Definitions

Label	Pin No.	I/O	Signal/Definition
			General
XTLI XTLO	24 23	I, O	**Crystal Input, Crystal Output.** Connect to a 50.8032 MHz crystal circuit.
VDD	3, 22, 25, 30, 53, 70, 89, 124, 132	PWR	**Digital Power.** Connect to +5 VDC.
AVDD	91, 101, 107	PWR	**Analog Power.** Connect to +5 VA.
GND	4, 8-9, 19, 31, 37, 62, 65, 75, 84, 123, 135	GND	**Digital Ground.** Connect to digital ground.
AGND	95-96, 109, 121, 122	GND	**Analog Ground.** Connect to analog ground.
SKYRX2	15		**NC.**
TEST	90		**Test.** NC.
			Host Bus Interface
AEN	56	I	**Host Bus Address Enable.** Active high input asserted during a DMA cycle. The PnP logic responds to the host-address bus and I/O command signal lines (IOR# or IOW#) when AEN is low.
SA[15:12] (RWA010 only), SA[11:0]	18-17, 26, 29, 55-54, 52-43	I	**Host Bus Address Lines.** Host address bus lines used for PnP ADDRESS, WRITE_DATA, READ_DATA ports and I/O Port Base decoding. All I/O and PnP registers are decoded with 16 bits (RWA010) or 10 bits (RWA011).
SD[15:0]	60-61, 63-64, 66-69, 79-76, 74-71	I/O	**Host Bus Data Lines.** Host bus bidirectional data lines used to transfer data between the host and the RWA010.
IOR#	57	I	**Host Bus Read.** Active low input asserted to strobe read data from the RWA010 onto the host data bus (SD[15:0]). This pin has an internal 100k Ω pull-up resistor.
IOW#	58	I	**Host Bus Write.** Active low input asserted to strobe write data from the host data bus (SD[15:0]) into the RWA010. This pin has an internal 100k Ω pull-up resistor.
IRQ[15, 11, 10, 9, 7, 5, 4, 3],	88-85, 83-80	O	**Interrupt Request.** Active high output asserted to indicate an interrupt request by the RWA010.
DRQ1, DRQ5, DRQ6, DRQ7	36-33	O	**DMA Request.** Active high output asserted to request DMA data transfer.
DACK1#, DACK5#, DACK6#, DACK7#	41-38	I	**DMA Request Acknowledge.** Active low input asserted to acknowledge the corresponding DMA request.
RESET	59	I	**Host Reset.** Active high input asserted to reset the RWA010. When asserted, all internal registers are reset to their hardware default states. The pin must be asserted at least 10 ms before being deasserted. While in the reset state, all host bus activity is ignored.
IOCS16#	32	O	**I/O 16.** Active low output asserted during an I/O read or write operation. This pin is an open collector output driver.
SBHE#	42	I	**System Bus High Enable.** Active low input asserted when the high-order byte of the host bus is to be accessed.
			Serial EEPROM Interface
SCK	1	O	**Serial EEPROM Clock.** 400 kHz clock timing output to a 24C02 serial EEPROM.
SDA	144	I/O	**Serial EEPROM Address/Data I/O.** Bidirectional data bit to and from a 24C02 serial EEPROM. Connect this pin to an external pull-up resistor (e.g., 10 kΩ) to VCC.
WC#	2	O	**Serial EEPROM Write Control.** Active low output to allow writing into the EEPROM memory.

Table 2. RWA010 Hardware Interface Signal Definitions (Cont'd)

Label	Pin No.	I/O	Signal/Definition
			Modem Controller Interface
MSEL#	6	O	**Modem Chip Select.** Active low output to the modem controller asserted whenever a valid address is present on host address bus, i.e., an address which falls within the I/O range written by the host bus to the I/O Space Configuration Register.
MIRQ	7	I	**Modem Interrupt Request.** Active high input from the modem's HINT pin.
RESET#	5	O	**Modem Reset.** Active low output; inverse of RESET from the host bus. This signal is used to reset the modem controller and the CD-ROM interface.
			Game Port and MIDI Port Interface
JA1 JA2	139 138	I	**Joystick A Switch Inputs 1 and 2.** Binary inputs used to determine the state of Joystick A switches 1 and 2. These ports each have a built-in 10 kΩ pull-up resistor.
JAX JAY	143 142	I	**Joystick A X-Y Position.** Analog inputs used to determine the position of the Joystick A potentiometer.
JB1 JB2	137 136	I	**Joystick B Switch Inputs 1 and 2.** Binary inputs used to determine the state of Joystick B switches 1 and 2. These ports each have a built-in 10 kΩ pull-up resistor.
JBX JBY	141 140	I	**Joystick B X-Y Position.** Analog inputs used to determine the position of the Joystick B potentiometer.
MIDI_RX	11	I	**MIDI Receive.** MIDI serial input data from the MPU-401 UART compatible interface. This pin has a built-in 100 kΩ pull-up resistor.
MIDI_TX	10	O	**MIDI Transmit.** MIDI serial output data to the MPU-401 UART compatible interface.
			Audio Interface
LAUX1 RAUX1	98 111	I	**Auxiliary Input 1 Left and Right.**
LAUX2 RAUX2	99 110	I	**Auxiliary Input 2 Left and Right.**
LLINE RLINE	100 108	I	**Line-Level Input Left and Right.**
LMIC RMIC	94 114	I	**Microphone Input Left and Right.**
LOUT ROUT	102 106	O	**Line-Level Output Left and Right.**
MONOIN	97	I	**Monaural Input.**
MONOOUT	103	O	**Monaural Output.**
			Audio Interconnect and Reference Voltage
VC	105	REF	**Centerpoint Voltage.** Connect to analog ground through 0.1 µF capacitor and 10 µF capacitor in parallel.
VREF	104	REF	**Reference Voltage.** Connect to analog ground through 0.1 µF and 10 µF in parallel.
LMIXOUT0 LMIXOUT1	93 92	DI	**Mixer Out Coupling Left.** Connect LMIXOUT0 to LMIXOUT1 though an external 0.47 µF capacitor.
RMIXOUT0 RMIXOUT1	112 113	DI	**Mixer Out Coupling Right.** Connect RMIXOUT0 to RMIXOUT1 though an external 0.47 µF capacitor.
			CD-ROM Interface (RWA011 Only)
CDSEL#	29	O	**CD-ROM Chip Select.**
CDSEL0#	28	O	**CD-ROM Chip Select 0.**
CDSEL1#	27	O	**CD-ROM Chip Select 1.**
CDIRQ	17	I	**CD-ROM Interrupt Request.**
CDDRQ	18	I	**CD-ROM DMA Request.**
CDDACK#	26	O	**CD-ROM DMA Request Acknowledge.**

Table 2. RWA010 Hardware Interface Signal Definitions (Cont'd)

Label	Pin No.	I/O	Signal/Definition
RWA010 Interconnect			
SLEEP	115	DI	Connect to IA_SLEEP.
TXSIN	119	DI	Connect to IA_TX.
CLKIN	125	DI	Connect to IA_FS.
CTRLSIN	120	DI	Connect to IA_CTRL.
IA_SLEEP	133	DI	Connect to SLEEP.
IA_TX	131	DI	Connect to TXSIN.
IA_FS	134	DI	Connect to CLKIN.
IA_CTRL	128	DI	Connect to CNTLSIN.
IA_FSYNC	127	DI	Connect to LRCLK.
IA_RX	129	DI	Connect to SDOUT.
IA_SCLK	130	DI	Connect to BCLK.
RWA030 Interface and Associated RWA010 Interconnect			
XCLK (MHZ50)	20	O	**50 MHz Clock.** Connect to RWA030 XCLK.
YCLK (MHZ25)	21	O	**25 MHz Clock.** Connect to RWA030 YCLK.
SADATAI	12	O	**Serial Audio Data In.** Connect to RWA030 SADATAI input.
SADATAO	13	I	**Serial Audio Data Out.** Connect to RWA030 SADATAO output.
LRCLK	116	O	**Left/Right Clock for Serial Audio Data.** Connect to RWA030 LRCLK and to RWA010 IA_FSYNC.
BCLK	117	O	**Bit Clock for Serial Audio Data.** Connect to RWA030 BCLK and to RWA010 IA_SCLK.
HSIFI	14	O	**High Speed Serial Interface Input.** Connect to RWA030 HSIFI.
HSIFO	16	I	**High Speed Serial Interface Output.** Connect to RWA030 HSIFO.
SDOUT	118	O	**Sampled Data Out.** Connect to RWA030 SDIN and to RWA010 IA_RX.
WRESET#	126	O	**Reset.** Active low. Connect to RWA030 RESET.
RWA020 Interface and Associated RWA010 Interconnect			
XCLK (MHZ50)	20	O	**50 MHz Clock.** Connect to RWA020 CLK.
YCLK (MHZ25)	21	O	**25 MHz Clock.** Not used; leave open.
SADATAI	12	O	**Serial Audio Data In.** Not used; leave open.
SADATAO	13	I	**Serial Audio Data Out.** Connect to RWA020 SADATAO output.
LRCLK	116	O	**Left/Right Clock for Serial Audio Data.** Connect to RWA020 LRCLK and to RWA010 IA_FSYNC.
BCLK	117	O	**Bit Clock for Serial Audio Data.** Connect to RWA020 BCLK and to RWA010 IA_SCLK.
HSIFO	14	O	**High Speed Serial Interface Output.** Not used; leave open.
HSIFI	16	I	**High Speed Serial Interface Input.** Not used; leave open.
SDOUT	118	O	**Sampled Data Out.** Not used; leave open.
WRESET#	126	O	**Reset.** Not used; leave open.

Notes:
I/O Type: I = Input, O = Output, DI = Device Interconnect.
No connection (NC) means no external connection allowed (pin may be connected to internal circuitry).

RWA020 Description

General

The host-based RWA020 supports 32-voice polyphony General MIDI wavetable synthesis. The wavetable engine generates digital audio data from a sound sample set stored in an external 1MB (1M x 8) ROM.

The RWA020 receives MIDI commands and transfers digital audio data to the RWA010 over a serial audio data output line without requiring external A/D conversion.

The RWA020 has an integrated ISA host bus PnP interface which utilizes one logical device.

The RWA020 is packaged in an 80-pin PQFP.

Features

- Supports 32 voices at 44.1 KHz
- Internal ISA host bus PnP interface
  - Revision 1.0a compatible
  - 16 bit I/O address decoding
  - Internal PnP Data ROM
- System Controller interface
  - Serial audio output data
- Wavetable ROM interface
  - Interface to 1MB (1M x 8) wavetable ROM
- Integrated MIDI receiver
  - 256-byte FIFO
  - Serial MIDI data mode

External Hardware Interface

ISA Host Bus PnP Interface

The RWA020 can connect directly to the ISA bus without the need for external data bus drivers. All host resources (i.e., I/O registers, IRQ channels, and device activation) are configured via the PnP protocol. Only one logical device is needed.

The interface signals supported are: 16 address inputs (SA[15:0]), 8 bidirectional data lines (SD[7:0]), Address Enable input (AEN), Host Bus Read input (IOR#), Reset input (RESET), Host Bus Write input, (IOW#), six interrupt request outputs (IRQ[12, 11, 10, 9 7, and 5]), and I/O Channel Ready output (IOCHRDY).

The RWA020 interface signals are shown in Figure 5.

RWA010 Mode

The RWA010 Mode is selected when MA0 is low during reset (see Table 3).

Crystal/Clock Interface

The XTLI input pin is to be connected the RWA010 XCLK output. The XTLO pin is to be left open.

RWA010 Interface

Three pins are used to connect to the RWA010: Frame Sync Clock (LRCLK) and Bit Clock (BCLK) inputs, and Serial Audio Data Out (SADATAO) output.

Standalone Mode

The Standalone Mode is selected when MA0 is high during reset (see Table 3).

Crystal/Clock Interface

The XTLI and XTLO pins are to be connected to a 50.8032 MHz crystal circuit.

DAC Interface

Three pins are used to connect to an external DAC: Frame Sync Clock (LRCLK) and Bit Clock (BCLK) outputs, and Serial Audio Data Out (SADATAO) output.

MIDI Interface

The RWA020 supports a 256-byte FIFO for storing and queuing MIDI data. Data is entered into the FIFO via the MIDI Serial Input (MIDI_IN).

Wavetable ROM Interface

The RWA020 external memory bus supports 20 address outputs (MA[20:0]) and eight bidirectional data lines (MD[7:0]) to connect to an external 1MB wavetable ROM. The ROM is organized as 1M x 8 with a maximum access time of 150 ns. The wavetable sound set is available in file form for OEM programming into the ROM. Alternatively, the Rockwell RWA021 (1MB) masked ROM in a 44-pin SOP containing the wavetable sound set is available.

Hardware Interface Signals

The RWA020 interface signals are shown Figure 5.

The RWA020 pin assignments for the 80-pin PQFP are shown in Figure 6.

The RWA020 pin signals are described in Table 3.

Additional Information

Additional information is described in the RWA020 Wavetable Synthesizer Designer's Guide (Order No. 1102.

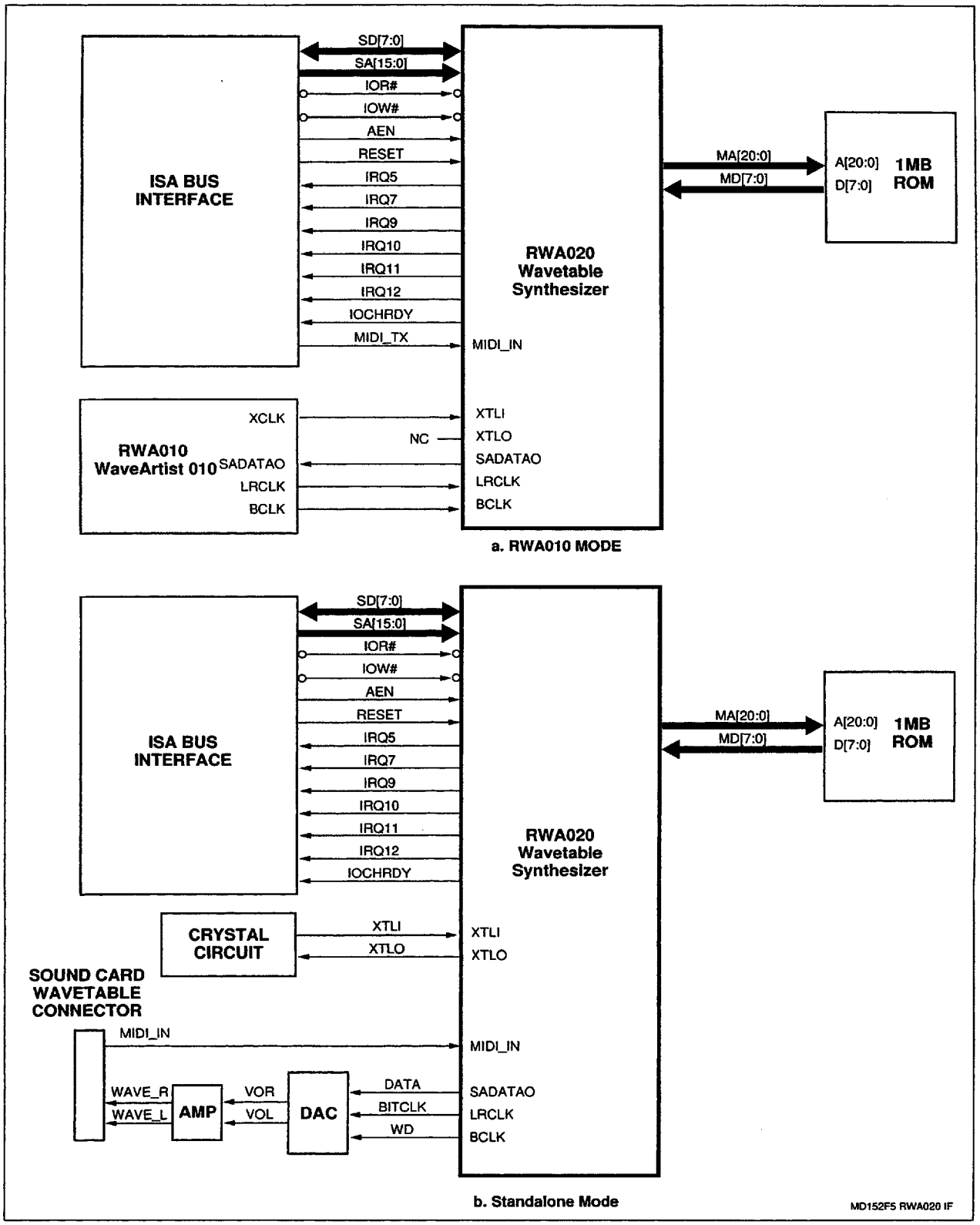

Figure 5. RWA020 Interface Signals

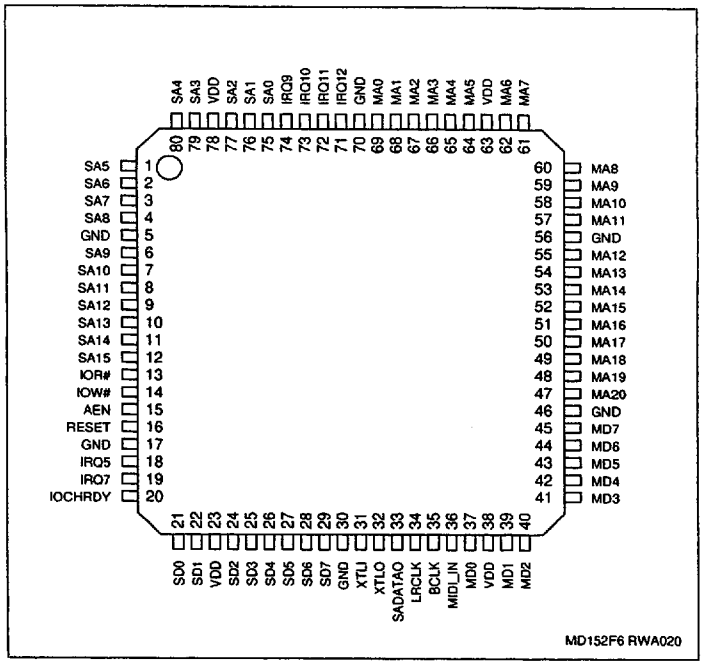

Figure 6. RWA020 Pin Signals - 80-Pin PQFP

Table 3. RWA020 Hardware Interface Signal Definitions

Label	Pin No.	I/O	Signal/Definition
			System
VDD	23, 38, 63, 78	PWR	**Digital Power.** Connect to +5 VDC.
GND	5, 17, 30, 46, 56, 70	GND	**Digital Ground.** Connect to digital ground.
XTLI XTLO	31 32	I O	**Crystal/Clock Input; Clock Output.** For RWA010 Mode operation, connect XTLI to the RWA010 CLK output and leave XTLO open. For Standalone Mode operation, connect XTLI and XTLO to a 50.8032 MHz crystal circuit.
			Host Bus Interface
AEN	15	I	**Host Bus Address Enable.** Active high input asserted during a DMA cycle. The PnP logic responds to the host address bus and I/O command signal lines (IOR# or IOW#) when AEN is low.
SA[15:0]	12-6, 4-1, 80-79, 77-75	I	**Host Bus Address Lines.** Host address bus lines used for PnP ADDRESS, WRITE_DATA, READ_DATA ports and I/O Port Base decoding. All I/O and PnP registers are decoded with 16 bits.
SD[7:0]	29-24, 22-21	I/O	**Host Bus Data Lines.** Host bus bidirectional data lines used to transfer data between the host and the RWA020.
IOR#	13	I	**Host Bus Read.** Active low input asserted to strobe read data from the RWA020 onto the host data bus (SD[7:0]). This pin has an internal 100k Ω pull-up resistor.
IOW#	14	I	**Host Bus Write.** Active low input asserted to strobe write data from the host data bus (SD[7:0]) into the RWA020. This pin has an internal 100k Ω pull-up resistor.
RESET	16	I	**Reset.** Active high input which, when asserted, resets all internal logic and registers to their hardware default states. The pin must be asserted at least 10 ms before being deasserted. While in the reset state, the RWA020 ignores all host bus activity.
IRQ[12-9, 7, 5]	71-74, 19-18	O	**Interrupt Request.** Active high output asserted to indicate an interrupt request by the RWA020. These pins are 16 mA tristate drivers.
IOCHRDY	20	O	**I/O Channel Ready.** Host active low not ready indicator. This pin is an open collector, 16 mA output driver.

Table 3. RWA020 Hardware Interface Signal Definitions (Cont'd)

Label	Pin No.	I/O	Signal/Definition
			Serial Audio Data Interface
LRCLK	34	I/O	**Left/Right Clock for Serial Audio Data.** In RWA010 Mode, LRCLK is an input indicating that data for the right channel (high) or left channel (low) is to be output on the SADATAO pin. Connect LRCLK to RWA010 LRCLK pin. In Standalone Mode, LRCLK is an output indicating that data for the right channel (high) or left channel (low) is being output on the SADATAO pin. Connect LRCLK to the DAC Word Select (WS) input pin.
BCLK	35	I/O	**Bit Clock for Serial Audio Data.** In RWA010 Mode, BCLK is an input clock that shifts the serial audio data out onto the SADATAO pin. Connect BCLK to RWA010 BCLK pin. In Standalone Mode, BCLK is an output clock that shifts the serial audio data out onto the SADATAO pin. Connect BCLK to the DAC Bit Clock (BITCLK) input pin.
SADATAO	33	O	**Serial Audio Data Out.** The serial data is sent most significant bit first, and in two's complement format. Data is shifted out on the rising edge of BCLK. In RWA010 Mode, connect SADATAO to the RWA010 SADATAO input pin. In Standalone Mode, connect SADATAO to the DAC Data (DATA) input pin.
			MIDI Interface
MIDI_IN	36	I	**MIDI Input.** This is the serial MIDI input pin. This pin has an internal 100k Ω pull-up resistor.
			Wavetable ROM Interface
MA[20:0]	47-55, 57-62, 65-69	O	**Memory Bus Address Lines.** MA[20:0] address the 1MB (1M x 8) external wavetable ROM. During reset, the following pins establish the RWA020 wavetable operating mode and must be externally connected either high, e.g., to VCC through a 10 KΩ pullup resistor, or low, e.g., to GND through a 10 KΩ pulldown resistor, as shown: MA0: Connect high to select the RWA010 Mode; Connect low to select the Standalone Mode. MA1: Connect high. MA2: Connect low. MA3: Connect high. MA4: Connect high. MA5: Connect high.
MD[7:0]	45-39, 37	I/O	**Memory Bus Data Lines.** MD[7:0] transfer 8-bit data from the 1MB (1M x 8) external wavetable ROM to the RWA020.

RWA030 Description

General

The RWA030 Music Processor is a high quality wavetable synthesizer which supports 16-channel 32-voice polyphony General MIDI wavetable synthesis. It generates audio data from a sound sample set stored in an external 2MB or 1MB ROM. In addition, the RWA030 supports downloading of sound samples into DRAM (up to 8MB).

The RWA030 also provides basic effects such as reverb, chorus, and 3D spatialization. Treble and bass equalization is supported.

The RWA030 is packaged in an 80-pin PQFP.

Features

- Supports 32 voices at 44.1 KHz
- Audio by Kurzweil
- Built-in basic effects
  - Reverb, chorus, and 3D spatialization
  - Treble and bass equalization
- Host processor interface
  - Serial audio output and input data
  - High speed serial control/status interface
  - Digitally sampled audio data input
- Wavetable ROM and sample DRAM interface
  - Interface to 2MB or 1MB wavetable ROM
  - Interface to sound sample DRAM (up to 8MB)

External Hardware Interface

The RWA030 is optimized for interfacing with the RWA010 host. The RWA030 can also be effectively connected to other hosts through an external DAC to support high quality music and sound effects.

The RWA030 interface signals are shown in Figure 7.

RWA010 Mode

The RWA010 Mode is selected when MODE0 and MODE1 pins are high (see Table 4).

Crystal/Clock Interface

The internal clocking frequency is provided by either an external 50.8032 MHz crystal circuit connected to the Crystal In (XTALI) and Crystal Out (XTALO) pins, or an external clock circuit driving the 50.8032 MHz Clock In (XCLK) and 50.8032/2 MHz Clock In (YCLK) pins, as selected by the Oscillator Enable (OSCEN) input.

RWA010 Interface

Audio data is transferred between the RWA010 and the RWA030 over the Serial Audio Data Out (SADATAO) and Serial Audio Data In (SADATAI) lines without requiring external D/A or A/D conversion. Left/Right Clock (LRCLK) and Bit Clock (BCLK) inputs are used for clocking the data transfer.

A sampled audio data input (SDIN) is also supported to accept digitized raw audio analog samples.

Control, status, and diagnostic data between the RWA030 and the RWA010 is transferred using the High Speed Serial In (HSIFI) and High Speed Serial Out (HSIFO) pins.

Standalone Mode

The Standalone Mode is selected when MODE0 and MODE1 pins are low (see Table 4).

Crystal/Clock Interface

The XTLI and XTLO pins are to be connected to a 50.8032 MHz crystal circuit.

DAC Interface

Three pins are used to connect to an external DAC: Frame Sync Clock (LRCLK) and Bit Clock (BCLK) outputs, and Serial Audio Data Output (SADATAO) output.

MIDI Interface

MIDI data is entered into the RWA010 via the MIDI Serial Input (MIDIIN).

External Memory Bus

The RWA030 external memory bus supports 23 address outputs (MA[22:0]), 16 bidirectional data lines (MD[15:0]), and associated control lines to connect to an external Wavetable ROM and to the optional sound sample DRAM.

ROM Interface

The RWA030 connects to an external 2MB or 1MB wavetable ROM. The ROM is organized as 1M x 16 bits or 512k x 16 bits with a maximum access time of 150 ns. The wavetable sound set is available in file form for OEM programming into the ROM. Alternatively, the Rockwell RWA031 (1MB) or RWA032 (2MB) masked ROM in a 44-pin SOP containing the wavetable sound set is available.

DRAM Interface

The RWA030 optionally connects to DRAM (up to 8MB) to allow sound samples to be downloaded through the RWA030. The DRAM must have a maximum access time of 70 ns.

Hardware Interface Signals

The RWA030 pin interface signals are shown in Figure 7.

The RWA030 pin assignments for the 80-pin PQFP are shown in Figure 8.

The RWA030 pin signals are described in Table 4.

Additional Information

Additional information is described in the RWA030 Music Processor Designer's Guide (Order No. 1103).

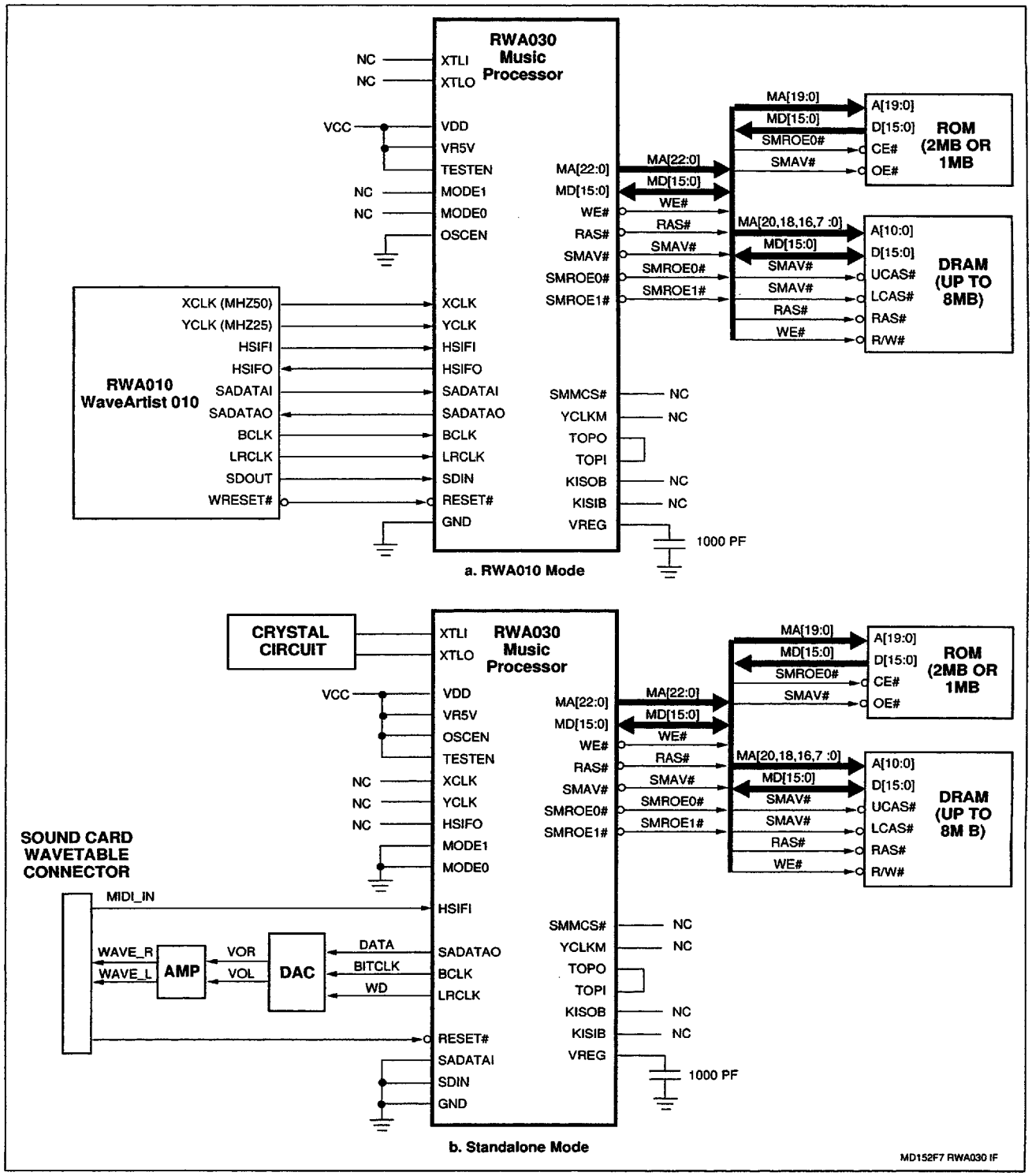

Figure 7. RWA030 Interface Signals

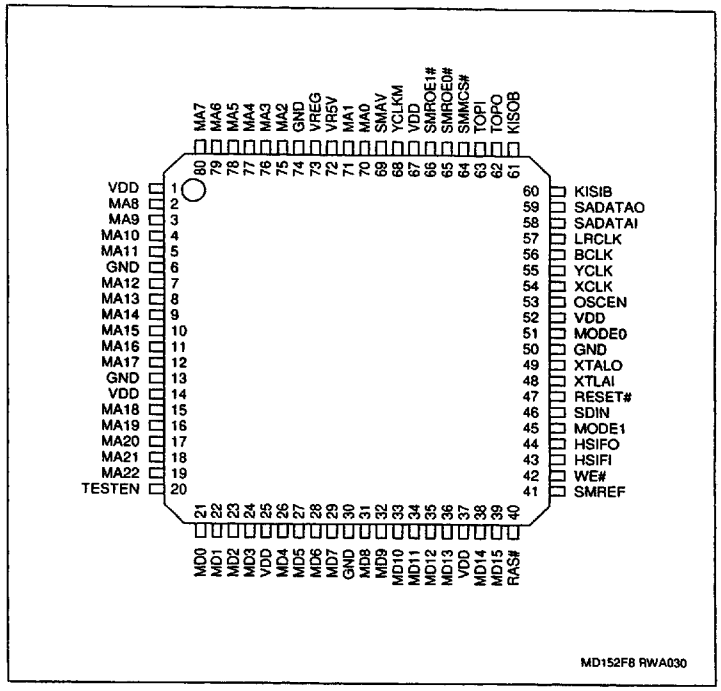

Figure 8. RWA030 Pin Signals - 80-Pin PQFP

Table 4. RWA030 Hardware Interface Signal Definitions

Label	Pin No.	I/O	Signal/Definition
			General
OSCEN	53	I	**Oscillator Enable.** There are two normal modes of clock operation as selected by the OSCEN input. OSCEN high selects the master clock mode in which the internal clock is derived from the crystal circuit using the XTALI and XTALO pins. OSCEN low selects the slave clock mode in which the internal clock is driven from an external clock circuit using the XCLK and YCLK pins.
XCLK, YCLK	54 55	I I	**XCLK (50 MHz), YCLK (25 MHz).** If slave clock mode is selected (OSCEN low), connect XCLK and YCLK to an external clock source. XCLK is 50.8032 MHz and YCLK is 25.4016 MHz. If OSCEN is high, leave these pins open.
XTALI, XTALO	48 49	I, O	**Crystal Input, Crystal Output.** If master clock mode is selected (OSCEN is high), connect XTALI and XTALO to a 50.8032 MHz crystal circuit. If OSCEN is low, leave these pins open.
RESET#	47	I	**Reset.** Active low input which, when asserted, resets all internal logic and registers to their hardware default states. The pin must be asserted at least 10 ms before being deasserted. While in the reset state, the RWA030 ignores all external interface activity.
TESTEN	20	I	**Test.** Connect to VCC.
VR5V	72	PWR	**Digital Power.** Connect to +5 VDC.
VREG	73	PWR	**Regulator Voltage.** Connect to digital ground through 1000 pF capacitor.
VDD	1, 14, 25, 37, 52, 67	PWR	**Digital Power.** Connect to +5 VDC.
GND	6, 13, 30, 50, 74	GND	**Digital Ground.** Connect to digital ground.
MODE0 MODE1	51 45	I	**Mode.** Two encoded input pins select the operating mode. The input selection is: **MODE1** **MODE0** **Operating Mode** Low Low Standalone Mode Low High Reserved High Low Reserved High High RWA010 Mode

Table 4. RWA030 Hardware Interface Signal Definitions (Cont'd)

Label	Pin No.	I/O	Signal/Definition
			Serial Audio Data Interface
LRCLK	57	I/O	**Left/Right Clock for Serial Audio Data.** In RWA010 Mode, LRCLK is an input indicating that data for the right channel (high) or left channel (low) is to be output on the SADATAO pin. Connect LRCLK to the RWA010 LRCLK pin. In Standalone Mode, LRCLK is an output indicating that data for the right channel (high) or left channel (low) is being output on the SADATAO pin. Connect LRCLK to the DAC WS input pin.
BCLK	56	I/O	**Bit Clock for Serial Audio Data.** In RWA010 Mode, BCLK is an input clock that shifts the serial audio data out onto the SADATAO pin. Connect BCLK to RWA010 BCLK pin. In Standalone Mode, BCLK is an output clock that shifts the serial audio data out onto the SADATAO pin. Connect BCLK to DAC Bit Clock (BITCLK) input pin.
SADATAO	59	O	**Serial Audio Data Out.** The serial data is sent most significant bit first, and in two's complement format. Data is shifted out on the rising edge of BCLK. In RWA010 Mode, connect SADATAO to the RWA010 SADATAO input pin. In Standalone Mode, connect SADATAO to the DAC Data (DATA) input pin.
SADATAI	58	I	**Serial Audio Data In.** Serial data is received in two's complement format, most significant bit first. In RWA010 Mode, connect SADATAI to the RWA010 SADATAI output pin. In Standalone Mode, connect SADATAI to ground.
SDIN	46	I	**Sampled Data In.** Digitized analog data sample in the RWA010 analog input. In RWA010 Mode, connect SDIN to the RWA010 SDOUT pin. In Standalone Mode, connect SDIN to ground.
			MIDI Interface
HSIFI	43	I	**MIDI Serial Data/High Speed Serial Interface Input.** In RWA010 Mode, connect HSIFI to the RWA010 HSIFO pin. In Standalone Mode, connect HSIFI to the MIDI input (MIDI_IN).
HSIFO	44	O	**High Speed Serial Interface Output.** High Speed Serial Interface output. In RWA010 Mode, connect HSIFO to the RWA010 HSIFI pin. In Standalone Mode, leave HSIFO open.
			Memory Bus Interface
MA[22:0]	19-15, 12-7, 5-2, 80-75, 71-70	O	**Memory Bus Address Lines.** MA[22:0] address the 2MB or 1MB external wavetable ROM and the optional sound sample DRAM (up to 8MB). The DRAM addressing is: **RWA030 Address Line** / **DRAM Address Line** / **Supported DRAM Size** MA[7:0] / A[7:0] / 64K x 16 (128KB) MA16 / A8 / 256K x 16 (512KB) MA18 / A9 / 1M x 16 (2MB) MA20 / A10 / 4M x 16 (8MB)
MD[15:0]	39-38, 36-31, 29-26, 24-21	I/O	**Memory Bus Data Lines.** MD[15:0] transfer 16-bit data from the external wavetable ROM to the RWA030 and between the RWA030 and the optional sound sample DRAM.
SMROE0#	65	O	**ROM Output Enable 0.** Active low output, asserted to enable the output of the wavetable ROM.
SMROE1#	66	O	**ROM Output Enable 1.** Not used; leave open.
WE#	42	O	**DRAM Write Enable.** Active low, asserted when writing to the optional DRAM.
RAS#	40	O	**DRAM Row Strobe.** Active low output, asserted to strobe the DRAM row address.
SMAV#	69	O	**DRAM Address Lines Valid.** Active low output, asserted to strobe the DRAM column address.
			Reserved
TOPO	62		**Reserved.** Connect TOPO# to the TOPI pin.
TOPI	63		**Reserved.** Connect TOPI to the TOPO# pin.
SMREF	41		**Reserved.** No external connection, leave open (this pin is connected to internal circuitry).
YCLKM	68		**Reserved.** No external connection, leave open (this pin is connected to internal circuitry).
SMMCS#	64		**Reserved.** No external connection, leave open (this pin is connected to internal circuitry).
KISOB	61		**Reserved.** No external connection, leave open (this pin is connected to internal circuitry).
KISIB	60		**Reserved.** No external connection, leave open (this pin is connected to internal circuitry).

Electrical and Environmental Specifications

The current and power requirements are listed in Table 5.

The absolute maximum ratings are listed in Table 6.

Table 5. Current and Power Requirements

Model	Current (ID)		Power (PD)		
	Typical Current (mA)	Maximum Current (mA)	Typical Power (mW)	Maximum Power (mW)	
RWA010					
Normal mode	TBD	TBD	TBD	TBD	
Sleep mode	TBD	TBD	TBD	TBD	
RWA020					
Normal mode	TBD	TBD	TBD	TBD	
Sleep mode	TBD	TBD	TBD	TBD	
RWA030					
Normal mode	TBD	TBD	TBD	TBD	
Sleep mode	TBD	TBD	TBD	TBD	

Notes:
Test conditions: VCC = 5.0 VDC for typical values; VCC = 5.25 VDC for maximum values.

Table 6. Absolute Maximum Ratings

Parameter	Symbol	Limits	Units
Supply Voltage	VDD	-0.5 to +7.0	V
Input Voltage	VIN	-0.5 to (+5VD +0.5)	V
Operating Temperature Range	TA	-0 to +70	°C
Storage Temperature Range	TSTG	-55 to +125	°C
Analog Inputs	VIN	-0.3 to (+5VA + 0.3)	V
Voltage Applied to Outputs in High Impedance (Off) State	VHZ	-0.5 to (+5VD + 0.5)	V
DC Input Clamp Current	IIK	±20	mA
DC Output Clamp Current	IOK	±20	mA
Static Discharge Voltage (25°C)	VESD	±2500	V
Latch-up Current (25°C)	ITRIG	±200	mA