NIPPON PRECISION CIRCUITS INC.

SM9103M

DVDRAM Head Amplifier LSI

OVERVIEW

The SM9103M is a photodiode photoelectric current-to-voltage conversion head amplifier LSI for optical disk pickups in DVDRAM/DVDROM equipment. It sums the photodiode current data signals and then converts the signals to a differential signal for output. The output tracking servo and focusing servo signals are derived from built-in sum and difference circuits, and the gain for these servo signals can be adjusted using serial interface controls. Each of the signals from the photodiodes, used to generate DPD (Differential Phase Detection) tracking servo signal, is current-to-voltage converted and then also output. It operates from a single 5 V supply, and is available in 36-pin plastic SSOP packages.

FEATURES

- RAM/ROM gain switching, low-noise RF signal generator (differential output)
- ROM tracking DPD signal output
- Variable-gain RAM tracking push-pull signal output
- Address signal, high-speed push-pull signal output
- Variable-gain focus error signal output
- Tracking PD sum signal output
- Focus PD sum signal output
- Offset correction timing output (logic)
- Temperature monitor function
- Serial interface to control internal parameter settings
- Sleep-mode function
- Single 5 V supply
- 36-pin plastic SSOP

TYPICAL APPLICATIONS

- Double-speed DVDROM equipment
- Double-speed DVDRAM equipment

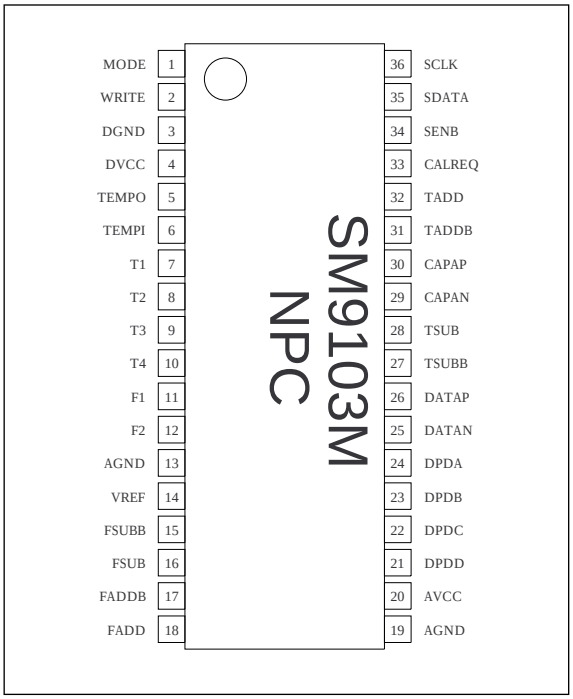
ORDERING INFORMATION

Device	Package
SM9103M	36-pin SSOP

PINOUT

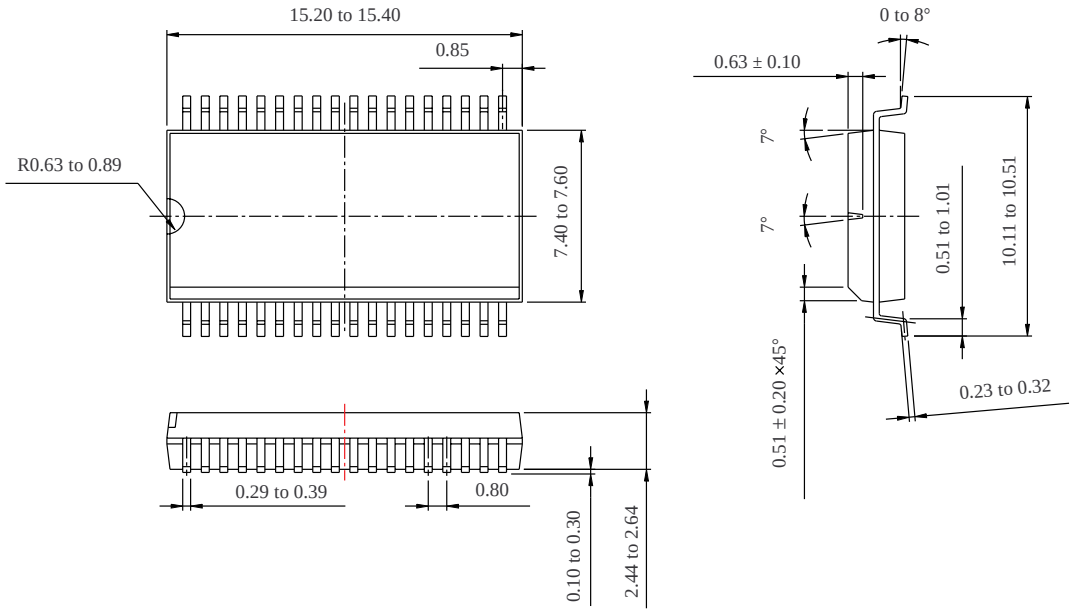
36-pin SSOP

(Top view)

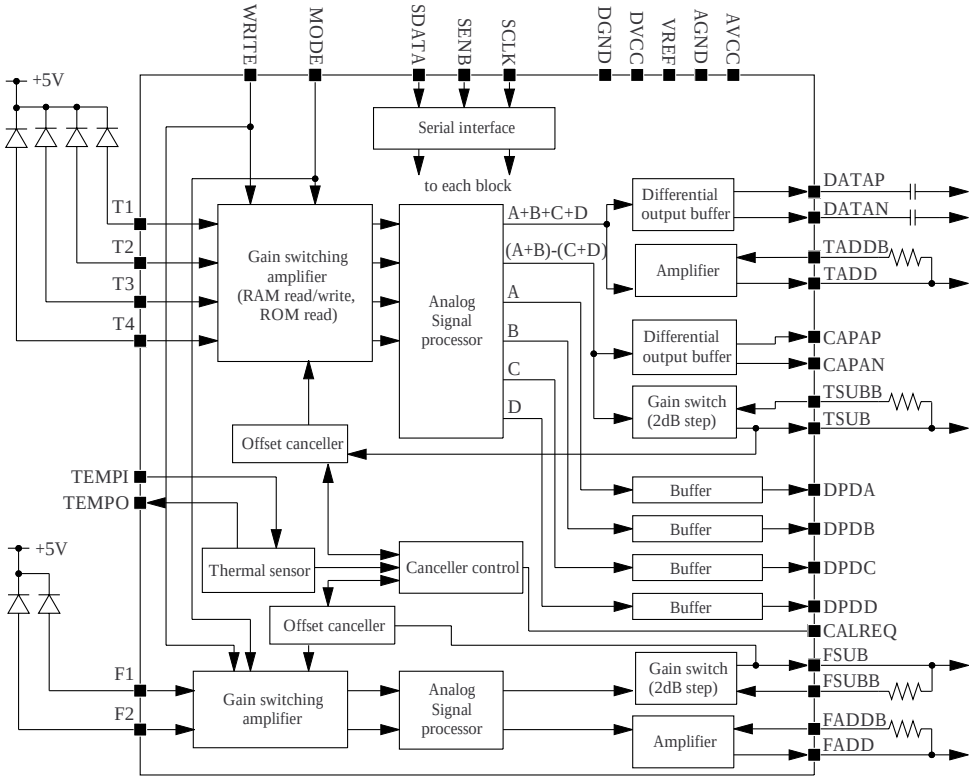


PACKAGE DIMENSIONS

(Unit: mm)



BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	I/O[1]	Function
1	MODE	Ipd	Mode switching/offset correction control input 1
2	WRITE	Ipd	Mode switching/offset correction control input 2
3	DGND	–	Logic circuit ground. Connect to the analog ground if there is no dedicated pickup or logic ground.
4	DVCC	–	Logic circuit supply. Connect to the analog supply if there is no dedicated pickup or logic supply.
5	TEMPO	O	Thermal sensor test output. Leave open for normal operation
6	TEMPI	I	Thermal sensor test input. Leave open for normal operation
7	T1	I	Tracking PD input A
8	T2	I	Tracking PD input B
9	T3	I	Tracking PD input C
10	T4	I	Tracking PD input D
11	F1	I	Focus PD input E
12	F2	I	Focus PD input F
13	AGND	–	Analog circuit ground
14	VREF	I	2.0 V reference voltage input
15	FSUBB	I	Focus error signal feedback input
16	FSUB	O	Focus error signal output
17	FADDB	I	Focus sum signal feedback input
18	FADD	O	Focus sum signal output
19	AGND	–	Analog circuit ground
20	AVCC	–	Analog circuit supply
21	DPDD	O	Buffered tracking signal output D for DPD servo
22	DPDC	O	Buffered tracking signal output C for DPD servo
23	DPDB	O	Buffered tracking signal output B for DPD servo
24	DPDA	O	Buffered tracking signal output A for DPD servo
25	DATAN	O	Phase-modulated data signal differential inverting output
26	DATAP	O	Phase-modulated data signal differential non-inverting output
27	TSUBB	I	Tracking push-pull signal feedback input
28	TSUB	O	Tracking push-pull signal output
29	CAPAN	O	ID data signal differential inverting output
30	CAPAP	O	ID data signal differential non-inverting output
31	TADDB	I	Tracking PD sum signal feedback input
32	TADD	O	Tracking PD sum signal output
33	CALREQ	O	Offset correction status/request output
34	SENB	I	Serial interface enable input
35	SDATA	I/O	Serial interface data input/acknowledge output
36	SCLK	I	Serial interface clock input

1. I = input, Ipd = Input with built-in pull-down resistor, I/O = input/output, O = output

SPECIFICATIONS

Absolute Maximum Ratings

GND = 0 V

Parameter	Symbol	Condition	Rating	Unit
Supply voltage range	V_{CC}		–0.5 to 7.0	V
Input voltage range	V_{IN}		– 0.5 to V_{CC} + 0.5	V
Input current range	I_{IN}		– 3.0 to +3.0	mA
Operating temperature range	T_{opr}		0 to 70	°C
Storage temperature range	T_{stg}		–40 to 125	°C
Power dissipation	P_D		250	mW
Soldering temperature	T_{sld}		260	°C
Soldering time	t_{sld}		10	s

Recommended Operating Conditions

GND = 0 V

Parameter	Symbol	Condition	Rating	Unit
Specs-guaranteed supply voltage range	V_{CC}		4.75 to 5.25	V
Operating supply voltage range	V_{CC}		4.5 to 5.5	V
Reference voltage input	V_{REF}		1.89 to 2.11	V
Operating temperature range	T_{opr}		0 to 70	°C

DC Electrical Characteristics

V_{CC} = 5 V ± 5%, GND = 0 V, T_a = 0 to 70 °C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Current consumption[1]	I_{CC1}	Operating mode	–	24	30	mA
	I_{CC2}	Sleep mode	–	–	1	
MODE, WRITE, SENB, SDATA, SCLK HIGH-level input voltage	V_{IH}		$0.8V_{CC}$	–	–	V
MODE, WRITE, SENB, SDATA, SCLK LOW-level input voltage	V_{IL}		–	–	$0.2V_{CC}$	V
MODE, WRITE HIGH-level input current	I_{IH1}	$V_{IN} = V_{CC}$	50	100	200	µA
SENB, SDATA, SCLK HIGH-level input current	I_{IH2}	$V_{IN} = V_{CC}$	–	–	3	µA
MODE, WRITE, SENB, SDATA, SCLK LOW-level input current	I_{IL}	V_{IN} = 0 V	–3	–	–	µA
CALREQ HIGH-level output voltage	V_{OH}	I_{OH} = –0.2 mA	V_{CC} – 0.2	–	–	V
CALREQ LOW-level output voltage	V_{OL1}	I_{OL} = 0.8 mA	–	–	0.4	V
SDATA LOW-level output voltage	V_{OL2}	I_{OL} = 7 mA	–	–	1.0	V
VREF input current	I_{REF}	V_{REF} = 2.0 V	–	–	250	µA

1. 18 kΩ resistor connected between TSUB and TSUBB
   47 kΩ resistor connected between TADD and TADDB
   22 kΩ resistor connected between FSUB and FSUBB
   27 kΩ resistor connected between FADD and FADDB
   SENB, SDATA, SCLK connected to GND; All other pins (excluding supply and ground pins) open circuit.

Tracking PD Input Characteristics (T1, T2, T3, T4)

V_{CC} = 5 V ± 5%, GND = 0 V, T_a = 0 to 70 °C

Parameter	Condition		Rating			Unit
			min	typ	max	
Input impedance	No signal		–	–	250	Ω
Input conversion noise current	100 kHz to 10 MHz	RAM read[1]	–	0.035	–	$µA_{rms}$
		ROM read[1]	–	0.27	–	
Pin voltage	No signal		–	–	1.5	V

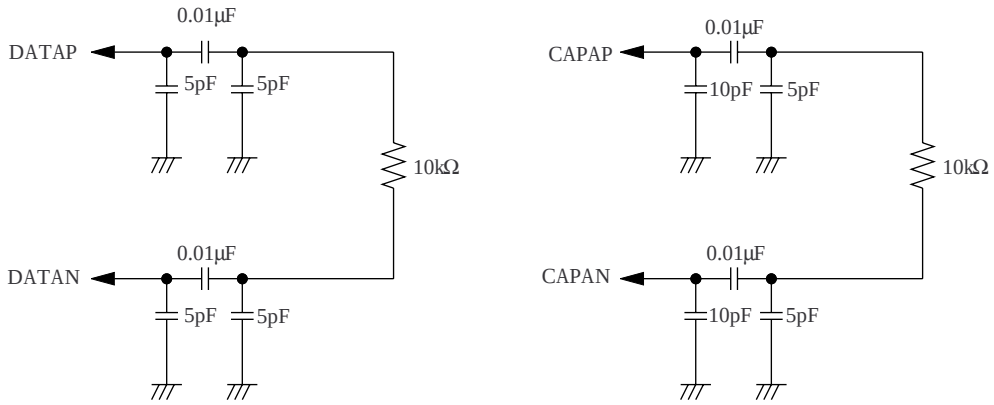
1. DATAP – DATAN output difference operation when 10 pF capacitors are connected to T1, T2, T3, T4

Data Signal Processor Characteristics

V_{CC} = 5 V ± 5%, GND = 0 V, T_a = 0 to 70 °C

Parameter	Condition	Rating			Unit
		min	typ	max	
DATAP–DATAN current-to-voltage converter coefficient[1]	RAM read	10.0	12.5	15.0	kΩ
	ROM read	2.50	3.12	3.74	
CAPAP–CAPAN current-to-voltage converter coefficient[2]	RAM read	11.3	14.1	16.9	kΩ
DATAP, DATAN, CAPAP, CAPAN output impedance		–	–	100	Ω
DATAP, DATAN, CAPAP, CAPAN output center voltage[3]	No signal	$0.9V_{REF}$	–	$1.1V_{REF}$	V
CAPAP, CAPAN output center voltage difference[3]	No signal	–	–	±50	mV
DATAP, DATAN, CAPAP, CAPAN output operating output voltage	10 kΩ load, output center voltage reference	–0.7	–	+0.7	V
Variable coefficient switching time	RAM ↔ ROM read	–	–	10	ms
Saturation output reset time[4]	RAM write → RAM read	–	–	500	ns
DATAP, DATAN signal bandwidth[5]	f = 100 kHz –3 dB frequency	19	–	–	MHz
CAPAP, CAPAN signal bandwidth[5]	f = 100 kHz –3 dB frequency	20	–	–	MHz
DATAP–DATAN, CAPAP–CAPAN gain peaking[5]	f = 100 kHz –3 dB frequency	–3	–	+0.5	dB
DATAP–DATAN, CAPAP–CAPAN group delay time[5]	f = 1 to 10 MHz	–	–	±1.0	ns

1. [DATAP – DATAN] = K × [I_{T1} + I_{T2} + I_{T3} + I_{T4}]
2. [CAPAP – CAPAN] = K × {[I_{T1} + I_{T2}] – [I_{T3} + I_{T4}]}
3. 5 kΩ load connected to ground to prevent abnormal operation
4. Converging to within final value ± 10%
5. 10 pF input load capacitors connected to T1, T2, T3, T4. DATAP, DATAN, CAPAP, CAPAN output load conditions shown below.



Tracking Signal Processor Characteristics

V_{CC} = 5 V ± 5%, GND = 0 V, T_a = 0 to 70 °C

Parameter	Condition		Rating			Unit
			min	typ	max	
TSUB current-to-voltage converter coefficient[1]	RAM read	R_f = 18 kΩ, $V_{OUT} = V_{REF} \pm 0.8$ V	10.64	11.95	13.26	kΩ
	ROM read		2.67	2.99	9.92	
	RAM write		1.78	1.99	2.20	
TADD current-to-voltage converter coefficient[2]	RAM read	R_f = 47 kΩ	27.82	31.25	34.68	kΩ
	ROM read		6.95	7.80	8.65	
	RAM write		4.63	5.20	5.77	
DPDA, DPDB, DPDC, DPDD current-to-voltage converter coefficient[3]	RAM read		40.0	50.0	60.0	kΩ
	ROM read		10.0	12.5	15.0	
T1, T2, T3, T4 converter coefficient relative error	TSUB output, RAM/ROM read		–	–	±2	%
TSUB, TADD, DPDA, DPDB, DPDC, DPDD output impedance			–	–	100	Ω
TSUB operating output voltage	10 kΩ load connected to VREF		1	–	3	V
TADD, DPDA, DPDB, DPDC, DPDD operating output voltage	10 kΩ load connected to VREF		V_{REF}	–	3	V
Converter coefficient switching time	RAM read ↔ ROM read		–	–	10	ms
	RAM write ↔ RAM read		–	–	3	µs
TSUB, TADD signal bandwidth[4]	DC to –3 dB frequency		1	–	–	MHz
DPDA, DPDB, DPDC, DPDD signal bandwidth[4]	f = 100 kHz to –3 dB frequency		5	–	–	MHz
TSUB, TADD gain peaking[4]	f = 10 kHz to –3 dB frequency		–3	–	+0.5	dB
DPDA, DPDB, DPDC, DPDD gain peaking[4]	f = 100 kHz to –3 dB frequency		–3	–	+4.0	dB
TSUB phase response[4]	@ f = 100 kHz		–	–	10	°
DPDA, DPDB, DPDC, DPDD group delay[4]	f = 1 to 5 MHz group delay differential absolute value		–	–	5	ns
	Relative error between 4 pins		–	–	1.0	
TSUB offset voltage	No input signal, V_{REF} reference, post-correction, T_a = 25°C, R_f = 18 kΩ	RAM read/write max gain	–	–	±10.0	mV
		RAM read, min to max gain	–	–	±26	
		RAM read/write differential gain max.	–	–	±4	
		ROM read, gain min/max	–	–	±100	
TADD offset voltage	No input signal, V_{REF} reference	RAM read	–	–	±30	mV
		ROM read	–	–	±300	
DPDA, DPDB, DPDC, DPDD offset voltage	No input signal, V_{REF} reference	RAM/ROM read	–550	–	+50	mV
TSUB offset voltage temperature coefficient	R_f = 18 kΩ		–	–	±0.4	mV/°C
TSUB variable gain range			–16	–	+14	dB
TSUB variable gain step width			–	2	–	dB

Parameter	Condition		Rating			Unit
			min	typ	max	
TSUB gain switching absolute accuracy	$V_{OUT} = V_{REF} \pm 0.8$ V	–16 to +8 dB	–	–	±0.5	dB
		+10 to +14 dB	–	–	±1.0	

1. TSUB = $K \times \{[I_{T1} + I_{T2}] - [I_{T3} + I_{T4}]\}$, gain = 0 dB
2. TADD = $K \times [I_{T1} + I_{T2} + I_{T3} + I_{T4}]$
3. DPDA = $K \times I_{T1}$, DPDB = $K \times I_{T2}$, DPDC = $K \times I_{T3}$, DPDD = $K \times I_{T4}$
4. T1, T2, T3, T4: 10 pF input load capacitance
   TSUB, TADD, DPDA, DPDB, DPDC, DPDD: 10 pF output load capacitance
   TSUB, TADD: 10 kΩ load resistance
   DPDA, DPDB, DPDC, DPDD: 100 kΩ load resistance

Focus PD Input Characteristics (F1, F2)

V_{CC} = 5 V ± 5%, GND = 0 V, T_a = 0 to 70 °C

Parameter	Condition		Rating			Unit
			min	typ	max	
Input impedance	No signal		–	–	250	Ω
Input conversion noise current	DC to 10 kHz	RAM read[1]	–	–	24	nA_{rms}
		ROM read[1]	–	–	96	
		RAM write[1]	–	–	150	
Pin voltage	No signal, V_{REF} reference		–	–	±50	mV

1. Conversion from FSUB output noise value when 14 pF capacitors connected to F1 and F2

Focus Signal Processor Characteristics

V_{CC} = 5 V ± 5%, GND = 0 V, T_a = 0 to 70 °C

Parameter	Condition		Rating			Unit
			min	typ	max	
FSUB current-to-voltage converter coefficient[1]	RAM read	R_f = 22 kΩ, $V_{OUT} = V_{REF} \pm 0.35$ V	370	415	460	kΩ
	ROM read		94	105	116	
	RAM write		58	65	72	
FADD current-to-voltage converter coefficient[2]	RAM read	R_f = 27 kΩ	223	250	277	kΩ
	ROM read		56.1	63	69.9	
	RAM write		35.6	40	44.1	
F1, F2 converter coefficient relative error	FSUB output, RAM/ROM read		–	–	±2	%
FSUB, FADD output impedance			–	–	100	Ω
FSUB operating output voltage	10 kΩ load connected to VREF		1	–	3	V
FADD operating output voltage	10 kΩ load connected to VREF		V_{REF}	–	3	V
Converter coefficient switching time	RAM read ↔ ROM read		–	–	10	ms
	RAM write ↔ RAM read		–	–	3	µs
FSUB, FADD signal bandwidth[3]	DC to –3 dB frequency		200	–	–	kHz
FSUB, FADD gain peaking[3]	f = 10 kHz to –3 dB frequency		–3	–	+0.5	dB
FSUB, FADD phase response[3]	@ f = 10 kHz		–	–	5	°

Parameter	Condition		Rating			Unit
			min	typ	max	
FSUB offset voltage	No input signal, V_{REF} reference, post-correction, T_a = 25°C	RAM read/write, ROM read max gain	–	–	±7.0	mV
		RAM read, min to max gain	–	–	±21	
		RAM read/write differential gain max.	–	–	±4	
FADD offset voltage	No input signal, V_{REF} reference		–	–	±50	mV
FSUB offset voltage temperature coefficient			–	–	±0.22	mV/°C
FSUB variable gain range			–16	–	+14	dB
FSUB variable gain step width			–	2	–	dB
FSUB gain switching absolute accuracy	$V_{OUT} = V_{REF} \pm 0.35$ V	–16 to +8 dB	–	–	±0.5	dB
		+10 to +14 dB	–	–	±1.0	

1. FSUB = $K \times [I_{F1} - I_{F2}]$, gain = 0 dB
2. FADD = $K \times [I_{F1} + I_{F2}]$
3. F1, F2: 14 pF input load capacitance
   FSUB, FADD: 10 pF output load capacitance, 10 kΩ load resistance

Mode Control Logic

Control input		Operating mode	Offset correction
WRITE	MODE		
LOW or open	LOW or open	RAM read	Active
LOW or open	HIGH	ROM read	
HIGH	LOW or open	RAM write	
HIGH	HIGH		Inactive

Offset Correction Characteristics

V_{CC} = 5 V ± 5%, GND = 0 V, T_a = 0 to 70 °C

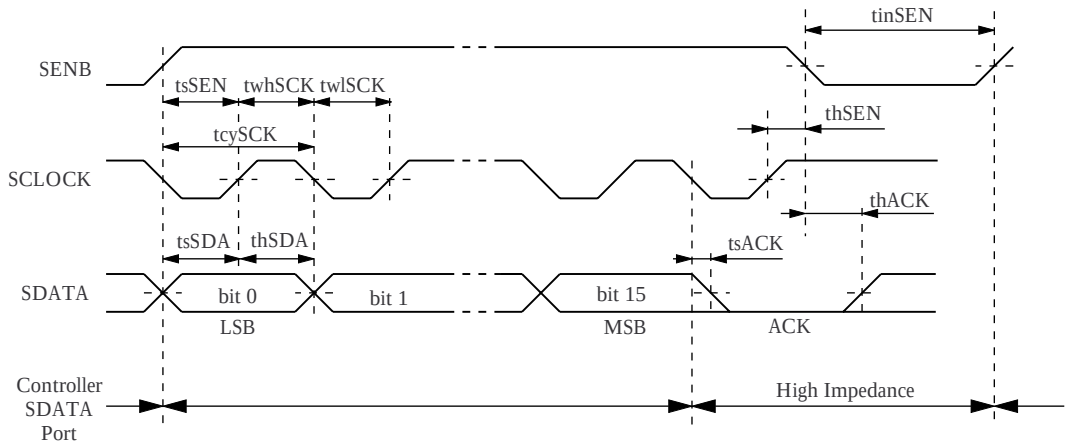
Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
TSUB offset residual		V_{REF} reference, T_a = 25 °C	–	–	±8.5	mV
FSUB offset residual		V_{REF} reference, T_a = 25 °C	–	–	±5.5	mV
Supply voltage droop detect level	V_1		1.9	2.8	3.7	V
Correction circuit startup supply voltage	V_2		3.2	3.8	4.4	V
V_1 and V_2 difference	$V_2 - V_1$		0.7	1.0	1.3	V
Correction thermal sensor detect temperature			15	20	25	°C
Offset correction time			–	–	150	ms

Serial Interface Characteristics

V_{CC} = 5 V ± 5%, GND = 0 V, T_a = 0 to 70 °C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
SCLK pulse cycle	t_{cySCK}		100	–	–	ns
SCLK HIGH-level pulsewidth	t_{whSCK}		40	–	–	ns
SCLK LOW-level pulsewidth	t_{wlSCK}		40	–	–	ns
SENB setup time	t_{sSEN}		20	–	–	ns
SENB hold time	t_{hSEN}		40	–	–	ns
SDATA setup time	t_{sSDA}		15	–	–	ns
SDATA hold time	t_{hSDA}		15	–	–	ns
ACK setup time[1]	t_{sACK}		0	–	20	ns
ACK hold time[1]	t_{hACK}		–	–	50	ns
SENB interval	t_{inSEN}		100	–	–	ns

1. ACK is the acknowledge output (n-channel open-drain). LOW-level output when the data received is valid.
SDATA load capacitance is 15 pF.



FUNCTIONAL DESCRIPTION

Serial Interface

The SM9103M uses a serial interface comprising 2 ports to control and set TSUB/FSUB output gain switching, sleep mode to reduce current consumption, and TSUB/FSUB offset correction. The address and bit configuration of each port is shown in table 1.

Table 1. Port address and bit configuration[1]

Bit number															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Data								**Address**							
MSB															**LSB**
TG3	TG2	TG1	TG0	FG3	FG2	FG1	FG0	×	LOW	LOW	LOW	LOW	LOW	×	×
SL1	CS1	–	–	–	–	–	–	×	LOW	LOW	LOW	LOW	HIGH	×	×

1. × = don't care, – = unassigned
   TG3 to TG0: TSUB gain set bits. Default = 0111 (0 dB)
   FG3 to FG0: FSUB gain set bits. Default = 0111 (0 dB)
   SL1: sleep mode set bit. Sleep mode when 1, normal operation when 0. Default = 0.
   CS1: offset correction control. Offset correction when 1, normal operation when 0. Default = 0.

Serial data is input on SDATA with the LSB first in sync with the falling edge of the SCLK clock. After the 16th SCLK falling edge and 16 bits of valid data has been input, the SDATA n-channel open-drain output goes LOW to perform the function of an acknowledge signal.

If the number of SCLK cycles which occur when SENB (serial interface enable) is HIGH is less than 16, the received data is ignored and the internal port is not updated. If the number of SCLK cycles is greater than 16, the data is still considered value up to the 16th SCLK falling edge, the data is latched into the internal port, and the acknowledge signal is output. The acknowledge signal is held until SENB goes LOW again.

Data Signal Processor

This stage creates the data signal and ID signal for output. The weak current from the tracking PD cells (T1, T2, T3, T4) are input to the front-end amplifier where the signals are current-to-voltage converted at fixed gain.

The gain setting is controlled by pins WRITE and MODE. WRITE switches between read/write, and MODE switches the gain between values corresponding to high-reflectivity and low-reflectivity discs. These signals control the settings for RAM (low-reflectivity disc) read/write and ROM (high-reflectivity disc) read.

The front-end amplifier outputs are processed by the signal processor block to generate intermediate signals. The data signal, (A + B + C + D), is converted to a difference signal by a differential output buffer and output on DATAP and DATAN. The ID signal, generated from the difference between 2 signals, (A + B) and (C + D), is converted to a difference signal by a differential output buffer and output on CAPAP and CAPAN. The data signal (DATAP, DATAN) and ID signal (CAPAP, CAPAN) DC components are removed using output stage capacitive networks.

T1, T2, T3 and T4 have a hold function to provide the appropriate reverse bias required by the tracking PD to ensure the data read bandwidth.

Tracking Signal Processor

The tracking stage generates the push-pull tracking error signal and output signal for DPD servo, as well as a push-pull sum signal used as an auxiliary signal.

The [(A + B) – (C + D)] signal from the common-data front-end amplifier and signal processor block is sent to the gain switching block. The gain switching block amplifies the difference signal using one of 16 preset gain settings in 2 dB steps to form a push-pull signal output on TSUB. A feedback resistor connected to TSUBB is used to ensure gain setting stability. The gain of the gain switching block is controlled by serial interface control bits as shown in table 2.

Each signal from T1, T2, T3, T4 is buffered and then output on DPDA, DPDB, DPDC, DPDD, respectively, for DPD servos.

The auxiliary signal is generated from the push-pull sum signal (A + B + C + D). This signal is buffered (TAB) and output on TADD. A feedback resistor connected to TADDB is used to ensure gain setting stability.

Table 2. TSUB gain setting

TG3	TG2	TG1	TG0	Gain (dB)[1]
0	0	0	0	+14
0	0	0	1	+12
0	0	1	0	+10
0	0	1	1	+8
0	1	0	0	+6
0	1	0	1	+4
0	1	1	0	+2
0	1	1	1	0
1	0	0	0	–2
1	0	0	1	–4
1	0	1	0	–6
1	0	1	1	–8
1	1	0	0	–10
1	1	0	1	–12
1	1	1	0	–14
1	1	1	1	–16

1. Default is 0 dB

Focus Signal Processor

The focus stage generates the focus error signal from the focus PD, and a sum signal. The weak focus PD current signals (F1, F2) are input to the front-end amplifier and then current-to-voltage converted at fixed gain.

The front-end amplifier output is sent to the signal processor block where the focus error signal (F1 – F2) and the sum signal (F1 + F2) are generated.

The focus error signal is sent to the gain switching block. The gain switching block amplifies the difference signal using one of 16 preset gain settings in 2 dB steps with output on FSUB. A feedback resistor connected to FSUBB is used to ensure gain setting stability. The gain of the gain switching block is controlled by serial interface control bits as shown in table 3.

The sum is buffered and output on FADD. A feedback resistor connected to FADDB is used to ensure gain setting stability.

Table 3. FSUB gain setting

FG3	FG2	FG1	FG0	Gain (dB)[1]
0	0	0	0	+14
0	0	0	1	+12
0	0	1	0	+10
0	0	1	1	+8
0	1	0	0	+6
0	1	0	1	+4
0	1	1	0	+2
0	1	1	1	0
1	0	0	0	–2
1	0	0	1	–4
1	0	1	0	–6
1	0	1	1	–8
1	1	0	0	–10
1	1	0	1	–12
1	1	1	0	–14
1	1	1	1	–16

1. Default is 0 dB

Offset Correction

The SM9103M has built-in offset correction circuits for tracking and focus. During offset correction, the internal the device operates in RAM read mode, and FSUB and TSUB operate at maximum gain (+14 dB). The outputs on FSUB, FADD and TSUB are indeterminate. Also, inputs T1, T2, T3, T4 and F1, F2 may be ignored. After correction is complete, the FSUB and TSUB gain settings return to their default values (0 dB).

Offset correction is performed under the following conditions:

- When power is applied.
- When the supply drops below 2.8 ± 0.9 V and then rises to above 3.8 ± 0.6 V.
- When sleep mode operation is cancelled.
- When the serial interface bit CS1 is 1. Note that if SL1 is also 1, then SL1 has priority.

Table 4. Offset correction setting

CS1	Offset correction[1]
0	No correction
1	Correction

1. Default is No correction

If the voltage falls below 2.8 ± 0.9 V during offset correction, then correction stops and does not restart until the supply recovers to above 3.8 ± 0.6 V.

During offset correction, the CALREQ output is held HIGH. CALREQ goes LOW after correction stops.

The SM9103M also incorporates a temperature detect function which detects temperature changes of 20 ± 5 °C from the time the initial correction is performed. If a temperature change is detected, CALREQ goes HIGH and the device waits for an offset correction instruction.

Note that when both WRITE and MODE are HIGH, offset correction is inactive and the output appears uncorrected. However, if a correction start condition occurs when correction is inactive, such as the correction flag CS1 set to 1, then correction operation is initiated internally but does not appear at the output unless correction is activated prior to correction operation finishing.

Once correction has been made inactive, the output remains uncorrected even if correction is subsequently reactivated. In this case, the output remains uncorrected until a valid correction start condition is detected.

Sleep Mode

The SM9103M features a sleep mode which can be used when the device is not operating to significantly reduce current consumption. The sleep mode is controlled by serial interface bit SL1.

Table 5. Sleep mode settings

SL1	Sleep mode[1]	Mode description
LOW	OFF	Normal operation
HIGH	ON	Sleep condition

1. Default is OFF

Preset Function

When power is applied or after offset correction, all serial interface flags are reset to their default values. Flags TG3 to TG0 and FG3 to FG0 are also set to their default values in sleep mode.

NPC
NIPPON PRECISION CIRCUITS INC.

NIPPON PRECISION CIRCUITS INC.

4-3, Fukuzumi 2-chome
Koto-ku, Tokyo 135-8430, Japan
Telephone: 03-3642-6661
Facsimile: 03-3642-6698

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