74LVC1G175

Single D-type flip-flop with reset; positive-edge trigger

Rev. 01 — 18 October 2004 **Product data sheet**

1. General description

The 74LVC1G175 is a high-performance, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The input can be driven from either 3.3 V or 5 V devices. This feature allows the use of this device in a mixed 3.3 V and 5 V environment.

This device is fully specified for partial power-down applications using I_{off}. The I_{off} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

The 74LVC1G175 is a single positive edge triggered D-type flip-flop with individual data (D) input, clock (CP) input, master reset ($\overline{MR}$) input, and Q output.

The master reset ($\overline{MR}$) is an asynchronous active LOW input and operate independently of the clock input. Information on the data input is transferred to the Q output on the LOW-to-HIGH transition of the clock pulse. The D input must be stable one set-up time prior to the LOW-to-HIGH clock transition, for predictable operation.

Schmitt-trigger action at all inputs makes the circuit highly tolerant to slower input rise and fall times.

2. Features

- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant inputs for interfacing with 5 V logic
- High noise immunity
- Complies with JEDEC standard:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8B/JESD36 (2.7 V to 3.6 V).
- ±24 mA output drive (V_{CC} = 3.0 V)
- ESD protection:
  - HBM EIA/JESD22-A114-B exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V.
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- Multiple package options
- Specified from –40 °C to +85 °C and –40 °C to +125 °C.

PHILIPS

3. Quick reference data

Table 1: Quick reference data

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PHL}, t_{PLH}	propagation delay CP to Q	C_L = 50 pF; V_{CC} = 3.3 V	1.0	3.1	5.7	ns
	propagation delay $\overline{MR}$ to Q	C_L = 50 pF; V_{CC} = 3.3 V	1.0	2.5	5.8	ns
f_{max}	maximum clock frequency	C_L = 50 pF; V_{CC} = 3.3 V	175	300	-	MHz
C_I	input capacitance		-	2.5	-	pF
C_{PD}	power dissipation capacitance	V_{CC} = 3.3 V [1] [2]	-	14	-	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in Volts;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

[2] The condition is V_I = GND to V_{CC}.

4. Ordering information

Table 2: Ordering information

Type number	Package			
	Temperature range	**Name**	**Description**	**Version**
74LVC1G175GW	–40 °C to +125 °C	SC-88	plastic surface mounted package; 6 leads	SOT363
74LVC1G175GV	–40 °C to +125 °C	SC-74	plastic surface mounted package; 6 leads	SOT457
74LVC1G175GM	–40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1.45 × 0.5 mm	SOT886

5. Functional diagram

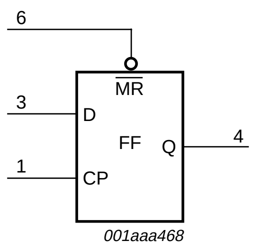


Fig 1. Logic symbol.

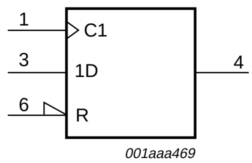


Fig 2. IEC logic symbol.

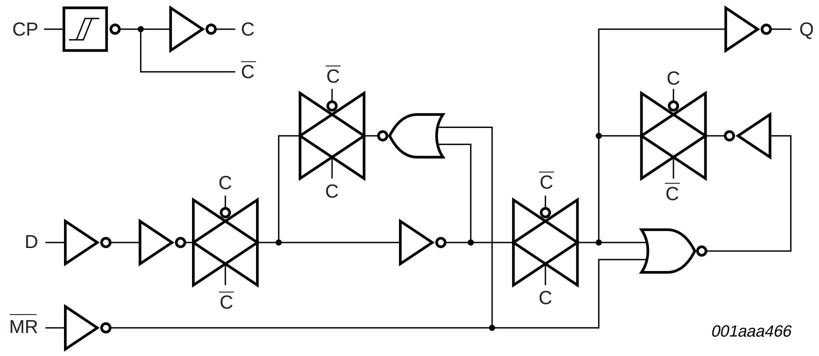


Fig 3. Logic diagram.

6. Pinning information

6.1 Pinning

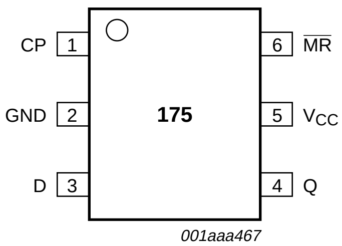


Fig 4. Pin configuration SC-88 and SC-74.

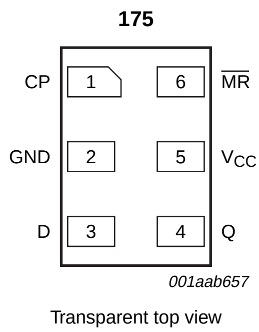


Fig 5. Pin configuration XSON6.

6.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
CP	1	clock input (LOW-to-HIGH, edge-triggered)
GND	2	ground (0 V)
D	3	data input
Q	4	flip-flop output
V_{CC}	5	supply voltage
$\overline{MR}$	6	master reset input (active LOW)

7. Functional description

7.1 Function table

Table 4: Function table [1]

Operating mode	Input			Output
	$\overline{MR}$	CP	D	Q
Reset (clear)	L	X	X	L
Load '1'	H	↑	h	H
Load '0'	H	↑	l	L

[1] H = HIGH voltage level;
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition;
L = LOW voltage level;
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition;
↑ = LOW-to-HIGH CP transition;
X = don't care.

8. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+6.5	V
I_{IK}	input diode current	$V_I < 0$ V		-	–50	mA
V_I	input voltage		[1]	–0.5	+6.5	V
I_{OK}	output diode current	$V_O > V_{CC}$ or $V_O < 0$ V		-	±50	mA
V_O	output voltage	active mode	[1] [2]	–0.5	V_{CC} + 0.5	V
		Power-down mode	[1] [2]	–0.5	+6.5	V
I_O	output diode current	V_O = 0 V to V_{CC}		-	±50	mA
I_{CC}, I_{GND}	V_{CC} or GND current			-	±100	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	power dissipation	T_{amb} = –40 °C to +125 °C		-	250	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] When V_{CC} = 0 V (Power-down mode), the output voltage can be 5.5 V in normal operation.

9. Recommended operating conditions

Table 6: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		1.65	5.5	V
V_I	input voltage		0	5.5	V
V_O	output voltage	active mode	0	V_{CC}	V
		Power-down mode; V_{CC} = 0 V	0	5.5	V

Table 6: Recommended operating conditions *...continued*

Symbol	Parameter	Conditions	Min	Max	Unit
T_{amb}	ambient temperature		–40	+125	°C
t_r, t_f	input rise and fall times	V_{CC} = 1.65 V to 2.7 V	0	20	ns/V
		V_{CC} = 2.7 V to 5.5 V	0	10	ns/V

10. Static characteristics

Table 7: Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = –40 °C to +85 °C [1]						
V_{IH}	HIGH-level input voltage	V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}	-	-	V
		V_{CC} = 2.3 V to 2.7 V	1.7	-	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	V
		V_{CC} = 4.5 V to 5.5 V	0.7 × V_{CC}	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.65 V to 1.95 V	-	-	0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	V
		V_{CC} = 4.5 V to 5.5 V	-	-	0.3 × V_{CC}	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = –100 µA; V_{CC} = 1.65 V to 5.5 V	V_{CC} – 0.1	-	-	V
		I_O = –4 mA; V_{CC} = 1.65 V	1.2	1.54	-	V
		I_O = –8 mA; V_{CC} = 2.3 V	1.9	2.15	-	V
		I_O = –12 mA; V_{CC} = 2.7 V	2.2	2.50	-	V
		I_O = –24 mA; V_{CC} = 3.0 V	2.3	2.62	-	V
		I_O = –32 mA; V_{CC} = 4.5 V	3.8	4.11	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = 100 µA; V_{CC} = 1.65 V to 5.5 V	-	-	0.10	V
		I_O = 4 mA; V_{CC} = 1.65 V	-	0.07	0.45	V
		I_O = 8 mA; V_{CC} = 2.3 V	-	0.12	0.30	V
		I_O = 12 mA; V_{CC} = 2.7 V	-	0.17	0.40	V
		I_O = 24 mA; V_{CC} = 3.0 V	-	0.33	0.55	V
		I_O = 32 mA; V_{CC} = 4.5 V	-	0.39	0.55	V
I_{LI}	input leakage current	V_I = 5.5 V or GND; V_{CC} = 5.5 V	-	±0.1	±5	µA
I_{off}	power OFF leakage current	V_I or V_O = 5.5 V; V_{CC} = 0 V	-	±0.1	±10	µA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V	-	0.1	10	µA
ΔI_{CC}	additional quiescent supply current per pin	V_I = V_{CC} – 0.6 V; I_O = 0 A; V_{CC} = 2.3 V to 5.5 V	-	5	500	µA
C_I	input capacitance		-	2.5	-	pF

Table 7: Static characteristics *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = −40 °C to +125 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}	-	-	V
		V_{CC} = 2.3 V to 2.7 V	1.7	-	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	V
		V_{CC} = 4.5 V to 5.5 V	0.7 × V_{CC}	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.65 V to 1.95 V	-	-	0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	V
		V_{CC} = 4.5 V to 5.5 V	-	-	0.3 × V_{CC}	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = −100 μA; V_{CC} = 1.65 V to 5.5 V	V_{CC} − 0.1	-	-	V
		I_O = −4 mA; V_{CC} = 1.65 V	0.95	-	-	V
		I_O = −8 mA; V_{CC} = 2.3 V	1.7	-	-	V
		I_O = −12 mA; V_{CC} = 2.7 V	1.9	-	-	V
		I_O = −24 mA; V_{CC} = 3.0 V	2.0	-	-	V
		I_O = −32 mA; V_{CC} = 4.5 V	3.4	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = 100 μA; V_{CC} = 1.65 V to 5.5 V	-	-	0.10	V
		I_O = 4 mA; V_{CC} = 1.65 V	-	-	0.70	V
		I_O = 8 mA; V_{CC} = 2.3 V	-	-	0.45	V
		I_O = 12 mA; V_{CC} = 2.7 V	-	-	0.60	V
		I_O = 24 mA; V_{CC} = 3.0 V	-	-	0.80	V
		I_O = 32 mA; V_{CC} = 4.5 V	-	-	0.80	V
I_{LI}	input leakage current	V_I = 5.5 V or GND; V_{CC} = 5.5 V	-	-	±20	μA
I_{off}	power OFF leakage current	V_I or V_O = 5.5 V; V_{CC} = 0 V	-	-	±20	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	40	μA
ΔI_{CC}	additional quiescent supply current per pin	V_I = V_{CC} − 0.6 V; I_O = 0 A; V_{CC} = 2.3 V to 5.5 V	-	-	5000	μA

[1] All typical values are measured at T_{amb} = 25 °C.

11. Dynamic characteristics

Table 8: Dynamic characteristics

GND = 0 V; see Figure 8

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb} = −40 °C to +85 °C [1]							
t_{PHL}, t_{PLH}	propagation delay CP to Q	see Figure 6					
		V_{CC} = 1.65 V to 1.95 V		1.5	4.9	13.4	ns
		V_{CC} = 2.3 V to 2.7 V		1.0	3.1	7.1	ns
		V_{CC} = 2.7 V		1.0	3.2	7.1	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	1.0	3.1	5.7	ns
		V_{CC} = 4.5 V to 5.5 V		1.0	2.2	4.0	ns
	propagation delay $\overline{MR}$ to Q	see Figure 7					
		V_{CC} = 1.65 V to 1.95 V		1.5	4.3	12.9	ns
		V_{CC} = 2.3 V to 2.7 V		1.0	2.8	7.0	ns
		V_{CC} = 2.7 V		1.0	3.0	7.0	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	1.0	2.5	5.8	ns
		V_{CC} = 4.5 V to 5.5 V		1.0	2.0	4.1	ns
t_W	clock pulse width HIGH or LOW	see Figure 6					
		V_{CC} = 1.65 V to 1.95 V		6.2	-	-	ns
		V_{CC} = 2.3 V to 2.7 V		2.7	-	-	ns
		V_{CC} = 2.7 V		2.7	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	2.7	1.3	-	ns
		V_{CC} = 4.5 V to 5.5 V		2.0	-	-	ns
	master reset pulse width LOW	see Figure 7					
		V_{CC} = 1.65 V to 1.95 V		6.2	-	-	ns
		V_{CC} = 2.3 V to 2.7 V		2.7	-	-	ns
		V_{CC} = 2.7 V		2.7	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	2.7	1.6	-	ns
		V_{CC} = 4.5 V to 5.5 V		2.0	-	-	ns
t_{rem}	removal time master reset	see Figure 7					
		V_{CC} = 1.65 V to 1.95 V		1.9	-	-	ns
		V_{CC} = 2.3 V to 2.7 V		1.4	-	-	ns
		V_{CC} = 2.7 V		1.3	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	1.2	0.4	-	ns
		V_{CC} = 4.5 V to 5.5 V		1.0	-	-	ns
t_{su}	set-up time D to CP	see Figure 6					
		V_{CC} = 1.65 V to 1.95 V		2.9	-	-	ns
		V_{CC} = 2.3 V to 2.7 V		1.7	-	-	ns
		V_{CC} = 2.7 V		1.7	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	1.3	0.5	-	ns
		V_{CC} = 4.5 V to 5.5 V		1.1	-	-	ns

Table 8: Dynamic characteristics *...continued*

GND = 0 V; see Figure 8

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_h	hold time D to CP	see Figure 6					
		V_{CC} = 1.65 V to 1.95 V		0.0	-	-	ns
		V_{CC} = 2.3 V to 2.7 V		0.3	-	-	ns
		V_{CC} = 2.7 V		0.5	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	1.2	0.2	-	ns
		V_{CC} = 4.5 V to 5.5 V		0.5	-	-	ns
f_{max}	maximum clock pulse frequency	see Figure 6					
		V_{CC} = 1.65 V to 1.95 V		80	125	-	MHz
		V_{CC} = 2.3 V to 2.7 V		175	-	-	MHz
		V_{CC} = 2.7 V		175	-	-	MHz
		V_{CC} = 3.0 V to 3.6 V	[2]	175	300	-	MHz
		V_{CC} = 4.5 V to 5.5 V		200	-	-	MHz
C_{PD}	power dissipation capacitance	V_{CC} = 3.3 V	[3] [4]	-	14	-	pF
T_{amb} = −40 °C to +125 °C							
t_{PHL}, t_{PLH}	propagation delay CP to Q	see Figure 6					
		V_{CC} = 1.65 V to 1.95 V		1.5	-	17	ns
		V_{CC} = 2.3 V to 2.7 V		1.0	-	9.0	ns
		V_{CC} = 2.7 V		1.0	-	9.0	ns
		V_{CC} = 3.0 V to 3.6 V		0.5	-	7.5	ns
		V_{CC} = 4.5 V to 5.5 V		0.5	-	5.5	ns
	propagation delay $\overline{MR}$ to Q	see Figure 7					
		V_{CC} = 1.65 V to 1.95 V		1.5	-	17	ns
		V_{CC} = 2.3 V to 2.7 V		1.0	-	9.0	ns
		V_{CC} = 2.7 V		1.0	-	9.0	ns
		V_{CC} = 3.0 V to 3.6 V		0.5	-	7.5	ns
		V_{CC} = 4.5 V to 5.5 V		0.5	-	5.5	ns
t_W	clock pulse width HIGH or LOW	see Figure 6					
		V_{CC} = 1.65 V to 1.95 V		6.2	-	-	ns
		V_{CC} = 2.3 V to 2.7 V		2.7	-	-	ns
		V_{CC} = 2.7 V		2.7	-	-	ns
		V_{CC} = 3.0 V to 3.6 V		2.7	-	-	ns
		V_{CC} = 4.5 V to 5.5 V		2.0	-	-	ns
	master reset pulse width LOW	see Figure 7					
		V_{CC} = 1.65 V to 1.95 V		6.2	-	-	ns
		V_{CC} = 2.3 V to 2.7 V		2.7	-	-	ns
		V_{CC} = 2.7 V		2.7	-	-	ns
		V_{CC} = 3.0 V to 3.6 V		2.7	-	-	ns
		V_{CC} = 4.5 V to 5.5 V		2.0	-	-	ns

Table 8: Dynamic characteristics *…continued*

GND = 0 V; see Figure 8

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{rem}	removal time master reset	see Figure 7				
		V_{CC} = 1.65 V to 1.95 V	1.9	-	-	ns
		V_{CC} = 2.3 V to 2.7 V	1.4	-	-	ns
		V_{CC} = 2.7 V	1.3	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	1.2	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	1.0	-	-	ns
t_{su}	set-up time D to CP	see Figure 6				
		V_{CC} = 1.65 V to 1.95 V	2.9	-	-	ns
		V_{CC} = 2.3 V to 2.7 V	1.7	-	-	ns
		V_{CC} = 2.7 V	1.7	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	1.3	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	1.1	-	-	ns
t_h	hold time D to CP	see Figure 6				
		V_{CC} = 1.65 V to 1.95 V	0.0	-	-	ns
		V_{CC} = 2.3 V to 2.7 V	0.3	-	-	ns
		V_{CC} = 2.7 V	0.5	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	1.2	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	0.5	-	-	ns
f_{max}	maximum clock pulse frequency	see Figure 6				
		V_{CC} = 1.65 V to 1.95 V	80	-	-	MHz
		V_{CC} = 2.3 V to 2.7 V	175	-	-	MHz
		V_{CC} = 2.7 V	175	-	-	MHz
		V_{CC} = 3.0 V to 3.6 V	175	-	-	MHz
		V_{CC} = 4.5 V to 5.5 V	200	-	-	MHz

[1] All typical values are measured at T_{amb} = 25 °C.

[2] These typical values are measured at V_{CC} = 3.3 V.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

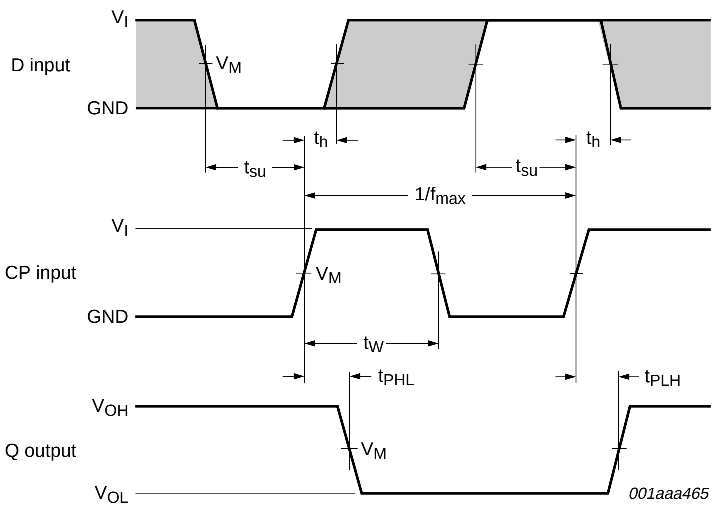
V_{CC} = supply voltage in Volts;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

[4] The condition is V_I = GND to V_{CC}.

12. Waveforms



Measurement points are given in Table 9.

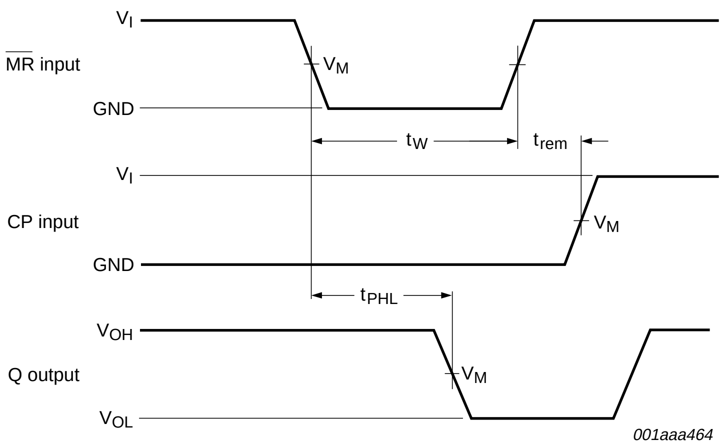
The shaded areas indicate when the input is permitted to change for predictable output performance.

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig 6. The clock input (CP) to output (Q) propagation delays, the clock pulse width, the D to CP set-up, the CP to D hold times and the maximum clock pulse frequency.

Table 9: Measurement points

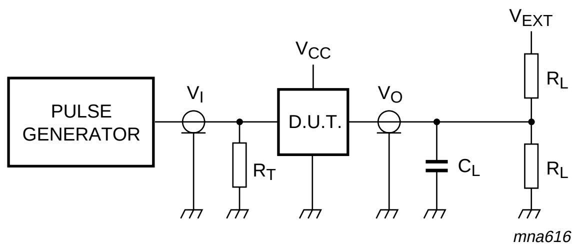
Supply voltage	Output	Input		
V_{CC}	V_M	V_M	V_I	$t_r = t_f$
1.65 V to 1.95 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	V_{CC}	≤ 2.0 ns
2.3 V to 2.7 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	V_{CC}	≤ 2.0 ns
2.7 V	1.5 V	1.5 V	2.7 V	≤ 2.5 ns
3.0 V to 3.6 V	1.5 V	1.5 V	2.7 V	≤ 2.5 ns
4.5 V to 5.5 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	V_{CC}	≤ 2.5 ns



Measurement points are given in Table 9.

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig 7. The master reset ($\overline{MR}$) input to output (Q) propagation delays, the master reset pulse width and the $\overline{MR}$ to CP removal time.



Test data is given in Table 10.

Definitions for test circuit:
R_L = Load resistor.
C_L = Load capacitance including jig and probe capacitance.
R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

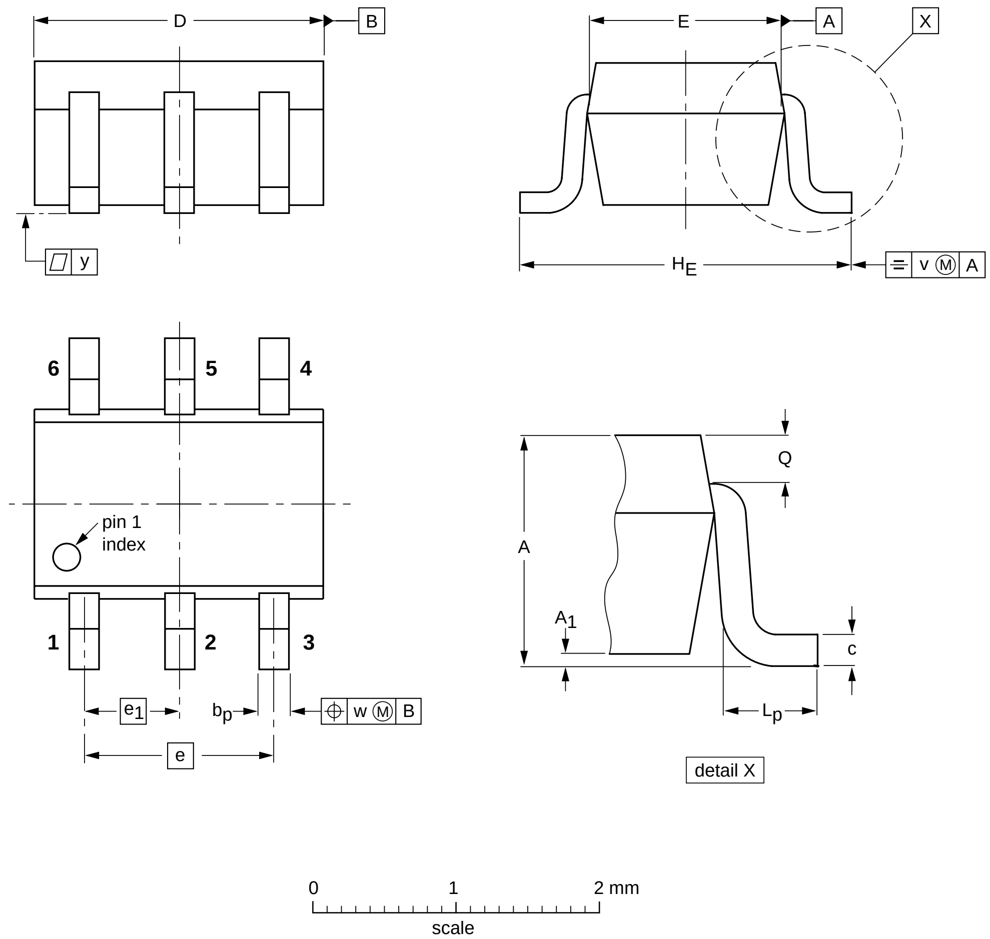
Fig 8. Load circuitry for switching times.

Table 10: Test data

Supply voltage	Input	Load		V_{EXT}		
V_{CC}	V_I	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
1.65 V to 1.95 V	V_{CC}	30 pF	1 kΩ	open	GND	2 × V_{CC}
2.3 V to 2.7 V	V_{CC}	30 pF	500 Ω	open	GND	2 × V_{CC}
2.7 V	2.7 V	50 pF	500 Ω	open	GND	6 V
3.0 V to 3.6 V	2.7 V	50 pF	500 Ω	open	GND	6 V
4.5 V to 5.5 V	V_{CC}	50 pF	500 Ω	open	GND	2 × V_{CC}

13. Package outline

Plastic surface mounted package; 6 leads **SOT363**



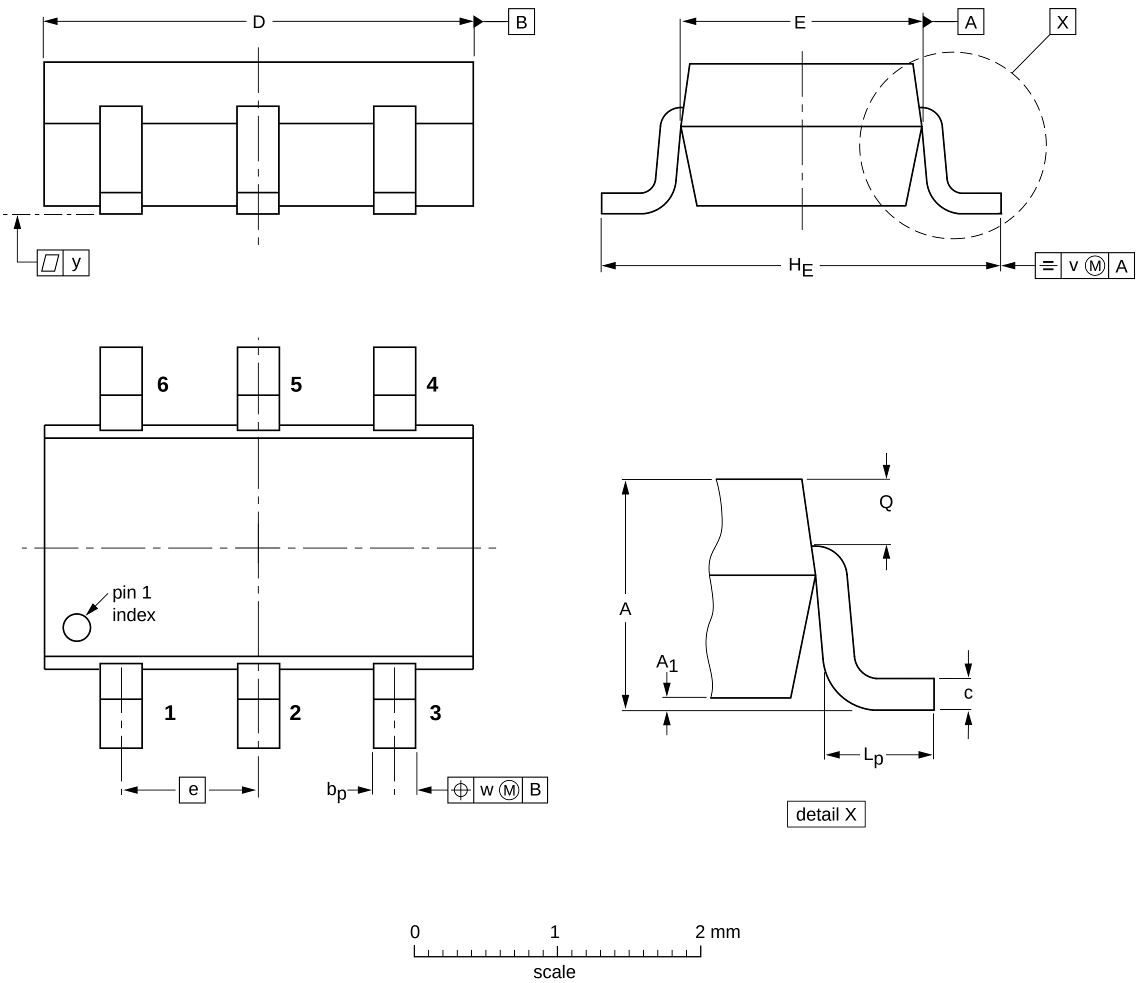
DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.8	0.1	0.30 0.20	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.25 0.15	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT363			SC-88			97-02-28

Fig 9. Package outline SOT363 (SC-88).

Plastic surface mounted package; 6 leads **SOT457**



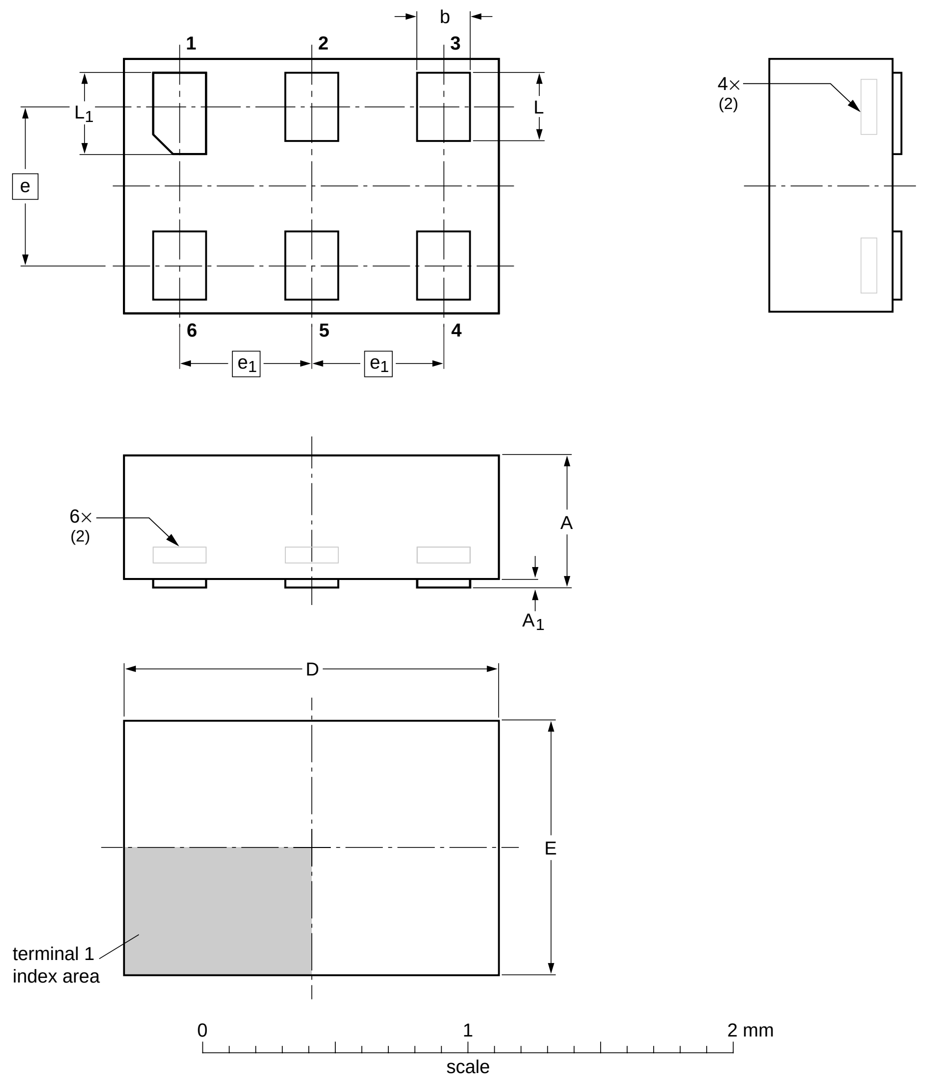
DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	c	D	E	e	H_E	L_p	Q	v	w	y
mm	1.1 0.9	0.1 0.013	0.40 0.25	0.26 0.10	3.1 2.7	1.7 1.3	0.95	3.0 2.5	0.6 0.2	0.33 0.23	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT457			SC-74			~~97-02-28~~ 01-05-04

Fig 10. Package outline SOT457 (SC-74).

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm **SOT886**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max	A_1 max	b	D	E	e	e_1	L	L_1
mm	0.5	0.04	0.25 0.17	1.5 1.4	1.05 0.95	0.6	0.5	0.35 0.27	0.40 0.32

Notes

1. Including plating thickness.
2. Can be visible in some manufacturing processes.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT886		MO-252				~~04-07-15~~ 04-07-22

Fig 11. Package outline SOT886 (XSON6).

14. Revision history

Table 11: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
74LVC1G175_2	20041018	Product data sheet	-	9397 750 13762	74LVC1G175_1
Modifications	• Package outline. Marking code and ESD data added.				
74LVC1G175_1	20040318	Product data sheet	-	9397 750 12973	-

15. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

16. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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19. Contents

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