Low-Voltage Dual SPST Analog Switch

FEATURES

- Wide Operation Voltage (+2.7 to +12 V)
- Low Charge Injection - Q_{INJ}: 1 pC
- Low Power Consumption
- TTL/CMOS Logic Compatible Over The Full Operating Voltage range
- Available in MSOP-8 and SOT23-8

BENEFITS

- Reduced Power Consumption
- Simple Logic Interface
- High Accuracy
- Reduce Board Space

APPLICATIONS

- Battery Operated Systems
- Portable Test Equipment
- Sample and Hold Circuits
- Cellular Phones
- Communication Systems
- Military Radio
- PBX, PABX Guidance and Control Systems

DESCRIPTION

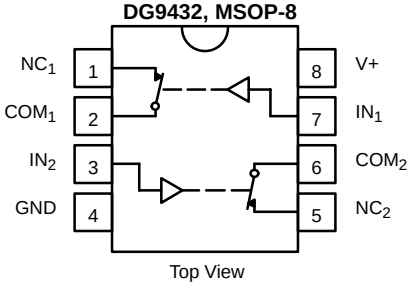
The DG9432/9433/9434 is a dual single-pole/single-throw monolithic CMOS analog switch designed for high performance switching of analog signals. Combining low power, high speed (t_{ON}: 25 ns, t_{OFF}: 20 ns), the DG9432/9433/9434 is ideal for portable and battery powered applications requiring high performance and efficient use of board space.

The DG9432/9433/9434 is built on Vishay Siliconix's low voltage BCD-15 process. An epitaxial layer prevents latchup. Break-before -make is guaranteed for DG9432/9433/9434.

Each switch conducts equally well in both directions when on, and blocks up to the power supply level when off.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION—DG9432

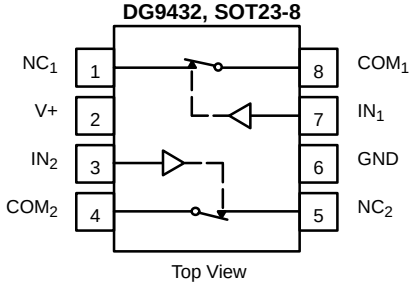
DG9432, MSOP-8



Top View

Device Marking: 9432

DG9432, SOT23-8



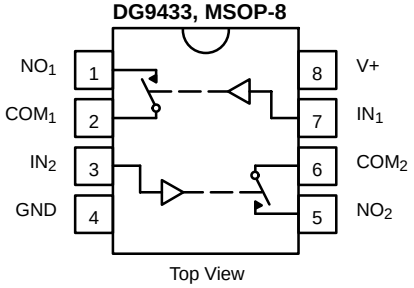
Top View

Device Marking: 4G

TRUTH TABLE DG9432	
Logic	**Switch**
0	On
1	Off

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION—DG9433/DG9434

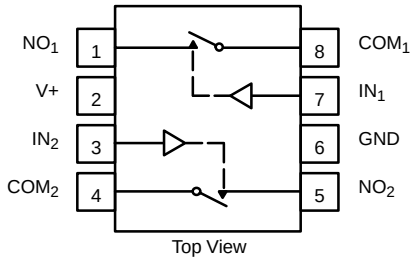
DG9433, MSOP-8



Top View

Device Marking: 9433

DG9433. SOT23-8

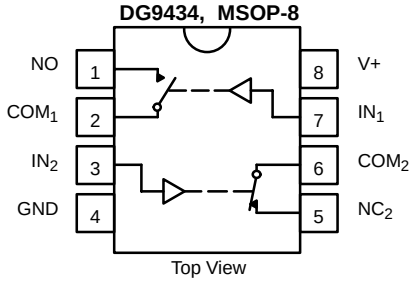


Top View

Device Marking: 4H

TRUTH TABLE DG9433	
Logic	**Switch**
0	Off
1	On

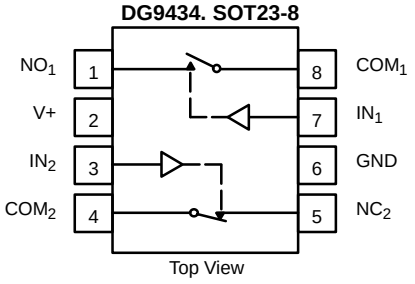
DG9434, MSOP-8



Top View

Device Marking: 9434

DG9434. SOT23-8



Top View

Device Marking: 4I

TRUTH TABLE DG9434		
Logic	**Switch-1**	**Switch-2**
0	Off	On
1	On	Off

ORDERING INFORMATION		
Temp Range	**Package**	**Part Number**
-40 to 85°C	MSOP-8	DG9432DQ
		DG9433DQ
		DG9434DQ
	SOT23-8	DG9432DS
		DG9433DS
		DG9434DS

ABSOLUTE MAXIMUM RATINGS

Reference to GND

V+ ..... -0.3 to +13.5 V

IN, COM, NC, NO[a] ..... -0.3 to (V+ + 0.3 V)

Continuous Current (Any terminal) ..... ±10 mA

Peak Current ..... ±20 mA

(Pulsed at 1ms, 10% duty cycle)

Storage Temperature (D Suffix) ..... -65 to 150°C

Power Dissipation (Packages)[b]

MSOP-8[c] ..... 320 mW

SOT23-8[c] ..... 515 mW

Notes:
a. Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 6.5 mW/°C above 75°C

SPECIFICATIONS (V+ = 3 V)

Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 3.3 V, ±10%, V_{IN} = 0.4 or 1.8 V[e]	Temp[a]	Limits -40 to 85°C Min[c]	Typ[b]	Max[c]	Unit
Switch On Resistance							
Analog Signal Range[e]	V_{ANALOG}		Full	V-		V+	V
Drain-Source On-Resistance	$r_{(on)}$	V+ = 2.7 V, I_{COM} = 1 mA, V_{COM} = 1.5 V	Room Full		81	100 120	Ω
$r_{(on)}$ Match[d]	$\Delta r_{(on)}$		Room		0.4	3.0	
Digital Control							
Input, High Voltage	V_{INH}	V+ Ranges 2.7 to 5 V	Full	1.8			V
Input, Low Voltage	V_{INL}		Full			0.4	
Input Current	I_{INH}			-1		1	µA
Dynamic Characteristics							
Break-Before-Make[d,g]	t_{OPEN}	V+ = 3 V, R_L = 300 Ω V_{NO} = V_{NC} = 1.5 V C_L = 35 pF, V_{IN} = 0 V, 3 V	Room Full	1			ns
Turn-OnTime[d]	t_{ON}		Room Full		60	80 100	
Turn-OffTime[d]	t_{OFF}		Room Full		14	25 35	
Charge Injection[d]	Q	C_L = 1 nF, R_{GEN} = 0 Ω, Vg = 0 V	Room		0.16		pC
Off-Isolation[d]	OIRR	C_L = 5 pF, R_L = 50 Ω, f = 1 MHz	Room		77		dB
		C_L = 5 pF, R_L = 50 Ω, f = 10 MHz	Room		55		
Crosstalk[d]	X_{TALK}	R_L = 50 Ω, f = 1 MHz, V+ = 2.5 V	Room		98		
Source Off Capacitance[d]	$C_{NC/NO(off)}$	f = 1 MHz, $V_{NC/NO}$ = 0 V	Room		7.5		pF
Drain Off Capacitance[d]	$C_{COM(off)}$	f = 1 MHz, V_{COM} = 0 V	Room		7.8		
Drain On Capacitance[d]	$C_{COM(on)}$		Room		22		
Supply Current	I_+	V+ = 3.3 V, V_{IN} = 0 or V+	Room	-1		-1	µA

Notes:
a. Room = 25°C, Full = as determined by the operating suffix.
b. Typical values are for design aid only, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Guarantee by design, not subjected to production test.
e. V_{IN} = input voltage to perform proper function.
f. Guaranteed by 12-V leakage testing, not production tested.
g. Applies for DG9434 only.

SPECIFICATIONS (V+ = 5 V)

Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 5 V, ±10%, V_{IN} = 0.4 or 1.8 V[e]	Temp[a]	Limits -40 to 85°C Min[c]	Typ[b]	Max[c]	Unit
Switch On Resistance							
Analog Signal Range[e]	V_{ANALOG}		Full	V_-		V_+	V
Drain-Source On-Resistance	$r_{(on)}$	V_+ = 4.5 V, I_{COM} = 1 mA, V_{COM} = 2.5 or 3.5 V	Room Full		39	60 70	Ω
$r_{DS(on)}$ Match	$\Delta r_{(on)}$	V_+ = 4.5 V, I_{COM} = 1 mA, V_{COM} = 3.5 V	Room		0.3	3.0	
Switch Off Leakage Current[f]	$I_{NC/NO(off)}$	V_+ = 5 V, V_{COM} = 0.5 V, 4.5 V $V_{NC/NO}$ = 4.5 V, 0.5 V	Room Full	-1 -10	0.3	1 10	nA
	$I_{COM(off)}$		Room Full	-1 -10	0.3	1 10	
Channel On Leakage Current[f]	$I_{COM(on)}$		Room Full	-1 10	0.3	1 10	
Digital Control							
Input, High Voltage	V_{INH}	V+ Ranges 2.7 to 5 V	Full	1.8			V
Input, Low Voltage	V_{INL}		Full			0.4	
Input Current	I_{INH}			-1		1	µA
Dynamic Characteristics							
Break-Before-Make[d,g]	t_{OPEN}	V_+ = 5 V, R_L = 300 Ω V_{NO} = V_{NC} = 3 V C_L = 35 pF, V_{IN} = 0 V, 5 V	Room Full	1			ns
Turn-OnTime	t_{ON}		Room Full		33	60 70	
Turn-OffTime	t_{OFF}		Room Full		10	20 30	
Charge Injection[d]	Q	C_L = 1 nF, R_{GEN} = 0 Ω, V_g = 0 V	Room		0.56		pC
Off-Isolation[d]	OIRR	C_L = 5 pF, R_L = 50 Ω, f = 1 MHz	Room		76		dB
		C_L = 5 pF, R_L = 50 Ω, f = 10 MHz, V_+ = 5 V	Room		54		
Crosstalk[d]	X_{TALK}	R_L = 50 Ω, f = 1 MHz, V_+ = 5 V	Room		96		
Source Off Capacitance[d]	$C_{NC/NO(off)}$	f = 1 MHz, $V_{NO/NC}$ = 0 V	Room		7.5		pF
Drain Off Capacitance[d]	$C_{COM(off)}$	f = 1 MHz, V_{COM} = 0 V	Room		7.8		
Drain On Capacitance[d]	$C_{COM(on)}$		Room		22		
Supply Current	I_+	V_+ = 5.5 V, V_{IN} = 0 or V_+	Room	-1		-1	µA

Notes:

a. Room = 25°C, Full = as determined by the operating suffix.
b. Typical values are for design aid only, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Guarantee by design, not subjected to production test.
e. V_{IN} = input voltage to perform proper function.
f. Guaranteed by 12-V leakage testing, not production tested.
g. Applies to DG9434 only.

SPECIFICATIONS (V+ = 12 V)

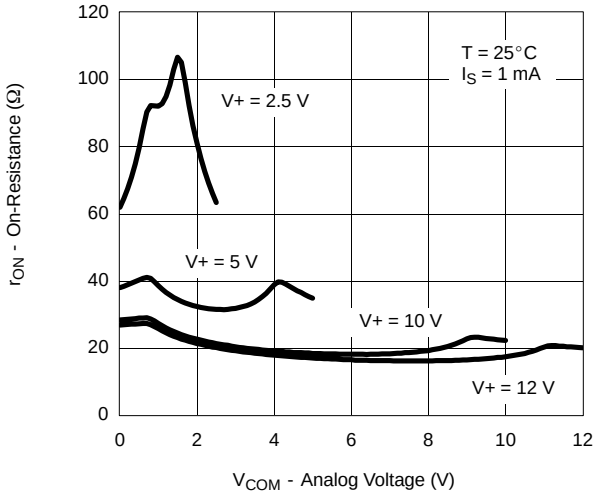
Parameter	Symbol	Test Conditions Otherwise Unless Specified V_+ = 12 V, ±10%, V_{IN} = 0.8 or 2.4 V[e]	Temp[a]	Limits -40 to 85°C Min[c]	Typ[b]	Max[c]	Unit
Switch On Resistance							
Analog Signal Range[e]	V_{ANALOG}		Full	V_-		V_+	V
Drain-Source On-Resistance	$r_{(on)}$	V_+ = 10.8 V, I_{COM} = 1 mA, V_{COM} = 9 V	Room Full		19	30 40	Ω
$r_{DS(on)}$ Match	$\Delta r_{(on)}$	V_+ = 10.8 V, I_{COM} = 1 mA, V_{COM} = 9 V	Room		0.3	3.0	
Switch Off Leakage Current[a]	$I_{NC/NO(off)}$	V_+ = 12 V, V_S = 1/11 V, V_{COM} = 11/1 V	Room Full	-1 -10	0.3	1 10	nA
	$I_{COM(off)}$		Room Full	-1 -10	0.3	1 10	
Channel On Leakage Current[a]	$I_{COM(on)}$		Room Full	-1 10	0.3	1 10	
Digital Control							
Input, High Voltage	V_{INH}	V+ = 12 V	Full			2.4	V
Input, Low Voltage	V_{INL}		Full	0.8			
Input Current	I_{INH}			-1		1	µA
Dynamic Characteristics							
Break-Before-Make[d,g]	t_{OPEN}	V_+ = 12 V, R_L = 300 Ω V_{NO} = V_{NC} = 8 V C_L = 35 pF, V_{IN} = 0 V, 12 V	Room Full	1			ns
Turn-OnTime	t_{ON}		Room Full		21	35 40	
Turn-OffTime	t_{OFF}		Room Full		6	18 25	
Charge Injection[d]	Q	C_L = 1 nF, R_{GEN} = 0 Ω, V_g = 0 V, V_+ = 5 V	Room		0.36		pC
Off-Isolation[d]	OIRR	C_L = 5 pF, R_L = 50 Ω, f = 1 MHz	Room		75		dB
		C_L = 5 pF, R_L = 50 Ω, f = 10 MHz	Room		53		
Crosstalk[d]	X_{TALK}	R_L = 50 Ω, f = 1 MHz, V_+ = 5 V	Room		96		
Source Off Capacitance[d]	$C_{NC/NO(off)}$	f = 1 MHz, $V_{NC/NO}$ = 0 V	Room		7.5		pF
Drain Off Capacitance[d]	$C_{COM(off)}$	f = 1 MHz, V_{COM} = 0 V	Room		7.8		
Drain On Capacitance[d]	$C_{COM(on)}$		Room		22		
Supply Current	I_+	V_+ = 12 V, V_{IN} =0 or V+	Room	-1		-1	µA

Notes:

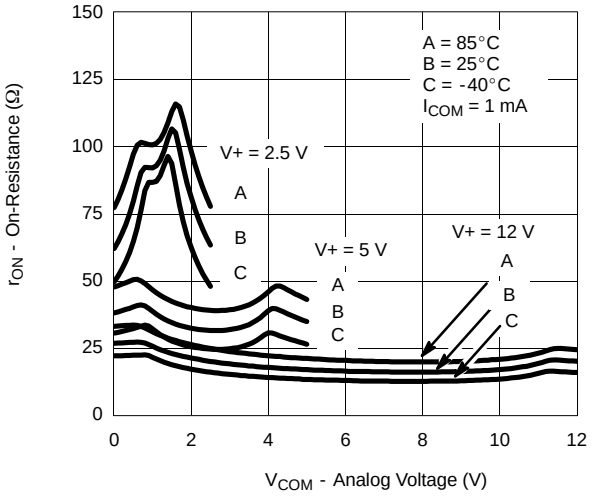
a. Room = 25°C, Full = as determined by the operating suffix.
b. Typical values are for design aid only, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Guarantee by design, not subjected to production test.
e. V_{IN} = input voltage to perform proper function.
f. Guaranteed by 12-V leakage testing, not production tested.
g. Applies for DG9434 only.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

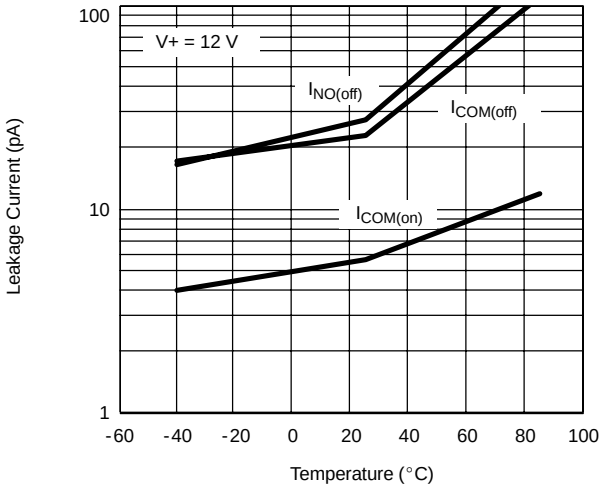
r_{ON} vs. V_{COM} and Single Supply Voltage



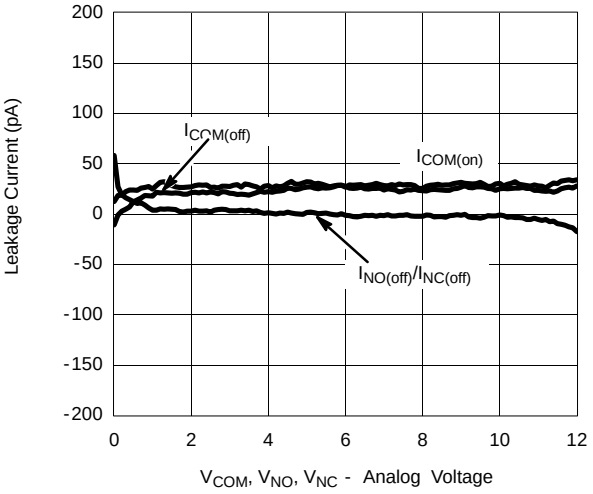
r_{ON} vs. Analog Voltage and Temperature



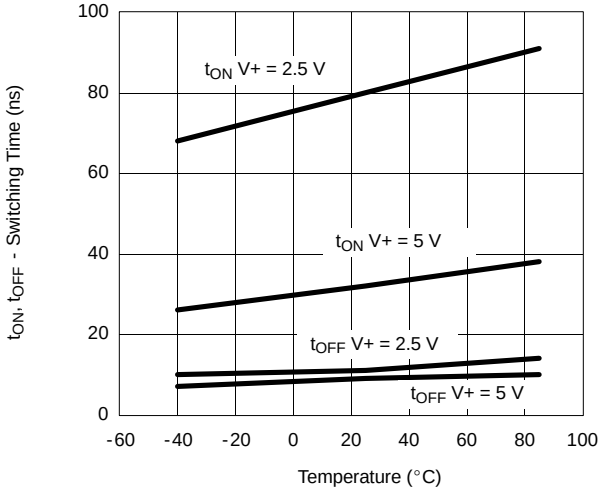
Leakage Current vs. Temperature



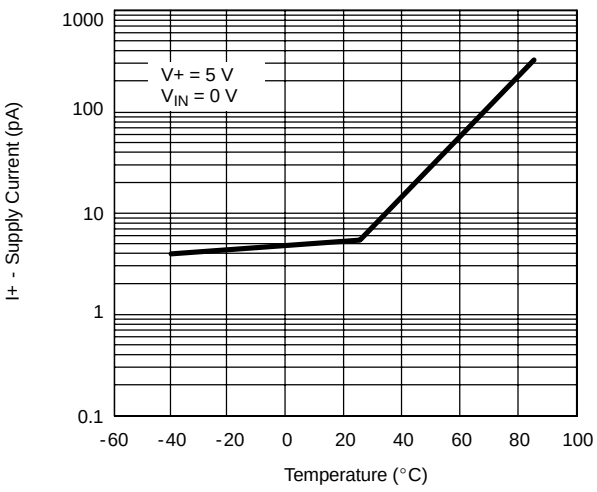
Leakage Current vs. Analog Voltage



Switching Time vs. Temperature

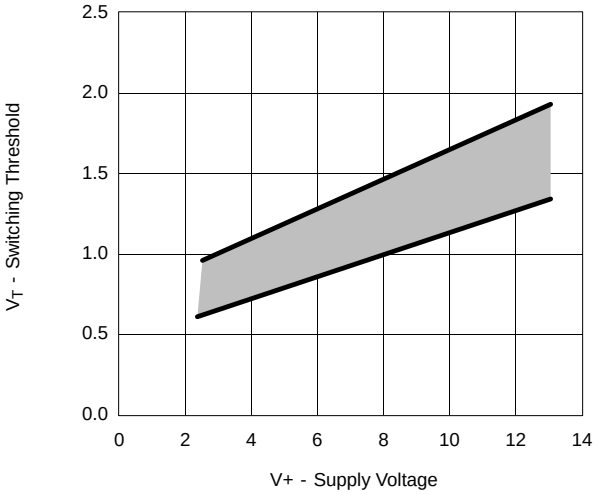


Suppy Current vs. Temperature

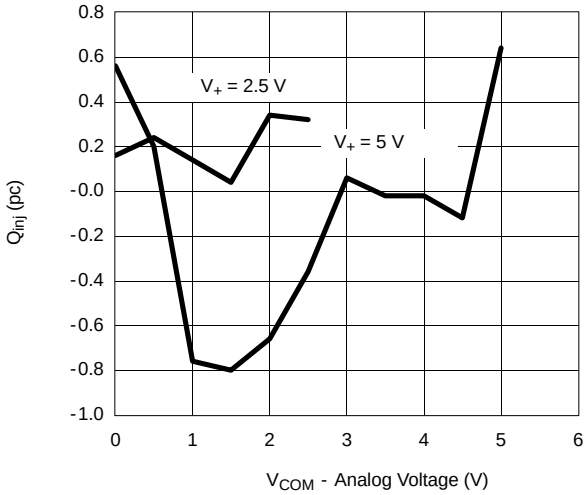


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

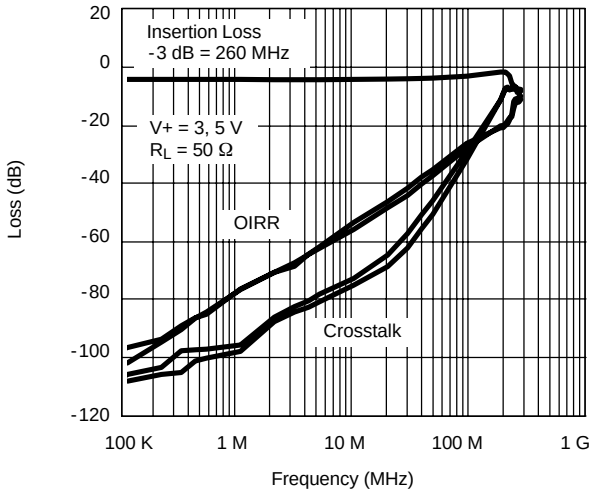
Switching Threshold vs. Supply Voltage



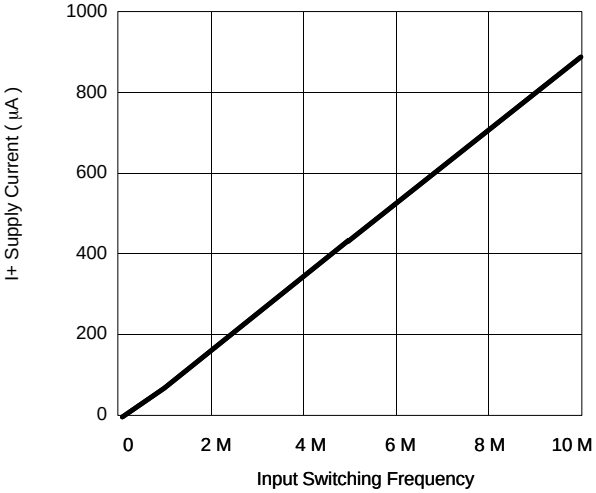
Charge Injection at Source



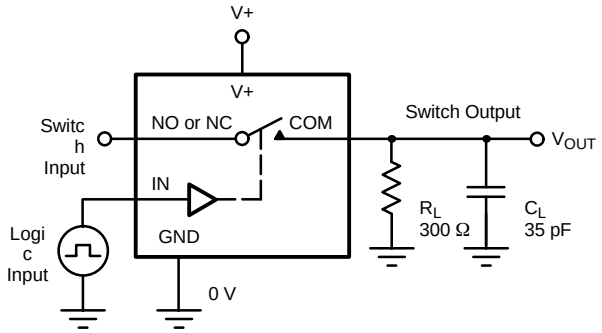
Insertion Loss, Off Isolation and Crosstalk vs. Frequency



Supply Current vs. Input Switching Frequency

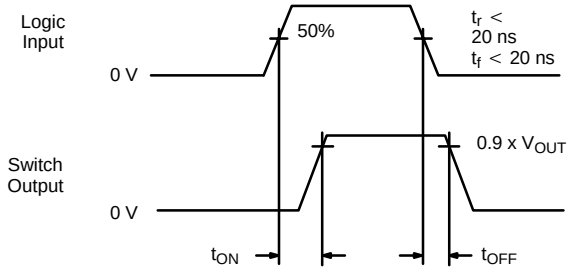


TEST CIRCUITS



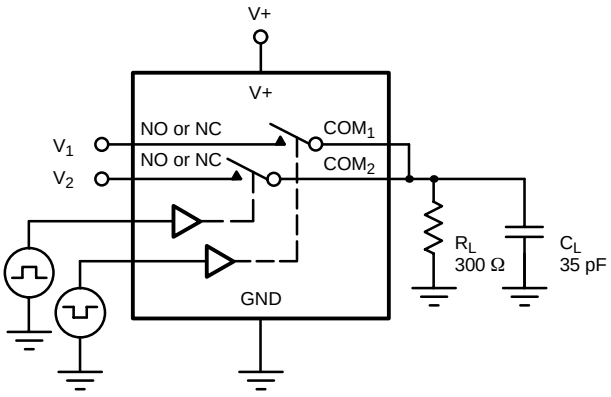
C_L (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM}\left(\frac{R_L}{R_L + R_{ON}}\right)$$



Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

FIGURE 1. Switching Time



C_L (includes fixture and stray capacitance)

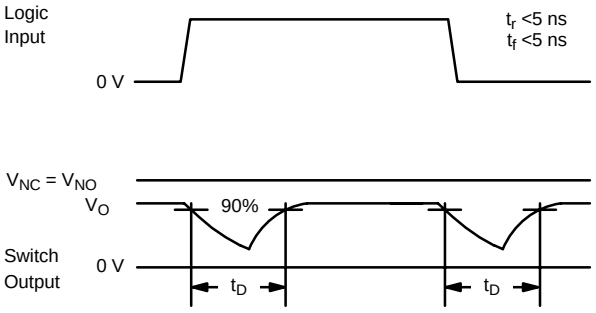
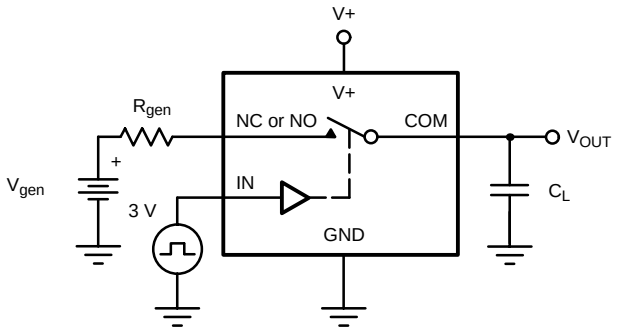
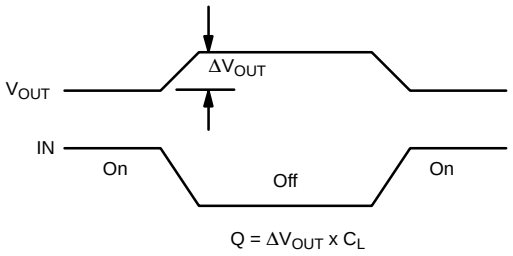


FIGURE 2. Break-Before-Make Interval





$Q = \Delta V_{OUT} \times C_L$

IN depends on switch configuration: input polarity determined by sense of switch.

FIGURE 3. Charge Injection

TEST CIRCUITS

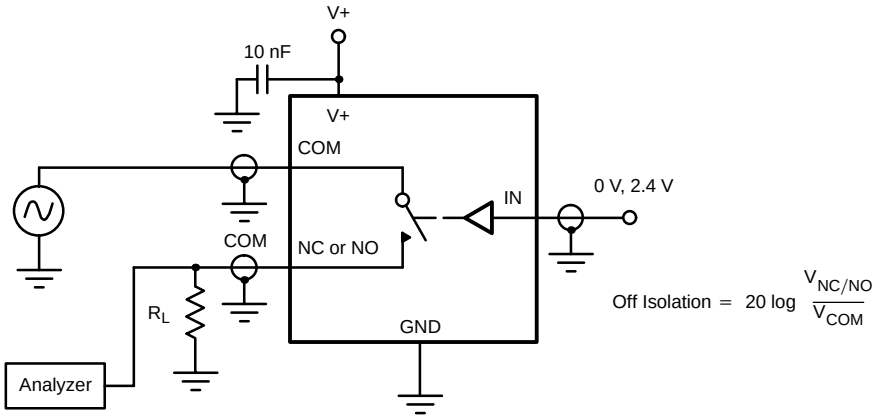


FIGURE 4. Off-Isolation

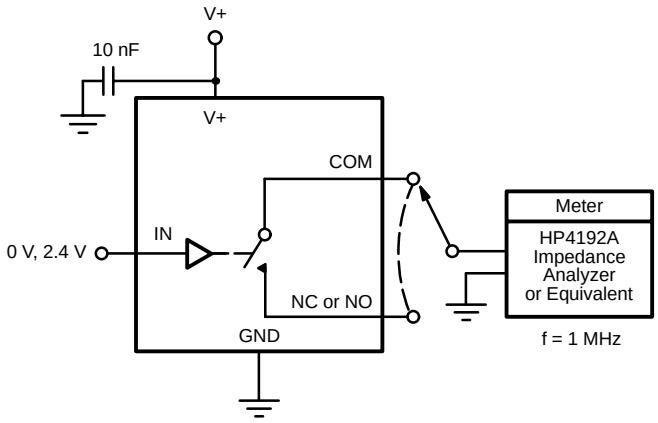


FIGURE 5. Channel Off/On Capacitance