DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4720B
HEF4720V
LSI
256-bit, 1-bit per word random access memories

Product specification
File under Integrated Circuits, IC04

January 1995

Philips Semiconductors

256-bit, 1-bit per word random access memories

HEF4720B HEF4720V

DESCRIPTION

The HEF4720B and HEF4720V are 256-bit, 1-bit per word random access memories with 3-state outputs. The memories are fully decoded and completely static.

Recommended supply voltage range for HEF4720B is 3 to 15 V and for HEF4720V is 4,5 to 12,5 V; minimum stand-by voltage for both types is 3 V.

The use of LOCMOS gives the added advantage of very low stand-by power. The circuits can be directly interfaced with standard bipolar devices (TTL) without using special interface circuits. The memory operates from a single power supply. The separate chip select input ($\overline{CS}$) allows simple memory expansion when the outputs are wire-ORed. If $\overline{CS}$ is HIGH, the outputs are floating and no new information can be written into the memory. The signal at O has the same polarity as the data input D, while the signal at $\overline{O}$ is the complement of the signal at O. The write control W must be HIGH for writing into the memory.

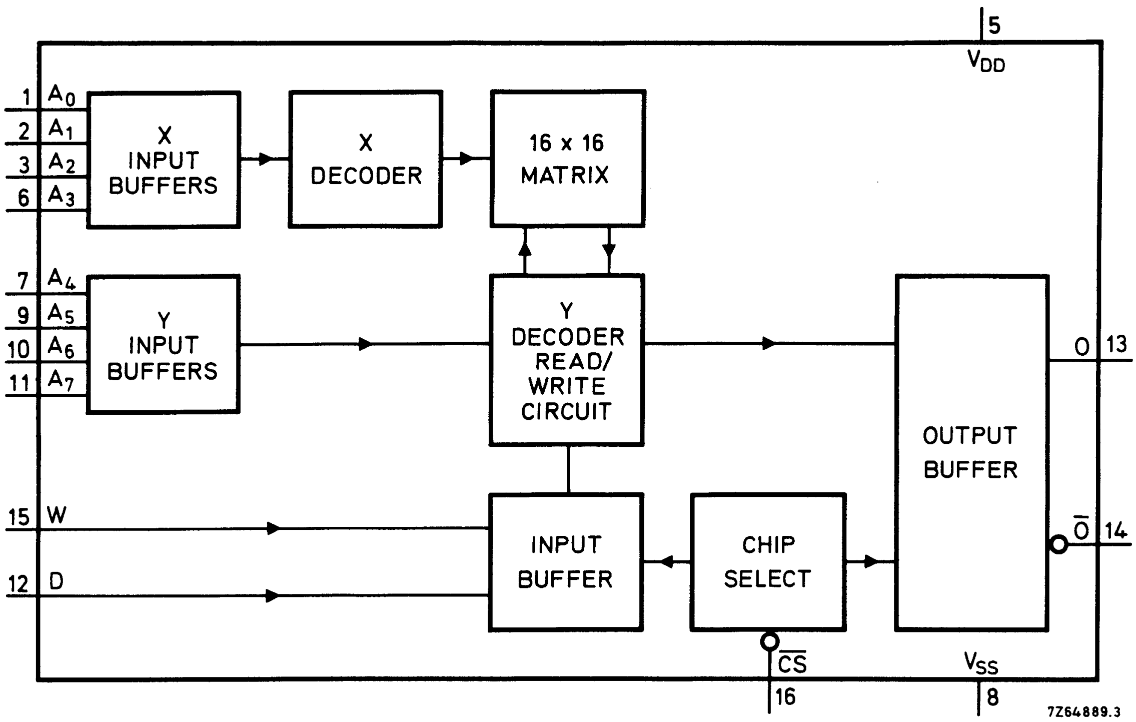


Fig.1 Functional diagram.

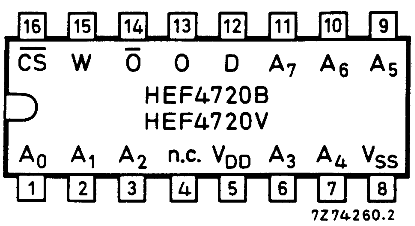


Fig.2 Pinning diagram.

HEF4720BP;	HEF4720VP(N):	16-lead DIL; plastic (SOT38-1)
HEF4720BD;	HEF4720VD(F):	16-lead DIL; ceramic (cerdip) (SOT74)
HEF4720BT;	HEF4720VT(D):	16-lead SO; plastic (SOT109-1)

( ): Package Designator North America

FAMILY DATA

See Family Specifications.

I_{DD} LIMITS

See below.

FUNCTION TABLE

$\overline{CS}$	W	O	$\overline{O}$	MODE
L	H	data written into memory	complement of data written into memory	write
L	L	data written into memory	complement of data written into memory	read
H	X	Z	Z	inhibit

Notes

1. H = HIGH state (the more positive voltage)
   L = LOW state (the less positive voltage)
   X = state is immaterial
   Z = high impedance OFF-state

PINNING

$\overline{CS}$	chip select input (active LOW)
W	write enable input
D	data input
A_0 to A_7	address inputs
O	3-state output (active HIGH)
$\overline{O}$	3-state output (active LOW)

SUPPLY VOLTAGE

	RATING	RECOMMENDED OPERATING	STAND-BY MIN.	
HEF4720B	–0,5 to 18	3,0 to 15,0	3	V
HEF4720V	–0,5 to 18	4,5 to 12,5	3	V

The values given at V_{DD} = 15 V in the following DC and AC characteristics, are not applicable to the HEF4720V, because of its lower supply voltage range.

DC CHARACTERISTICS

V_{SS} = 0 V

	V_{DD} V	V_{OL} V	SYMBOL	T_{amb} (°C) –40 MIN.	–40 MAX.	+25 MIN.	+25 MAX.	+85 MIN.	+85 MAX.	
Output current LOW	4,75	0,4	I_{OL}	2,4		2		1,6		mA
	10	0,5		4,8		4		3,2		mA
	15	1,5		10,0		10		7,5		mA
Quiescent device current	5		I_{DD}		25		25		200	µA
	10				50		50		400	µA
	15				100		100		800	µA
Input leakage current			$\pm I_{IN}$							
HEF4720V	10				0,3		0,3		1	µA
HEF4720B	15				0,3		0,3		1	µA

AC CHARACTERISTICS

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.		
Output capacitance	5	C_O		5		pF	
	10			5		pF	
	15			5		pF	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA
Read cycle							
Read access time	5	t_{ACC}		320	580	ns	292 ns + (0,55 ns/pF) C_L
	10			130	220	ns	118 ns + (0,23 ns/pF) C_L
	15			100	160	ns	92 ns + (0,16 ns/pF) C_L
Chip select to output time	5	t_{CO}			180	ns	
	10				70	ns	
	15				50	ns	
Address hold time	5	t_{OA}	0			ns	
	10		0			ns	
	15		0			ns	
Output hold time with respect to address input	5	t_{VAL1}	60	170		ns	142 ns + (0,55 ns/pF) C_L
	10		20	50		ns	38 ns + (0,23 ns/pF) C_L
	15		15	40		ns	32 ns + (0,16 ns/pF) C_L
Output hold time with respect to chip select input	5	t_{COH}			130	ns	
	10				70	ns	
	15				60	ns	
Output floating time with respect to chip select input	5	t_{COF}	0			ns	
	10		0			ns	
	15		0			ns	
Read cycle time	5	t_{RC}	580			ns	
	10		220			ns	
	15		160			ns	
Output transition times LOW to HIGH	5	t_{TLH}		60	120	ns	10 ns + (1,0 ns/pF) C_L
	10			30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
HIGH to LOW	5	t_{THL}		40	80	ns	14 ns + (0,52 ns/pF) C_L
	10			22	40	ns	11 ns + (0,22 ns/pF) C_L
	15			15	30	ns	7 ns + (0,16 ns/pF) C_L

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.		
Write cycle							
Write cycle time	5	t_{WC}	580			ns	
	10		220			ns	
	15		160			ns	
Address to write set-up time	5	t_{AW}	110			ns	
	10		50			ns	
	15		50			ns	
Write pulse width	5	t_{WP}	370		10 000	ns	
	10		130		10 000	ns	
	15		80		10 000	ns	
Write recovery time	5	t_{WR}	100			ns	
	10		40			ns	
	15		30			ns	
Data set-up time	5	t_{DW}	250			ns	
	10		100			ns	
	15		80			ns	
Data hold time	5	t_{DH}	100			ns	
	10		30			ns	
	15		20			ns	
Chip select set-up time with respect to write pulse	5	t_{CSW}	370			ns	
	10		130			ns	
	15		80			ns	
Chip select hold time with respect to write pulse	5	t_{CSH}	0			ns	
	10		0			ns	
	15		0			ns	
Chip select lead time over write pulse to prevent writing	5	t_{CSL}	0			ns	
	10		0			ns	
	15		0			ns	

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.	
Read-modify-write cycle						
Read enable hold time	5	t_{RH}	0			ns
	10		0			ns
	15		0			ns
Output hold time with respect to write pulse	5	t_{VAL2}	60			ns
	10		20			ns
	15		15			ns
Read-modify-write cycle time	5	t_{RWC}	1050			ns
	10		390			ns
	15		270			ns

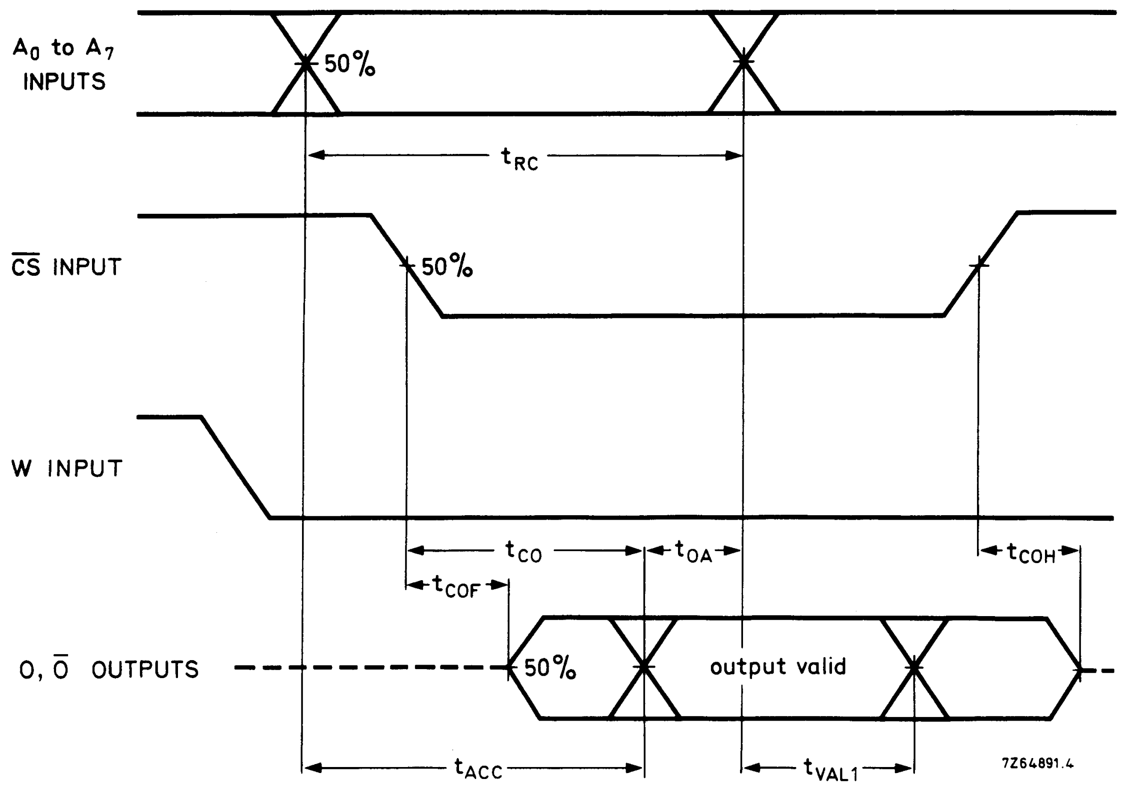


Fig.3 Read cycle timing diagram.

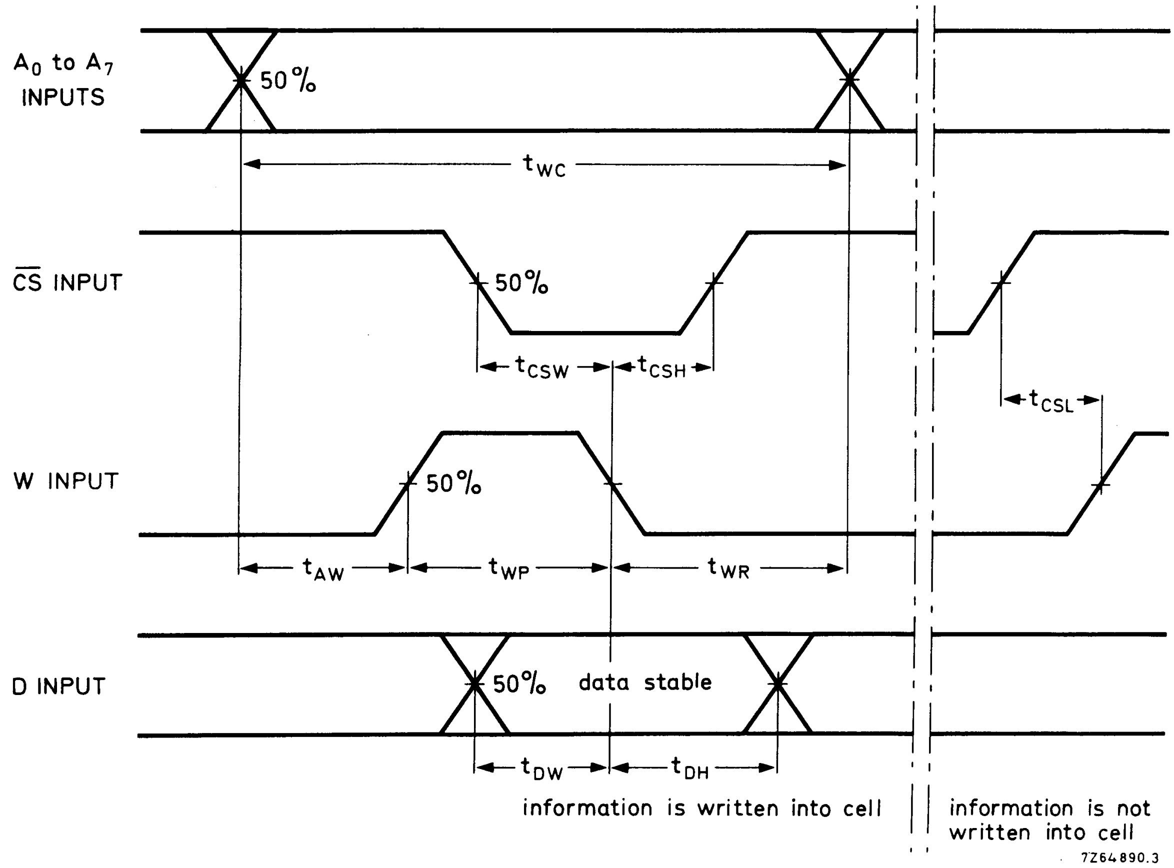


Fig.4 Write cycle timing diagram.

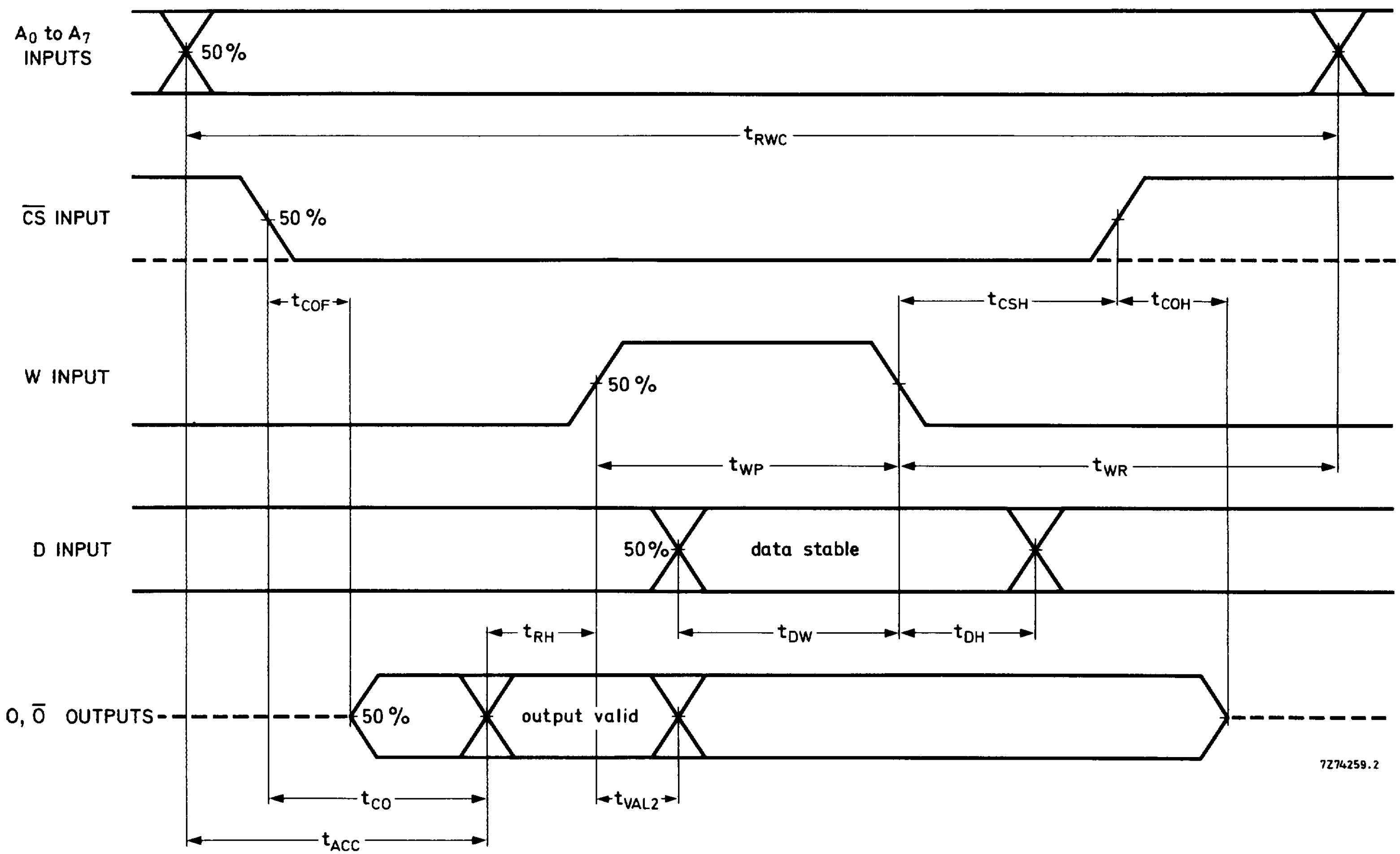


Fig.5 Read-modify-write cycle timing diagram.

APPLICATION INFORMATION

Extension of memory capacity

The memory capacity of the HEF4720B; V is 256 bits (or 256 words of 1 bit). The capacity of a system can be extended in various ways by the connection of further HEF4720B; V ICs.

Extending the word length

By connecting a number of HEF4720B; V ICs as shown in Fig.6, the word length (i.e. bits per word) is multiplied by that number. That is, each device stores 1 bit per word but the total number of words remains 256. For example, if four devices are used in this way, 256 four-binary-bit words can be stored.

Extending the number of words

If a number of HEF4720B; V ICs are connected as shown in Fig.7, the words available are multiplied by that number, but the word length remains 1 bit. Notice that in this case additional addresses are used in conjunction with the $\overline{CS}$ input. In the case shown in Fig.7 (4 × HEF4720B; V in parallel), the addresses and data inputs are loaded with four inputs (= 20 pF), the $\overline{CS}$ inputs are loaded with one input each.

Extending both the word length and number of words

Figure 8 shows how a combination of the extensions described above can be used to obtain both greater word length and additional words. It is clear that the capacitive load of the driving circuits puts a limit to the free choice of the interface. In Fig.8, each address is loaded with 16 inputs, i.e. 16 × 5 = 80 pF: each CS inverter is loaded with 8 inputs, i.e. 8 × 5 = 40 pF. The data inverters in this case are loaded with only two inputs each.

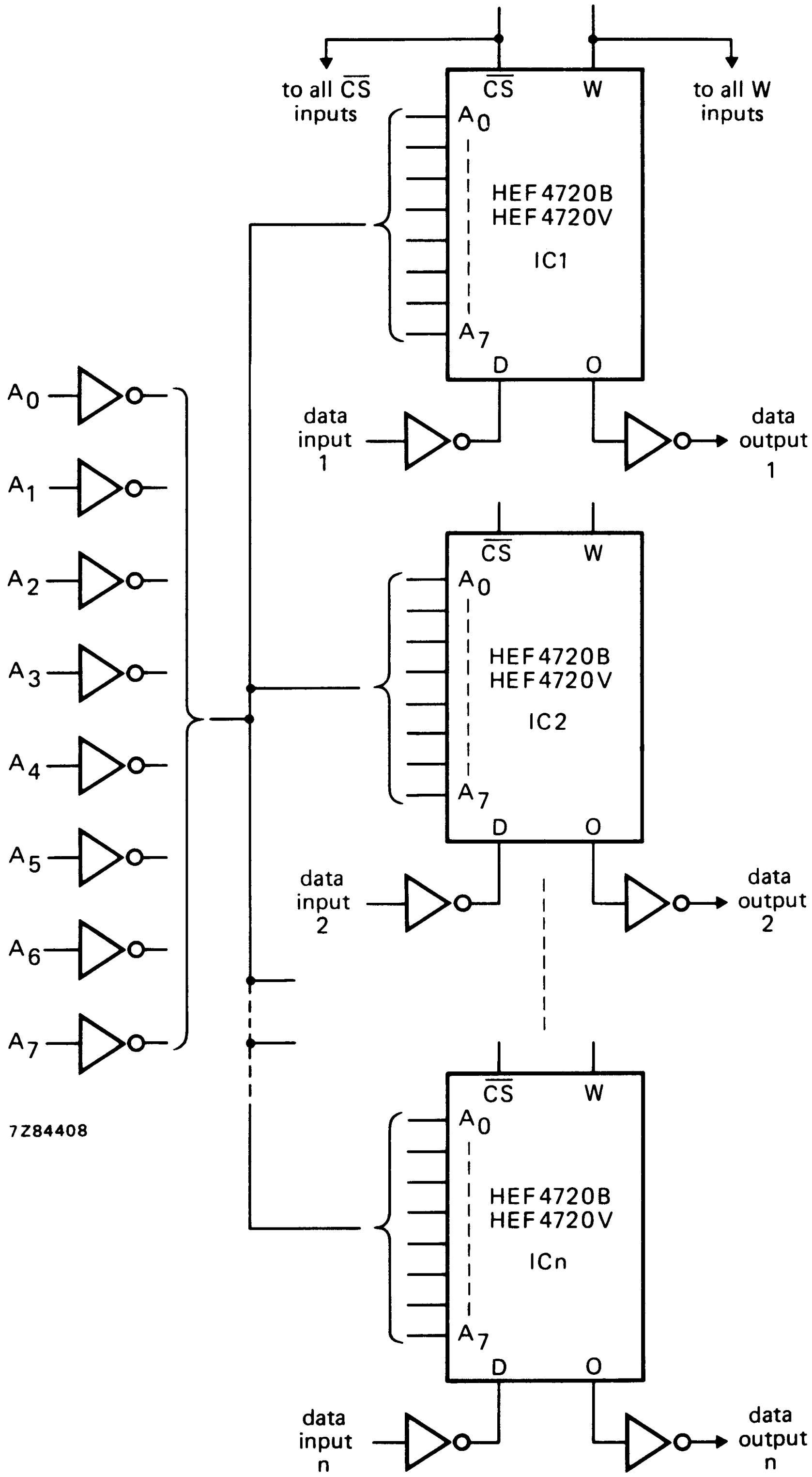


Fig.6 Using extra HEF4720B; V ICs to extend the word length.

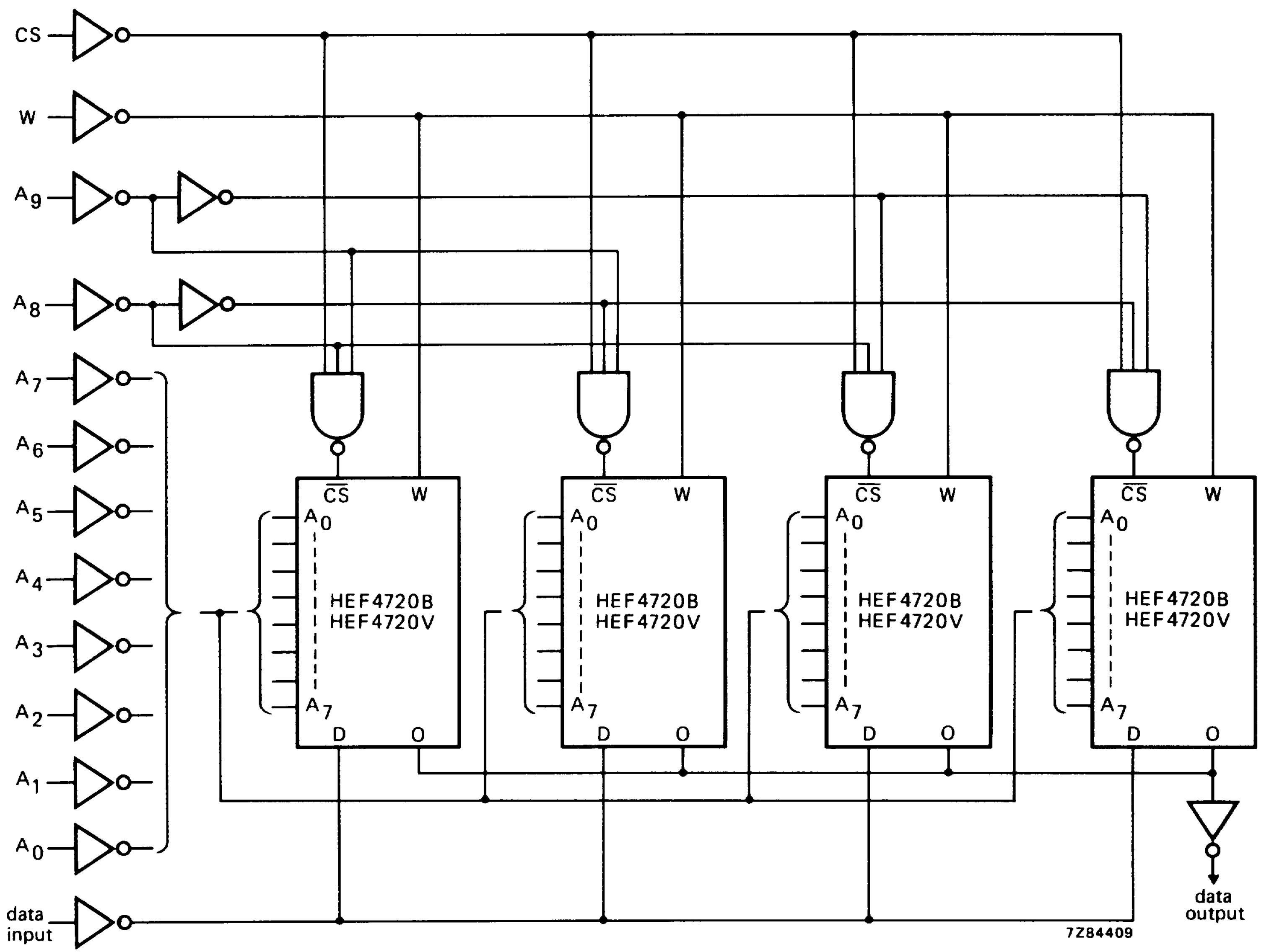


Fig.7 Using extra HEF4720B; V ICs to obtain more words.

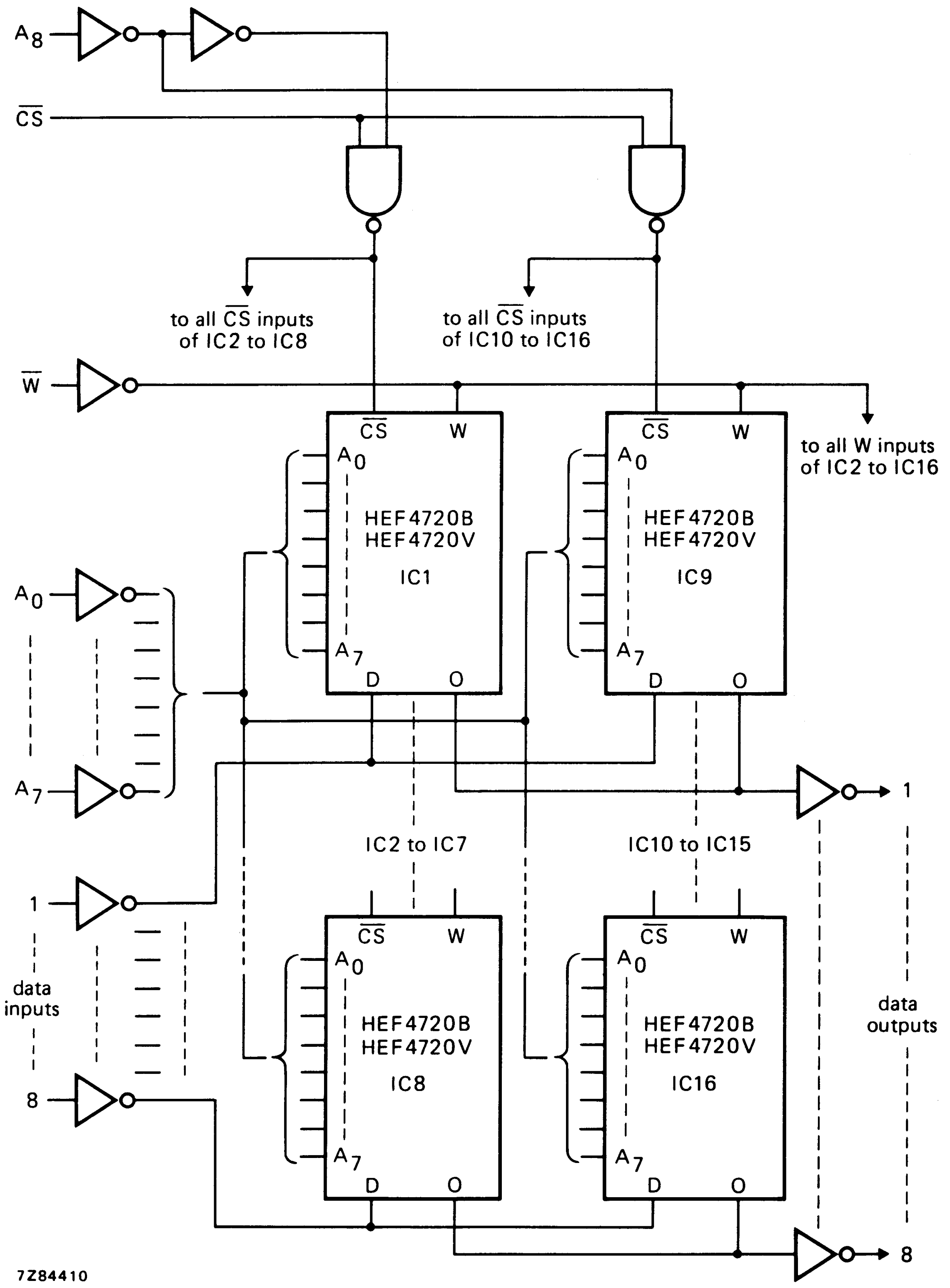


Fig.8 Using extra HEF4720B; V ICs to obtain more words and greater word length.

Memory retention

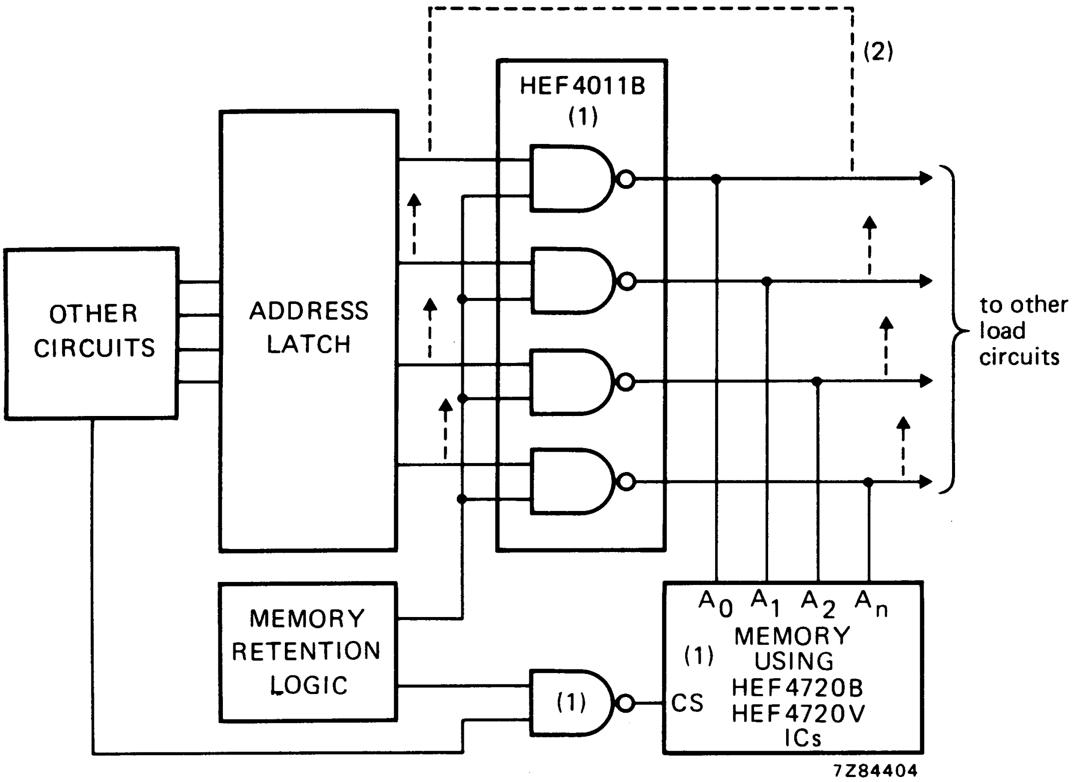
It is sometimes necessary to ensure that the information stored in the memory cannot be erased inadvertently. This can be arranged by adding detection circuits, by measures in the timing, and by the addition of a battery. With the HEF4720B; V, memory retention is very easily obtained because its current drain in the stand-by condition is almost zero. The wide supply voltage range makes it possible to keep the memory active by means of a simple battery, thereby preventing information loss.

In designing the memory retention circuits, two aspects should be kept in mind. The memory retention will not function in an optimum way if the battery voltage is low or if the voltage transitions at the address input are too slow. The first of these is usually the result of using too simple a battery back-up circuit, e.g. a battery charged via a diode from the TTL supply voltage. In this case, the LOCMOS supply voltage falls below the safe operating voltage. Special arrangements should be made to overcome this.

Slow address transitions (the second cause of memory loss) are due to a long RC-time in the power system. When the power is switched on or off, the 5 V line changes between 0 and 5 V in milliseconds to seconds so producing a correspondingly long transition time in the various logic outputs. This creates problems in the proper operation of the HEF4720B; V, with loss of memory as a possible result. This can be prevented by ensuring that input rise and fall times do not exceed 10 μs.

Three possibilities for controlling the rise and fall times at the HEF4720B; V interface are given here:

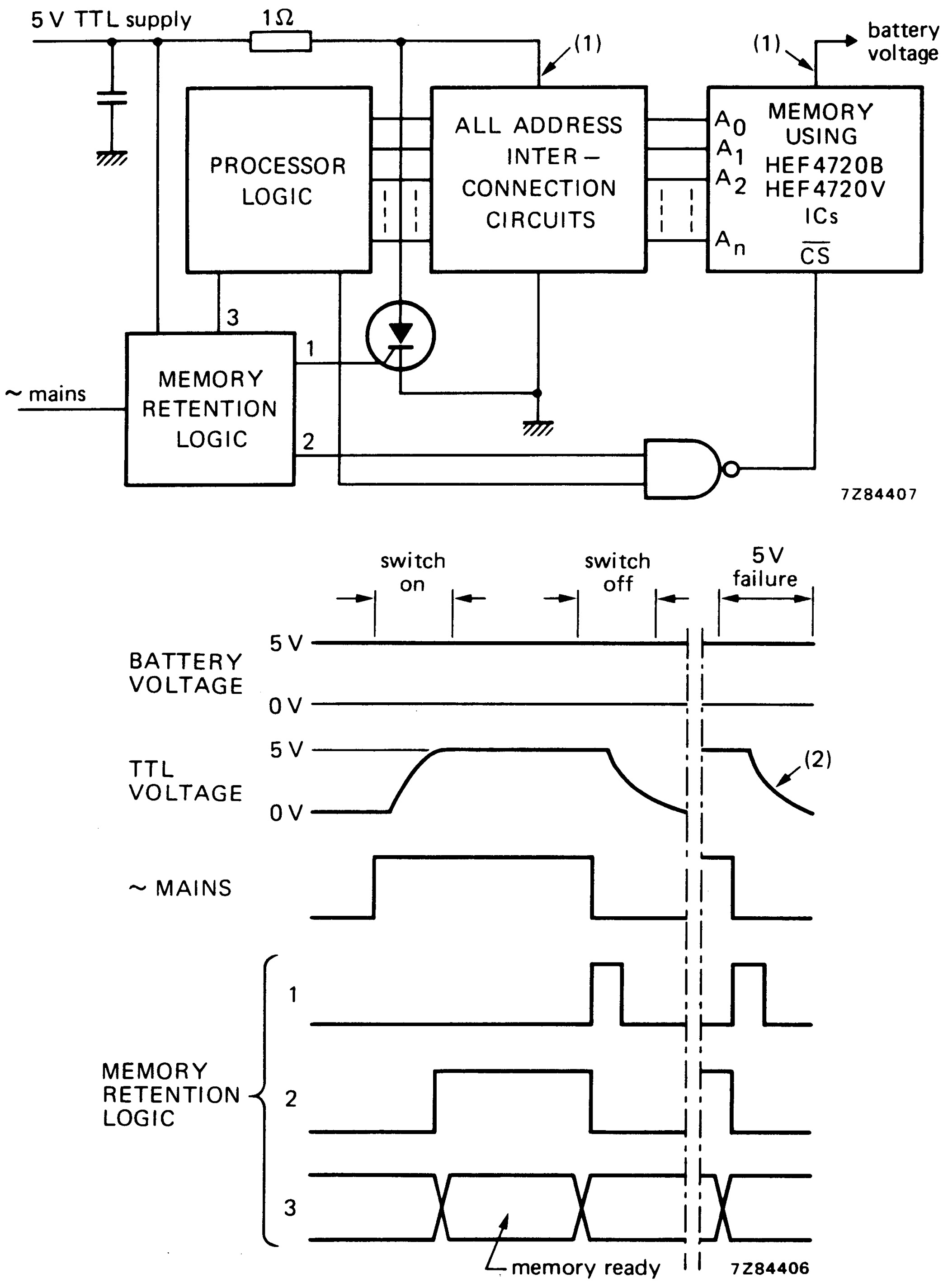
1. LOCMOS gates can be connected between the address latch and the HEF4720B; V (Fig.9). In the event of a low voltage, or mains supply failure, the gates can be blocked by a signal from the memory retention logic thus isolating the HEF4720B; V from the address and $\overline{CS}$ inputs.
2. The interface power supply can be separated from the TTL power supply by means of a low-value resistor (Fig.10); a thyristor is connected from the interface power supply to earth. The system is arranged so that, upon switching off or failure of the interface supply, the thyristor turns on thus ensuring a rapid fall of the supply voltage.
3. The best solution is to select the interface circuits from the LOCMOS family and to feed all these circuits from the battery (Fig.11). These stages then remain active when the TTL 5 V supply fails. The interface circuits are mostly only active on a clock pulse, have the possibility of being inactive on a gate level, or can be forced into one position.



(1) These devices have a battery supply.

(2) Alternative connection.

Fig.9 Use of battery-operated LOCMOS gates to isolate the memory in case of power supply failure. Devices marked (1) are connected to the battery. The HEF4011B can sink about 0,7 mA: if the load is greater than this, only the memory should be connected, other loads being connected to the address latch as shown by the dashed-line connections.



(1) Leads should be so arranged to prevent cross-talk; thyristor connections must be short.

(2) Slope > 500 mV/μs in the vicinity of the threshold.

Fig.10 Using a thyristor to ensure a rapid fall of interface supply at switch-off or supply failure.

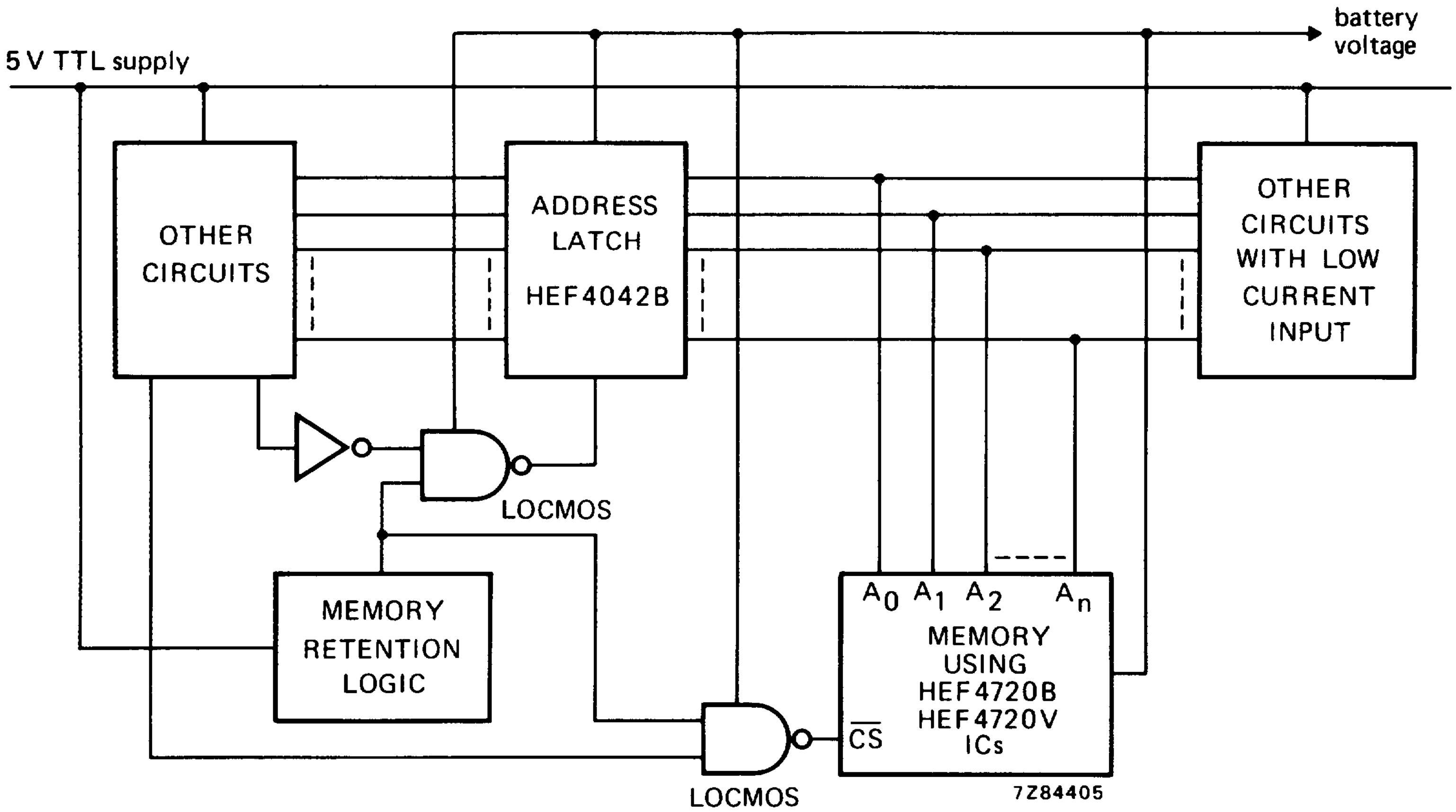


Fig.11 Preferred solution for memory retention; all interface circuits are battery-fed LOCMOS. Note that maximum sink current of the HEF4042B is about 1,5 mA.