

GaAs MMIC SUB-HARMONICALLY PUMPED IRM MIXER, 26 - 33 GHz

Typical Applications

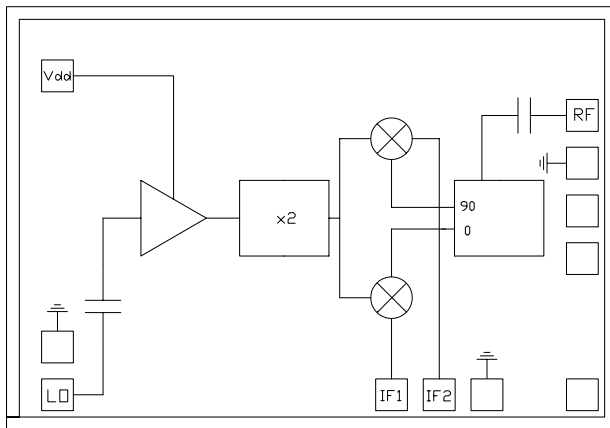
The HMC404 is ideal for:

- 26 to 33 GHz Microwave Radios
- Up and Down Converter for Point to Point Radios
- Satellite Communication Systems

Features

- Integrated LO Amplifier: +2 dBm Input
- Sub-Harmonically Pumped (x2) LO
- Image Rejection: 22 dB
- Small Size: 1.24mm x 1.86mm

Functional Diagram



General Description

The HMC404 chip is a sub-harmonically pumped (x2) MMIC image rejection mixer with an integrated LO amplifier which can be used as an upconverter or downconverter. The chip utilizes a GaAs PHEMT technology that results in a small overall chip area of 2.31mm². The on-chip 90° hybrid provides excellent amplitude and phase balance resulting in greater than 22 dB of image rejection. The LO amplifier is a single bias (+4V) two stage design with only +2 dBm nominal drive required.

Electrical Specifications, T_A = +25° C

Parameter	IF = 1 GHz LO = +2 dBm & Vdd = +4V			Units
	Min.	Typ.	Max.	
Frequency Range, RF	26 - 33			GHz
Frequency Range, LO	13 - 16.5			GHz
Frequency Range, IF	DC - 3			GHz
Conversion Loss (As IRM)		11	15	dB
Image Rejection	15	22		dB
Noise Figure		11	15	dB
1 dB Compression (Input)	+2	+6		dBm
2LO to RF Isolation	20	35		dB
2LO to IF Isolation	20	35		dB
IP3 (Input)	8	16		dBm
Amplitude Balance		±1.5		dB
Phase Balance		±7		Deg
Supply Current (I _{dd})		28		mA

* Unless otherwise noted, all measurements performed as downconverter.

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Data Taken As IRM With 1 GHz IF Hybrid

Conversion Gain vs. Temperature
@ LO= +2 dBm, Vdd= +4V

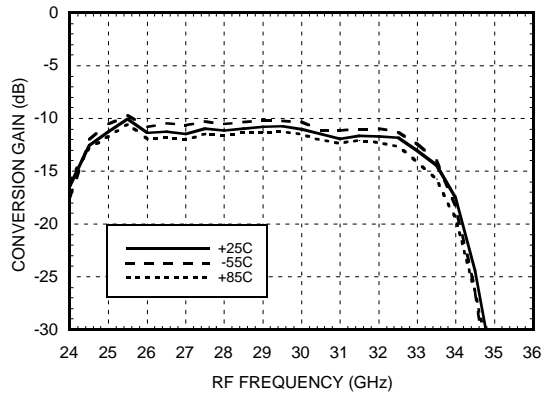
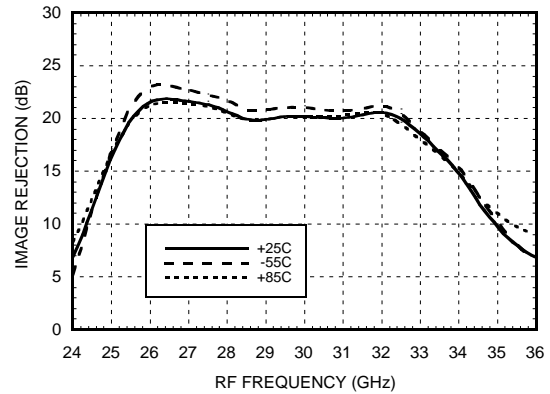
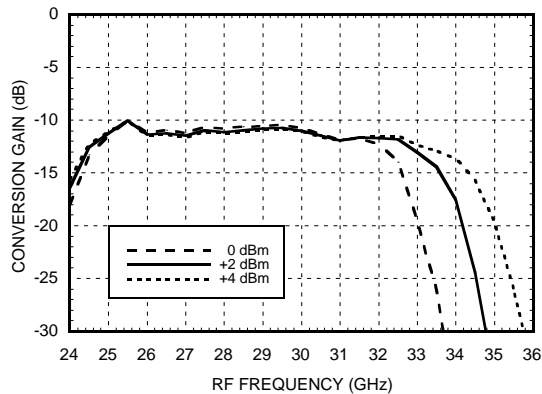


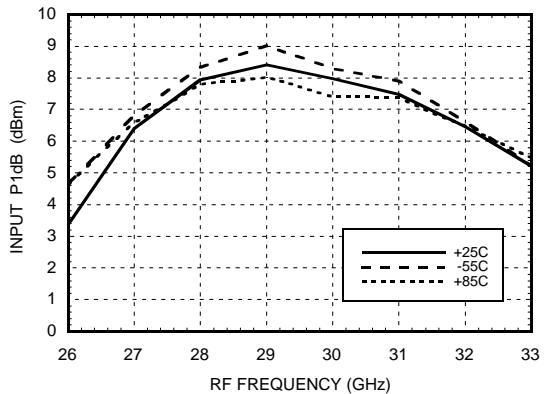
Image Rejection vs. Temperature
@ LO= +2 dBm, Vdd= +4V



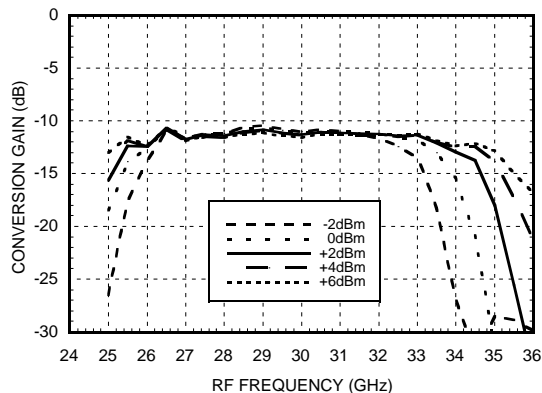
Conversion Gain vs. LO Drive
@ Vdd= +4V



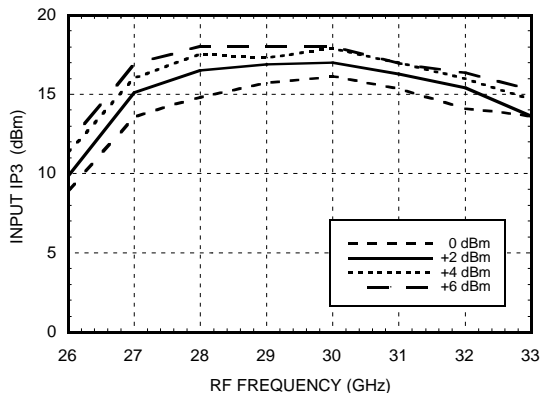
Input P1dB vs. Temperature
@ LO= +2 dBm, Vdd= +4V



Upconverter Performance Conversion Gain vs. LO Drive
@ Vdd= +4V



Input IP3 vs. LO Drive
@ Vdd= +4V*

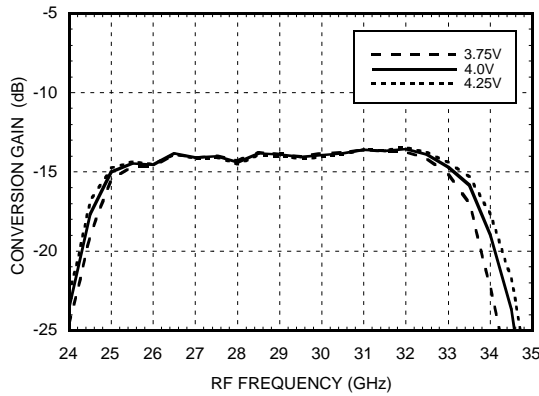


* Two-tone input power= -10 dBm each tone, 1 MHz spacing.

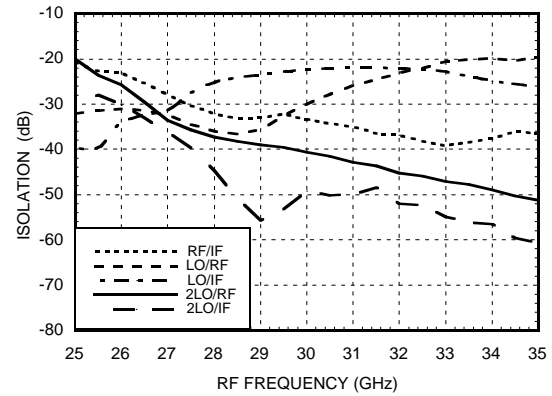
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Quadrature Channel Data Taken Without IF Hybrid

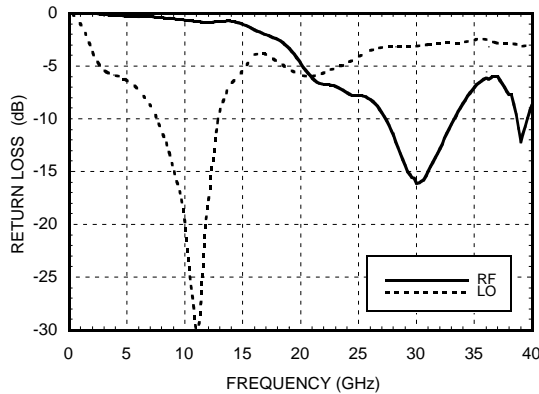
Conversion Gain vs. Vdd @ LO= +2 dBm, IF= 100 MHz



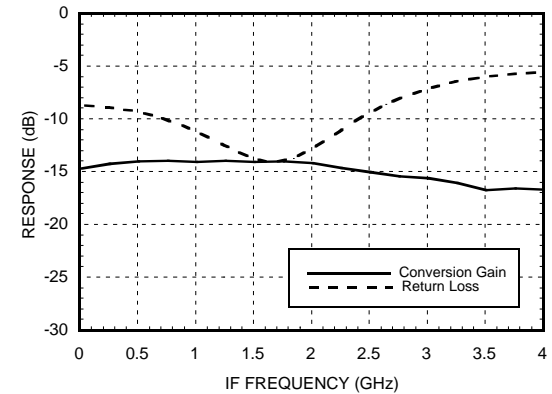
Isolation @ LO= +2 dBm, IF= 100 MHz, Vdd= +4V



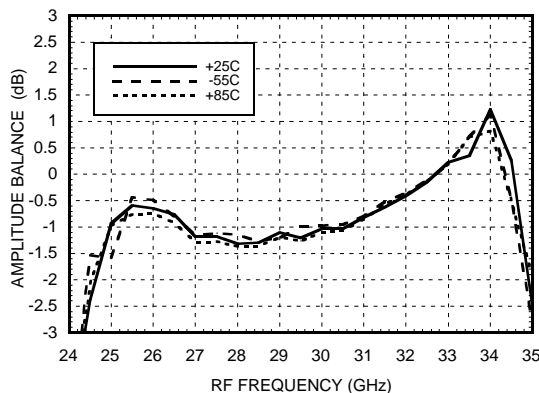
Return Loss @ LO= +2 dBm, Vdd= +4V



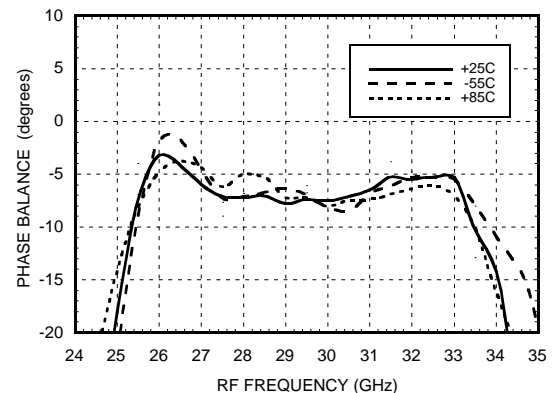
IF Bandwidth @ LO= +2 dBm, Vdd= +4V



Amplitude Balance vs. Temperature @ LO= +2 dBm, IF= 100 MHz, Vdd= +4V



Phase Balance vs. Temperature @ LO= +2 dBm, IF= 100 MHz, Vdd= +4V



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MxN Spurious @ IF Port, Vdd = +4V

mRF	nLO					
	±5	±4	±3	±2	±1	0
-3						
-2	65					
-1		28	71			
0				22	-3	
1				X	55	18
2		76	56			
3						

RF = 30.5 GHz @ -10 dBm
 LO = 15 GHz @ +2 dBm
 All values in dBc below IF power level.
 Measured as downconverter

MxN Spurious @ RF Port, Vdd = +4V

mIF	nLO					
	±5	±4	±3	±2	±1	0
-3				66		
-2				64	64	
-1				X	53	
0				17	6	
1				22	57	36
2				76	65	
3				55		

IF = 0.5 GHz @ -10 dBm
 LO = 15 GHz @ +2 dBm
 All values in dBc below RF power level.
 Measured as upconverter.

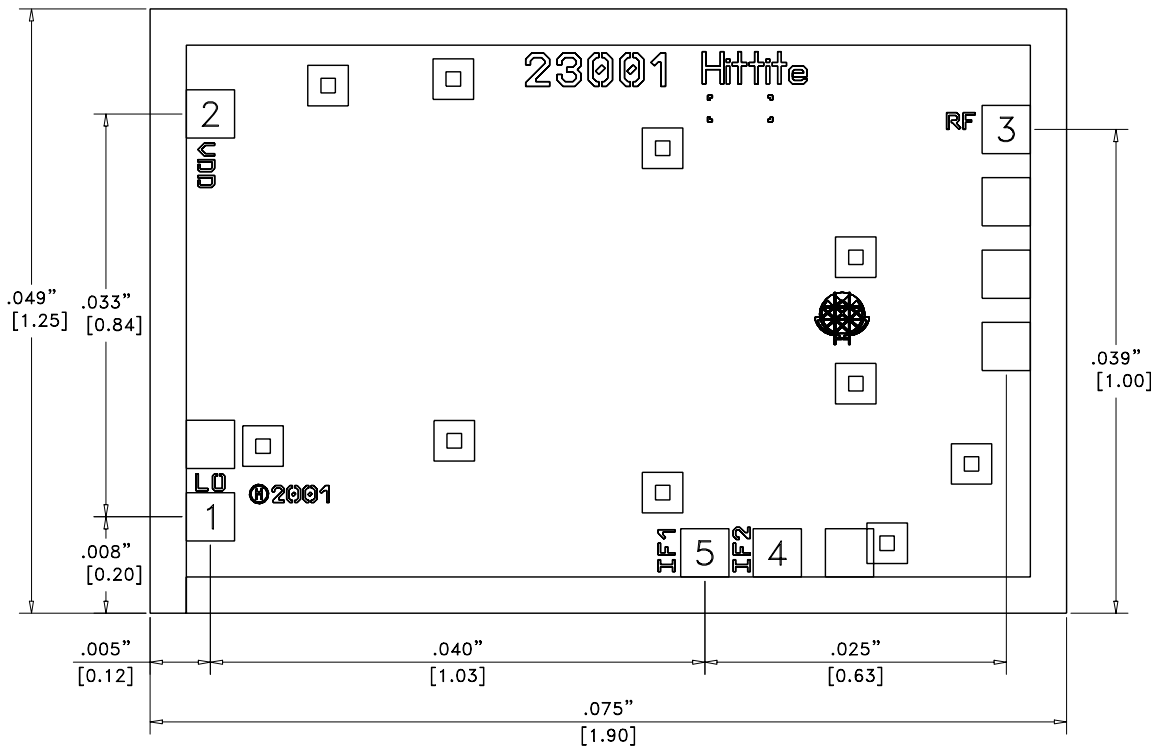
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Absolute Maximum Ratings

RF / IF Input (Vdd = +5V)	+13 dBm
LO Drive (Vdd = +5V)	+13 dBm
Vdd	5.5V
Continuous Pdiss (Ta = 85 °C) (derate 2.64 mW/°C above 85 °C)	238 mW
Storage Temperature	-65 to +150 °C
Operating Temperature	-55 to +85 °C

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Outline Drawing


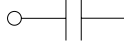
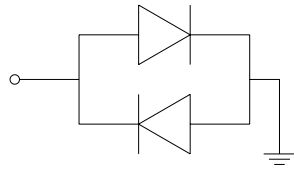
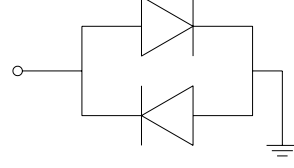


NOTES:

1. ALL DIMENSIONS IN INCHES (MILLIMETERS)
2. ALL TOLERANCES ARE ± 0.001 (0.025)
3. DIE THICKNESS IS 0.004 (0.100) BACKSIDE IS GROUND
4. BOND PADS ARE 0.004 (0.100) SQUARE
5. BOND PAD SPACING, CTR-CTR: 0.006 (0.150)
6. BACKSIDE METALLIZATION: GOLD
7. BOND PAD METALLIZATION: GOLD
8. NO CONNECTION REQUIRED TO UNLABELED BOND PADS

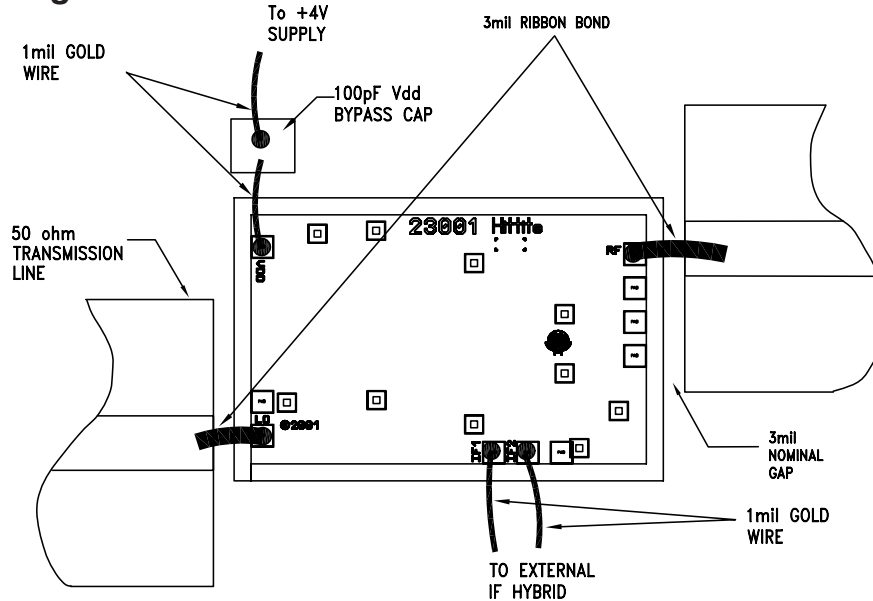
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Pad Descriptions

Pad Number	Function	Description	Interface Schematic
1	LO Port	LO Port. This pad is AC coupled and matched to 50 Ohm from 13 - 16.5 GHz	
2	Vdd	Power supply for the LO Amplifier. An external RF bypass capacitor of 100 - 330 pF is required. A MIM border capacitor is recommended. The bond length to the capacitor should be as short as possible. The ground side of the capacitor should be connected to the housing ground.	
3	RF Port	RF Port. This pad is AC coupled and matched to 50 Ohm from 26 - 33 GHz.	
4	IF2	IF Port. This pin is DC coupled. For applications not requiring operation to DC, this port should be DC blocked externally using a series capacitor whose value has been chosen to pass the necessary IF frequency range. For operation to DC, this pin must not source/sink more than 3mA of current or die non-function and possible die failure will result.	
5	IF1	IF Port. This pin is DC coupled. For applications not requiring operation to DC, this port should be DC blocked externally using a series capacitor whose value has been chosen to pass the necessary IF frequency range. For operation to DC, this pin must not source/sink more than 3mA of current or die non-function and possible die failure will result.	

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Assembly Diagrams



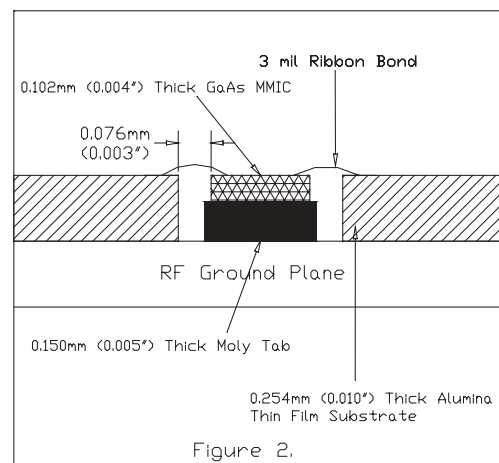
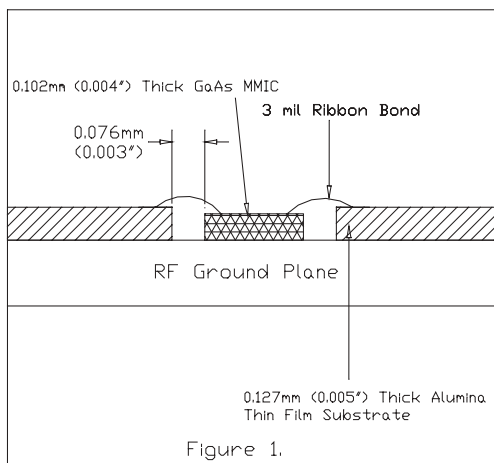
Mounting & Bonding Techniques for Millimeterwave GaAs MMICs

The die should be attached directly to the ground plane eutectically or with conductive epoxy (see HMC general Handling, Mounting, Bonding Note).

50 Ohm Microstrip transmission lines on 0.127mm (5 mil) thick alumina thin film substrates are recommended for bringing RF to and from the chip (Figure 1). If 0.254mm (10 mil) thick alumina thin film substrates must be used, the die should be raised 0.150mm (6 mils) so that the surface of the die is coplanar with the surface of the substrate. One way to accomplish this is to attach the 0.102mm (4 mil) thick die to a 0.150mm (6 mil) thick molybdenum heat spreader (moly-tab) which is then attached to the ground plane (Figure 2).

Microstrip substrates should be brought as close to the die as possible in order to minimize ribbon bond length. Typical die-to-substrate spacing is 0.076mm (3 mils). Gold ribbon of 0.075 mm (3 mil) width and minimal length <0.31 mm (<12 mils) is recommended to minimize inductance on RF, LO & IF ports.

An RF bypass capacitor should be used on the Vdd input. A 100 pF single layer capacitor (mounted eutectically or by conductive epoxy) placed no further than 0.762mm (30 Mils) from the chip is recommended.



**GaAs MMIC SUB-HARMONICALLY
PUMPED IRM MIXER, 26 - 33 GHz****Handling Precautions**

Follow these precautions to avoid permanent damage.

Cleanliness:

Handle the chips in a clean environment.
DO NOT attempt to clean the chip using liquid cleaning systems.

Static Sensitivity:

Follow ESD precautions to protect against $> \pm 250V$ ESD strikes.

Transients:

Suppress instrument and bias supply transients while bias is applied.
Use shielded signal and bias cables to minimize inductive pick-up.

General Handling:

Handle the chip along the edges with a vacuum collet or with a sharp pair of bent tweezers.
The surface of the chip has fragile air bridges and should not be touched with vacuum collet, tweezers, or fingers.

Mounting

The chip is back-metallized and can be die mounted with AuSn eutectic preforms or with electrically conductive epoxy. The mounting surface should be clean and flat.

Eutectic Die Attach:

A 80/20 gold tin preform is recommended with a work surface temperature of 255 °C and a tool temperature of 265 °C. When hot 90/10 nitrogen/hydrogen gas is applied, tool tip temperature should be 290 °C. DO NOT expose the chip to a temperature greater than 320 °C for more than 20 seconds. No more than 3 seconds of scrubbing should be required for attachment.

Epoxy Die Attach:

Apply a minimum amount of epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip once it is placed into position.
Cure epoxy per the manufacturer's schedule.

Wire Bonding

Ball or wedge bond with 0.025 mm (1 mil) diameter pure gold wire (DC bias, IF1 and IF2) or Ribbon Bond (RF and LO ports) 0.076 mm x 0.013 mm (3 mil x 0.5 mil) size is recommended. Thermosonic wirebonding with a nominal stage temperature of 150 °C and a ball bonding force of 40 to 50 grams or wedge bonding force of 18 to 22 grams is recommended. Use the minimum level of ultrasonic energy to achieve reliable wirebonds.

Wirebonds should be started on the chip and terminated on the package or substrate. All bonds should be as short as possible <0.31 mm (12 mils).