Ordering number : EN5974

Monolithic Digital IC

LB1980H

Three-Phase Brushless Motor Driver for VCR Capstan Motors

Overview

The LB1980H is a 3-phase brushless motor driver that is particularly appropriate for VCR capstan motor drivers.

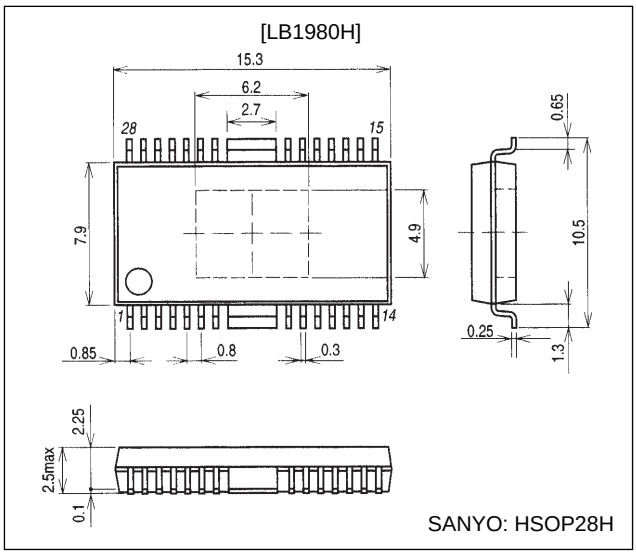
Functions

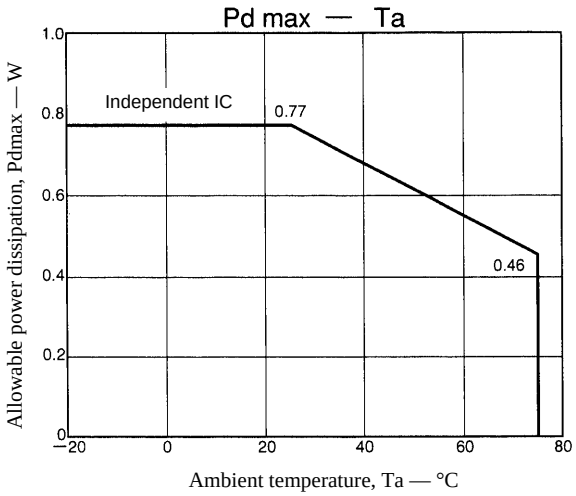
- 3-phase full-wave drive
- Built-in torque ripple correction circuit (variable correction ratio)
- Current limiter circuit
- Upper and lower side output stage over-saturation prevention circuit that does not require external capacitors.
- FG amplifier
- Thermal shutdown circuit

Package Dimensions

unit: mm

3233-HSOP28H





SANYO Electric Co.,Ltd. Semiconductor Bussiness Headquarters

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		7	V
	V_S max		24	V
Maximum output current	I_O max		1.3	A
Allowable power dissipation	Pd max	Mounted on a 71.6 × 114.3 × 1.6 mm glass Epoxy printed circuit board	1.81	W
		Independent device	0.77	W
Operating temperature	Topr		–20 to + 75	°C
Storage temperature	Tstg		–55 to + 150	°C

Allowable Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_S		5 to 22	V
	V_{CC}		4.5 to 5.5	V
Hall input amplitude	V_{HALL}	Between the Hall inputs	±30 to ±80	mVo-p
GSENSE pin input range	V_{GSENSE}	With respect to the control system ground	–0.20 to + 0.20	V

Electrical Characteristics at Ta = 25°C, V_{CC} = 5 V, V_S = 15 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
V_{CC} supply current	I_{CC}	RL = ∞, V_{CTL} = 0 V, V_{LIM} = 0 V (Quiescent)		12	18	mA
[Outputs]						
Output saturation voltage	$V_O$sat1	I_O = 500 mA, Rf = 0.5 Ω, Sink + Source V_{CTL} = V_{LIM} = 5 V (With saturation prevention)		2.1	2.6	V
	$V_O$sat2	I_O = 1.0 A, Rf = 0.5 Ω, Sink + Source V_{CTL} = V_{LIM} = 5 V (With saturation prevention)		2.6	3.5	V
Output leakage current	$I_O$leak				1.0	mA
[FR]						
FR pin input threshold voltage	V_{FSR}		2.25	2.50	2.75	V
FR pin input bias current	I_B (FSR)		–5.0			µA
[Control]						
CTLREF pin voltage	V_{CREF}		2.05	2.15	2.25	V
CTLREF pin input range	V_{CREFIN}		1.50		3.50	V
CTL pin input bias current	I_B (CTL)	With V_{CTL} = 5 V and the CTLREF pin open			4.0	µA
CTL pin control start voltage	V_{CTL} (ST)	With Rf = 0.5 Ω, V_{LIM} = 5 V, I_O ≥ 10 mA, Hall input logic fixed (U, V, W = H, H, L)	2.00	2.15	2.30	V
CTL pin control Gm	Gm (CTL)	With Rf = 0.5 Ω, ΔI$_O$ = 200 mA, Hall input logic fixed (U, V, W = H, H, L)	0.46	0.58	0.70	A/V
[Current Limiter]						
LIM current limit offset voltage	Voff (LIM)	With Rf = 0.5 Ω, V_{CTL} = 5 V, I_O ≥ 10 mA, Hall input logic fixed (U, V, W = H, H, L)	140	200	260	mV
LIM pin input bias current	I_B (LIM)	With V_{CTL} = 5 V and the V_{CREF} pin open	–2.5			µA
LIM pin current control level	I_{LIM}	With Rf = 0.5 Ω, V_{CTL} = 5 V, V_{LIM} = 2.06 V, Hall input logic fixed (U, V, W = H, H, L)	830	900	970	mA
[Hall Amplifier]						
Hall amplifier input offset voltage	Voff (HALL)		–6		+6	mV
Hall amplifier input bias current	I_B (HALL)			1.0	3.0	µA
Hall amplifier common-mode input voltage range	V_{CM} (HALL)		1.3		3.3	V
[TRC]						
Torque ripple correction ratio	TRC	For the high and low peaks in the Rf waveform when I_O = 200 mA. (Rf = 0.5 Ω, with the ADJ pin open)*1		9		%
ADJ pin voltage	V_{ADJ}		2.37	2.50	2.63	V
[FG Amplifier]						
FG amplifier input offset voltage	Voff (FG)		–8		+8	mV
FG amplifier input bias current	I_B (FG)		–100			nA
FG amplifier output saturation voltage	$V_O$sat (FG)	Sink side, for the load provided by the internal pull-up resistor			0.5	V
FG amplifier voltage gain	V_G (FG)	For the open loop state with f = 10 kHz	41.5	44.5	47.5	dB
FG amplifier common-mode input voltage	V_{GM} (FG)		0.5		4.0	V

Notes : 1. The torque ripple correction ratio is determined as follows from the Rf voltage waveform.
2. Parameters that are indicated as design target values in the conditions column are not tested.

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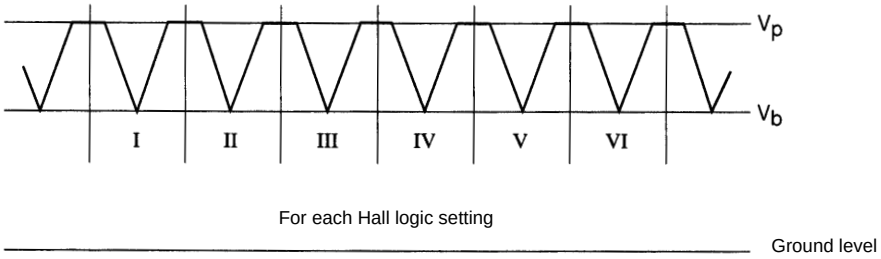
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[Saturation]						
Saturation prevention circuit lower side voltage setting	$V_O$sat (DET)	The voltages between each OUT and Rf pair when I_O = 10 mA, Rf = 0.5 Ω, and $V_{CTL} = V_{LIM}$ = 5 V	0.175	0.25	0.325	V
[TSD]						
TSD operating temperature	TSD	Design target value*2		180		°C
Hysteresis width	ΔTSD	Design target value*2		20		°C

Notes : 1. The torque ripple correction ratio is determined as follows from the Rf voltage waveform.
2. Parameters that are indicated as design target values in the conditions column are not tested.



$$\text{Correction ratio} = \frac{2 \times (V_p - V_b)}{V_p - V_b} 100 \times (\%)$$

Truth Table and Control Functions

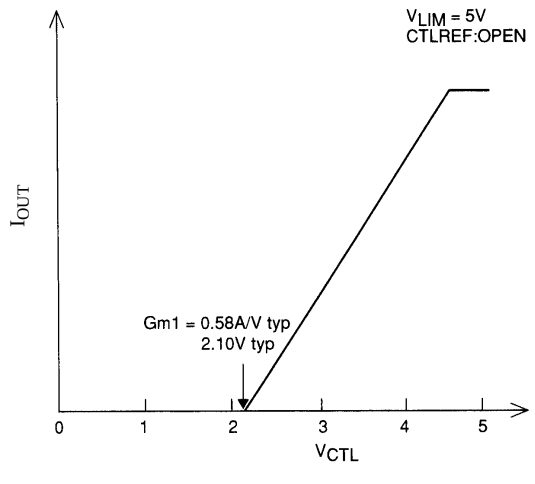
	Source → Sink	Hall input			FR
		U	V	W	
1	Phase V → Phase W	H	H	L	H
	Phase W → Phase V				L
2	Phase U → Phase W	H	L	L	H
	Phase W → Phase U				L
3	Phase U → Phase V	H	L	H	H
	Phase V → Phase U				L
4	Phase W → Phase V	L	L	H	H
	Phase V → Phase W				L
5	Phase W → Phase U	L	H	H	H
	Phase U → Phase W				L
6	Phase V → Phase U	L	H	L	H
	Phase U → Phase V				L

Note: Since the drive technique adopted is a 180° technique, phases other than the sink and source phase do not turn off.

Note: In the FR column, “H” refers to a voltage of 2.75 V or higher, and “L” refers to 2.25 V or lower (when V_{CC} = 5 V.)

Note: In the Hall input column, “H” refers to the state in the corresponding phase where the + input is at a potential at least 0.01 V higher than the – input, and “L” refers to the state where the – input is at a potential at least 0.01 V higher than the + input.

Control Function and Current Limiter Function



Control Characteristics

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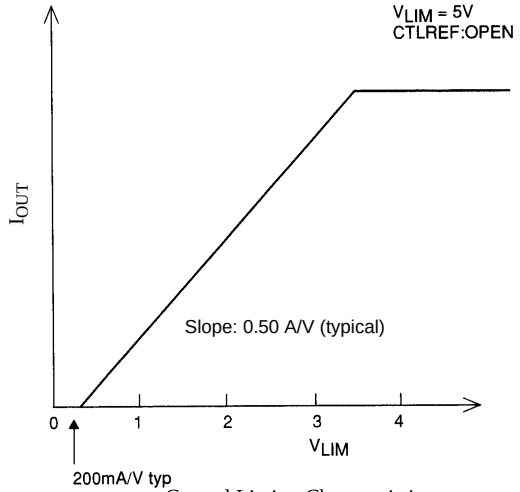

Control Limiter Characteristics

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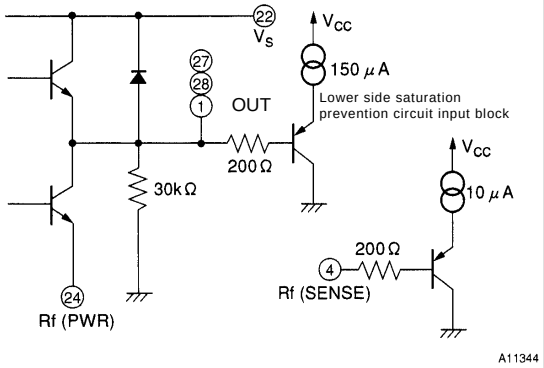
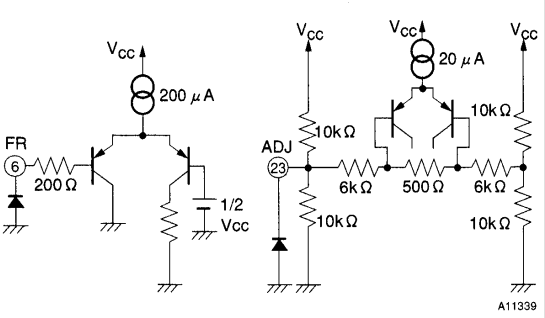
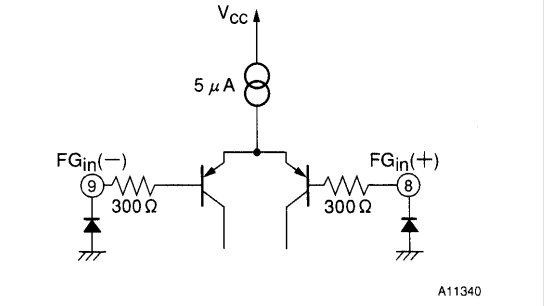
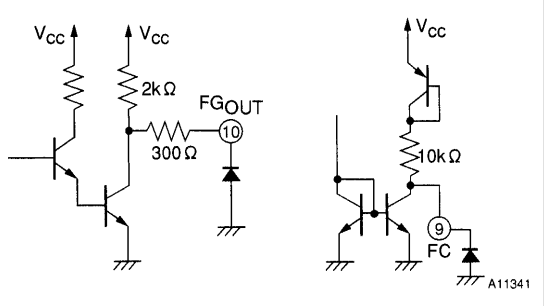
Pin Descriptions

Pin No.	Pin	Function	Equivalent circuit
27 28 1	U_{OUT} V_{OUT} W_{OUT}	U phase output V phase output W phase output (Spark killer diodes are built-in.)	
4 24	Rf (SENSE) Rf (PWR)	Output current detection. The control block current limiter operates using the resistor Rf connected between these pins and ground. Also, the lower side saturation prevention circuit and the torque ripple correction circuit operate based on the voltages across this resistor. It is especially important to note that, since the saturation prevention level is set using this voltage, the lower side saturation prevention circuit will become less effective in the high current region if the value of Rf is lowered excessively. Also, the PWR and SENSE pins must be connected together.	
22	V_S	Output block power supply	
5	GSENSE	Ground sensing. The influence of the common ground impedance on Rf can be excluded by connecting this pin to nearest ground for the Rf resistor side of the motor ground wiring that includes Rf. (This pin must not be left open.)	
6	FR	Forward/reverse selection. The voltage applied to this pin selects the motor direction (forward or reverse). (Vth = 2.5 V at V_{CC} = 5 V (typical))	
23	ADJ	Used for external adjustment of the torque ripple correction ratio. Apply a voltage externally with a low-impedance circuit to the ADJ pin to adjust the correction ratio. The correction ratio falls as the applied voltage is increased, and increases as the applied voltage decreases. The torque ripple correction ratio can be modified by factors in the range 0 to 2 times the ratio that applies when his pin is left open. (The pin voltage is set to about V_{CC}/2 internally, and the input impedance is about 5 kΩ.)	
7	GND	Ground for all circuits other than the output transistors. The lowest potential of the output transistors is that of the Rf pin.	
8	FG_{IN}^{+}	Input used when the FG amplifier is used as an inverting input. A feedback resistor must be connected between FG_{OUT} and this pin.	
9	FG_{IN}^{-}	Noninverting input used when the FG amplifier is used as a differential input amplifier. No bias is applied internally.	
10	FG_{OUT}	FG amplifier output. There is an internal resistive load.	
14	FC	Speed control loop frequency characteristics correction.	

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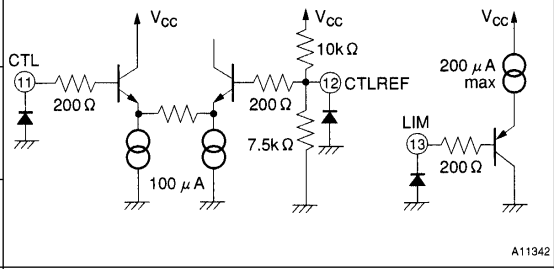
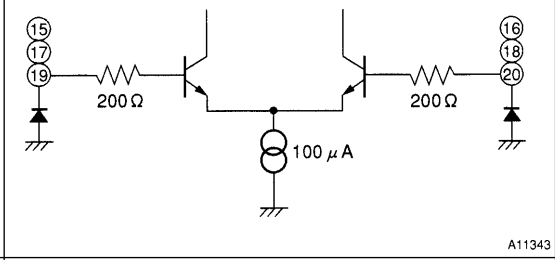
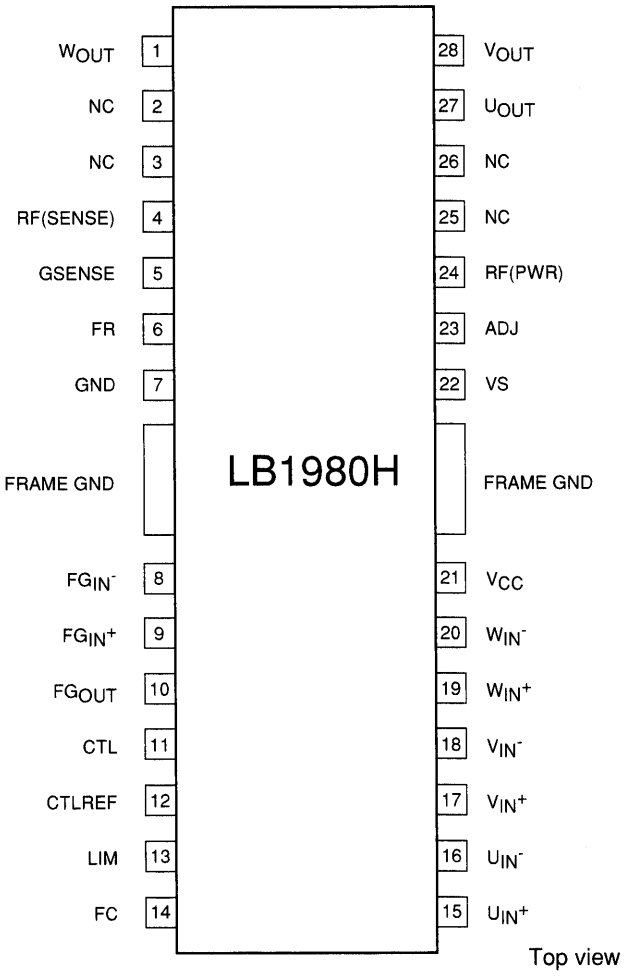
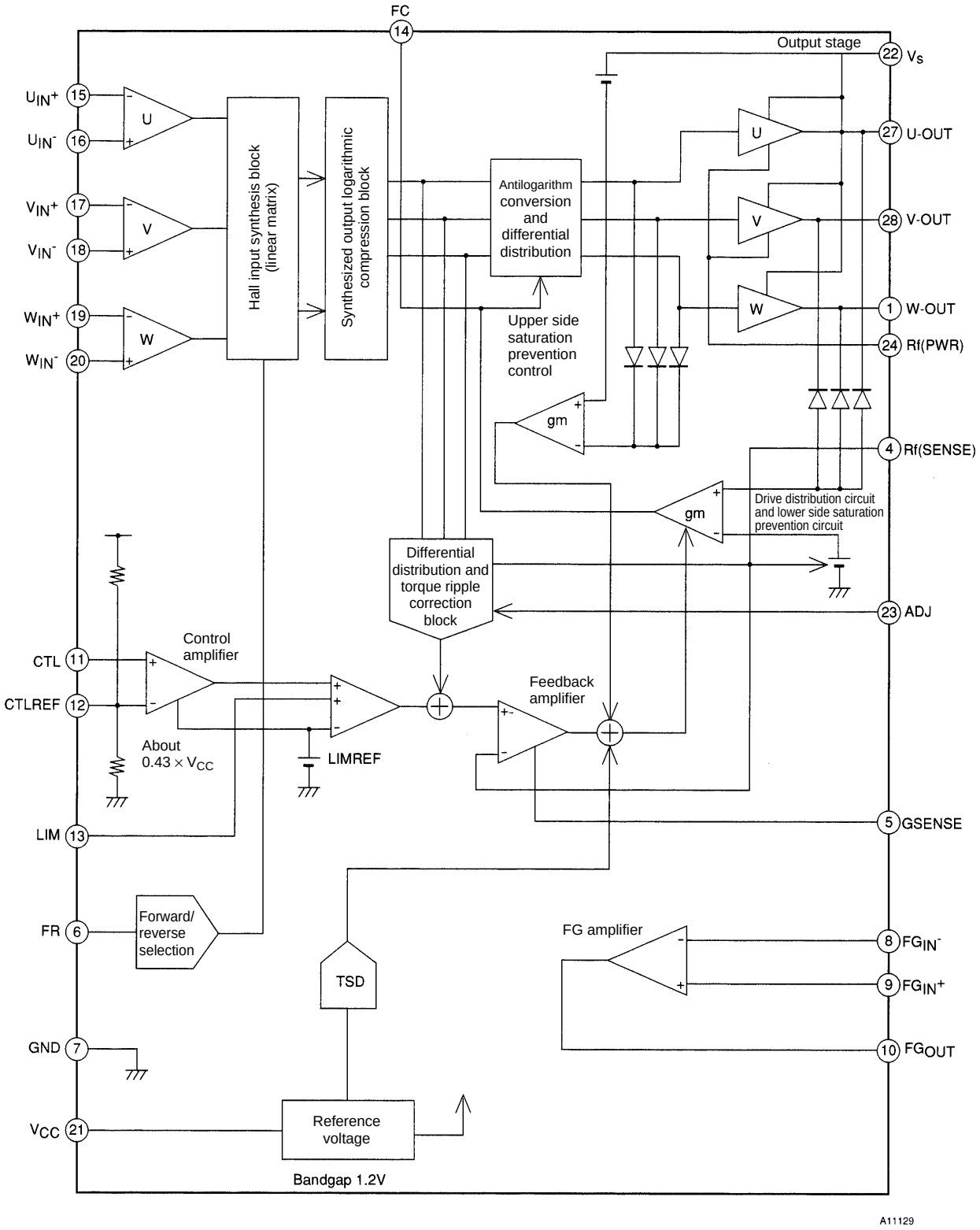
Pin No.	Pin	Function	Equivalent circuit
11	CTL	Speed control input. The control implemented is fixed current drive controlled by current feedback from Rf. Gm = 0.58/V (typical) when Rf = 0.5 Ω	
12	CTLREF	Control reference voltage. While this pin is set to about 0.43 × V_{CC} internally, this voltage can be modified by applying a voltage from a low-impedance circuit. (The input impedance is about 4.3 kΩ).	
13	LIM	Current limiter function control. The output current can be varied linearly by applying a voltage to this pin. The slope is 0.5 A/V (typical) when Rf = 0.5 Ω.	
15 16	U_{IN}^+ U_{IN}^-	U phase Hall element inputs. Logic high is defined as states where $IN^+ > IN^-$.	
17 18	V_{IN}^+ V_{IN}^-	V phase Hall element inputs. Logic high is defined as states where $IN^+ > IN^-$.	
19 20	W_{IN}^+ W_{IN}^-	W phase Hall element inputs. Logic high is defined as states where $IN^+ > IN^-$.	
21	V_{CC}	Power supply for all internal blocks other than the output block. This voltage must be stabilized so that noise and ripple do not enter the IC.	

Pin Assignment



Block Diagram



Sample Application Circuit