Complete 12-Bit A/D Converter

FEATURES

- Industry-Standard 574A Compatible
- Complete 12-Bit A/D Converter with Reference and Clock
- Improved Reference Output Current Capability
- 25µs Maximum Conversion Time
- Fast Bus Access Time
- 8- or 16-Bit Microprocessor Interface
- Guaranteed Linearity over Temperature

APPLICATIONS

- Signal Processing
- Data Acquisition
- Process Monitoring and Control

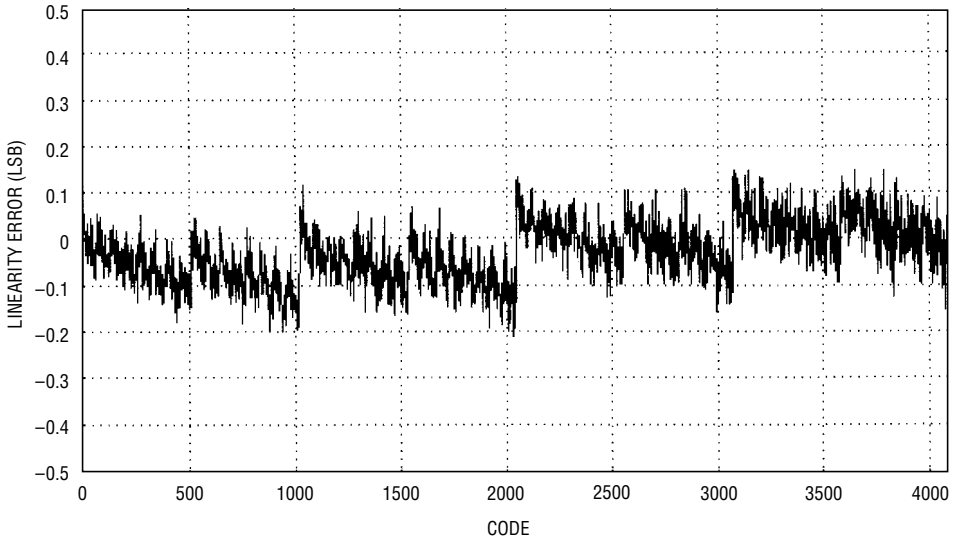
DESCRIPTION

The LT®574A is a complete 12-bit A/D converter in the industry-standard 574A pinout. The three-state output buffers interface directly to an 8- or 16-bit microprocessor bus. A high precision 10V reference and clock are included on-chip, and the device provides full-rated performance without external circuitry or clock signals.

The LT574A provides several advantages over other 574A type devices. External load driving capability of the reference has been improved to up to 8.5mA beyond the ADC current required. Maximum V_{CC} has been increased to 22V and the reference can source full load current at a V_{CC} of 11.4V without requiring an external buffer. The reference is trimmed to 10.00V with 0.2% maximum error and 5ppm/°C typical TC. Bus timing specifications are significantly faster than original 574A specifications, easing microprocessor interface concerns.

TYPICAL PERFORMANCE

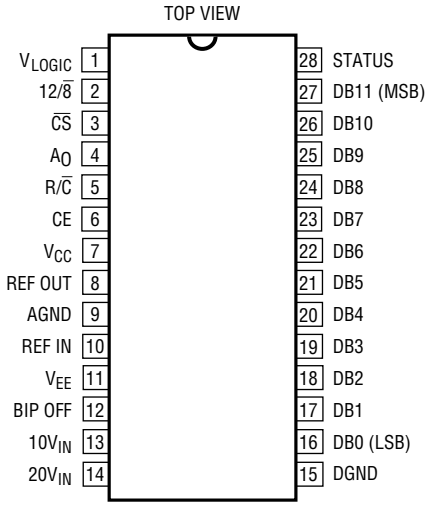
Integral Linearity



ABSOLUTE MAXIMUM RATINGS

V_{CC} to Digital Common ..... 0V to 22V
V_{EE} to Digital Common ..... 0V to –16.5V
V_{LOGIC} to Digital Common ..... 0V to 7V
Analog Common to Digital Common ..... ±1V
Digital Inputs to
  Digital Common..... –0.5V to V_{LOGIC} + 0.5V
Analog Inputs (REF In, BIP Off, $10V_{IN}$)
  to Analog Common..... V_{EE} to 16.5V
$20V_{IN}$ to Analog Common..... V_{EE} to 24V
REF Out ..... Indefinite Short to Analog Common
  Momentary Short to V_{CC}
Power Dissipation..... 1000mW
Junction Temperature..... 165°C
Operating Temperature Range
  J, K, L Grades ..... 0°C to 70°C
Storage Temperature ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION



NW PACKAGE
28-LEAD PDIP WIDE

T_{JMAX} = 100°C, θ_{JA} = 70°C/W

ORDER PART NUMBER
LT574AJNW
LT574AKNW
LT574ALNW

Consult factory for Industrial and Military grade parts.

CONVERTER ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 12V or 15V, V_{EE} = – 12V, V_{LOGIC} = 5V, unless otherwise specified.

PARAMETER		LT574AJ MIN	LT574AJ TYP	LT574AJ MAX	LT574AK MIN	LT574AK TYP	LT574AK MAX	LT574AL MIN	LT574AL TYP	LT574AL MAX	UNITS
Resolution	●			12			12			12	Bits
Integral Linearity Error	●			±1			±0.5			±0.5	LSB
Differential Linearity Error (Minimum Resolution for Which No Missing Codes are Guaranteed)	●	11			12			12			Bits
Unipolar Offset (Adjustable to Zero)				±2			±1			±1	LSB
Bipolar Offset (Adjustable to Zero)				±4			±4			±2	LSB
Full-Scale Calibration Error (With Fixed 50Ω REF Out to REF In (Adjustable to Zero)				±10			±10			±4	LSB
Temperature Coefficients											
Unipolar Offset	●			±2(10)			±1(5)			±1(5)	LSB(ppm/°C)
Bipolar Offset	●			±2(10)			±1(5)			±1(5)	LSB(ppm/°C)
Full-Scale Calibration	●			±9(50)			±5(27)			±2(10)	LSB(ppm/°C)
Supply Sensitivity (Change in Full Scale Calibration)											
13.5V ≤ V_{CC} ≤ 16.5V or 11.4V ≤ V_{CC} ≤ 12.6V	●			±2.0			±1.0			±1.0	LSB
–16.5V ≤ V_{EE} ≤ –13.5V or 12.6V ≤ V_{EE} ≤ –11.4V	●			±2.0			±1.0			±1.0	LSB
4.5V ≤ V_{LOGIC} ≤ 5.5V	●			±0.5			±0.5			±0.5	LSB
Input Ranges											
Unipolar	●	0		10	0		10	0		10	V
	●	0		20	0		20	0		20	V
Bipolar	●	–5		5	–5		5	–5		5	V
	●	–10		10	–10		10	–10		10	V
Input Impedance											
10V Span	●	3	5	7	3	5	7	3	5	7	kΩ
20V Span	●	6	10	14	6	10	14	6	10	14	kΩ

INTERNAL REFERENCE ELECTRICAL CHARACTERISTICS

PARAMETER		LT574AJ MIN	LT574AJ TYP	LT574AJ MAX	LT574AK MIN	LT574AK TYP	LT574AK MAX	LT574AL MIN	LT574AL TYP	LT574AL MAX	UNITS
REF OUT Voltage (No Load)		9.98		10.02	9.98		10.02	9.99		10.01	V
Line Regulation, $11.4 \le V_{IN} \le 22V$			1	5		1	5		1	5	ppm/V
	●			10			10			10	ppm/V
Load Regulation (Sourcing Current), $0 \le I_{OUT} \le 10mA$			12	30		12	30		12	30	ppm/mA
	●			50			50			50	ppm/mA
Reference Temperature Coefficient	●			50			27			10	ppm/°C

DIGITAL AND DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS		LT574A, All Grades MIN	TYP	MAX	UNITS
	V_{LOGIC} Supply Range		●	4.5	5.0	5.5	V
	V_{EE} Supply Range		●	–11.4		–16.5	V
	V_{CC} Supply Range		●	11.4		22.0	V
	V_{LOGIC} Operating Current		●		27	40	mA
	V_{EE} Operating Current		●		–15	–25	mA
	V_{CC} Operating Current		●		1.7	3.5	mA
	Power Dissipation		●		390	700	mW
V_{IH}	Logic High Input Voltage	12/8, CE, A_0, R/C, CE	●	2.0		5.5	V
V_{IL}	Logic Low Input Voltage	12/8, CE, A_0, R/C, CE	●	–0.5		0.8	V
I_{IN}	Logic Input Current		●	–100		100	µA
C_{IN}	Digital Input Pin Capacitance				5		pF
V_{OH}	Logic Output Voltage	$I_{SOURCE} \le 600µA$		2.4			V
V_{OL}	Logic Low Output Voltage	$I_{SINK} \le 1.6mA$				0.4	V
	Leakage Current	High-Z State		–20		20	µA
C_{OUT}	Output Capacitance				5		pF

The ● denotes the specifications which apply over the full operating temperature range.

DIGITAL TIMING ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 15V, V_{EE} = –15V, V_{LOGIC} = 5V, unless otherwise specified.

	SYMBOL	PARAMETER	LT574A, All Grades MIN	TYP	MAX	UNITS
Read Timing, Full Control Mode	t_{DD}	Access Time (from CE)		75	150	ns
	t_{HD}	Data Valid After CE Low	25			ns
	t_{HL}	Output Float Delay			150	ns
	t_{SSR}	$\overline{CS}$-to-CE Setup	50			ns
	t_{SRR}	R/$\overline{C}$-to-CE Setup	0			ns
	t_{SAR}	AO-to-CE Setup	50			ns
	t_{HSR}	$\overline{CS}$ Valid After CE Low	50			ns
	t_{HRR}	R/$\overline{C}$ High After CE Low	0			ns
	t_{HAR}	A_0 Valid After CE Low	50			ns

DIGITAL TIMING ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 15V, V_{EE} = –15V, V_{LOGIC} = 5V, unless otherwise specified.

	SYMBOL	PARAMETER	LT574A, All Grades MIN	TYP	MAX	UNITS
Convert Start Timing, Full Control Mode	t_{DSC}	STS Delay from CE			200	ns
	t_{HEC}	CE Pulse Width	50			ns
	t_{SSC}	CS-to-CE Setup	50			ns
	t_{HSC}	CS Low During CE High	50			ns
	t_{SRC}	R/C-to-CE Setup	50			ns
	t_{HRC}	R/C Low During CE High	50			ns
	t_{SAC}	AO-to-CE Setup	0			ns
	t_{HAC}	AO Valid During CE High	50			ns
	t_C	Conversion Time				
		8-Bit Cycle	10		17	µs
		12-Bit Cycle	15		25	µs
Stand-Alone Mode Timing	t_{HRL}	Low R/C Pulse Width	50			ns
	t_{DS}	STS Delay From R/C			200	ns
	t_{HDR}	Data Valid After R/C Low	25			ns
	t_{HS}	STS Delay After Data Valid	25		600	ns
	t_{HRH}	High R/C Pulse Width	150			ns
	t_{DDR}	Data Access Time			150	ns

BLOCK DIAGRAM

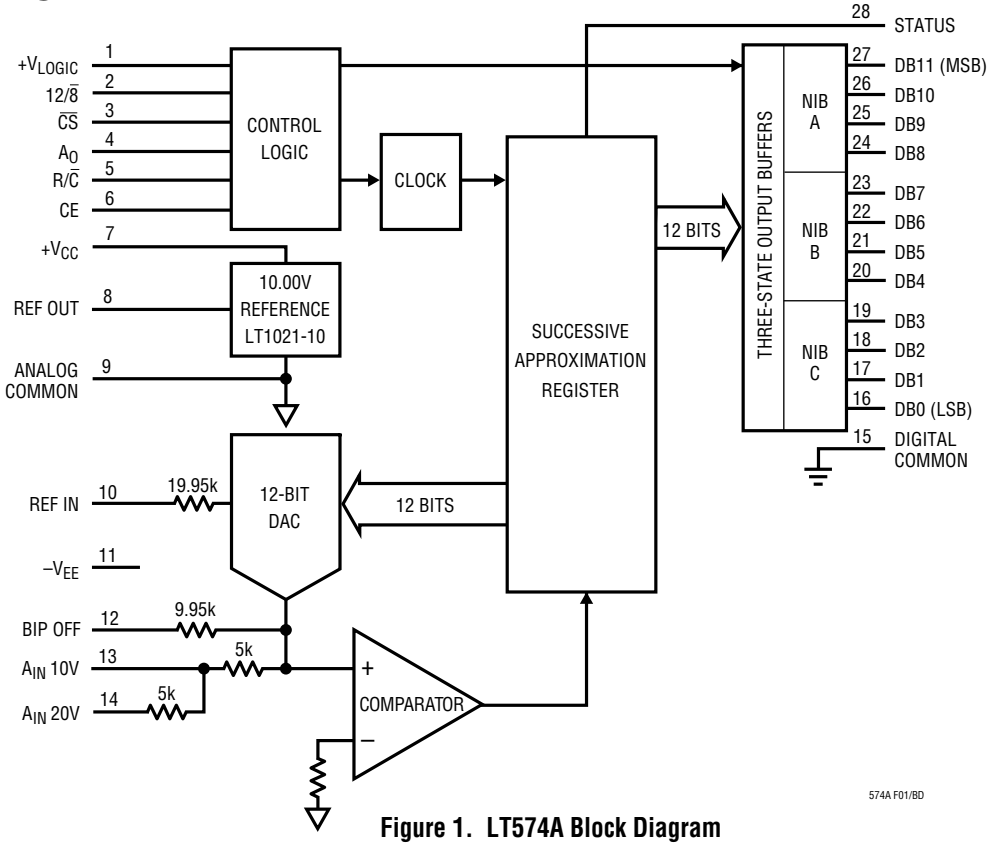


Figure 1. LT574A Block Diagram

DISCUSSION OF SPECIFICATIONS

Integral Linearity Error

Integral linearity (INL) error refers to the deviation of each code from a theoretical line drawn from "full scale." Zero is defined as the input voltage occurring 0.5LSB (1.22mV for 10V full scale) before the first code transition (0 to 1) and "full scale" is defined as the voltage occurring 1.5LSB beyond the last code transition (4094 to 4095).

Differential Linearity Error

A guaranteed "no missing codes" specification requires that every code combination appears in a monotonically increasing sequence. Thus LT574A grades which guarantee no missing codes to 12-bit resolution have a maximum DNL error of ±1LSB; grades which guarantee no missing code to an 11-bit level means that all code combinations of the upper 11 bits are present. In practice very few of the 12-bit codes are missing on the lower grade(s).

Unipolar Offset

Unipolar offset error is defined as the deviation of the first code transition from a level 0.5LSB above analog common. Unipolar offset can be adjusted as shown on the following pages. The unipolar offset temperature coefficient specifies the change of the first transition value versus a change in ambient temperature.

Bipolar Offset

The major carry transition (2047 to 2048) should occur for an analog value 0.5LSB above analog common in the bipolar mode. Bipolar offset error can also be adjusted as shown on the following pages. The bipolar offset error and temperature coefficient specify the initial deviation and maximum change in the error versus temperature.

Quantization Uncertainty

Analog-to-digital converters have inherent quantization uncertainty of ±0.5LSB. This uncertainty is a fundamental property of the conversion process and cannot be reduced for a converter of a given resolution.

Left-Justified Data

The LT574A uses a left-justified data format. The analog input is represented as a fraction of full scale, ranging from 0 to 4095/4096. A binary point to the left of the MSB is implied.

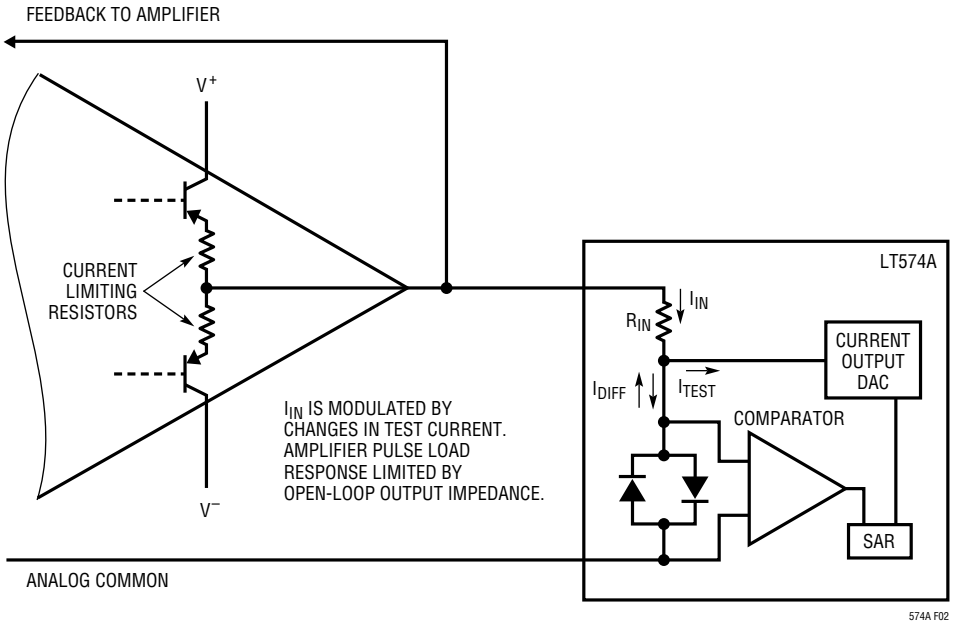


Figure 2. Op Amp/LT574A Interface

DISCUSSION OF SPECIFICATIONS

Full-Scale Calibration Error

The last output code transition (4094 to 4095) should occur for an analog value 1.5LSB below the nominal full scale (9.9963V for 10.000V full scale). The deviation of the actual level at which this transition occurs from the ideal level is the full-scale calibration error. Typically less than 0.1% of full scale, this error can be adjusted to zero as shown in Figures 3 and 4.

Temperature Coefficients

The temperature coefficients for unipolar offset, bipolar offset and full-scale calibration specify the maximum change from the nominal (25°C) value to T_{MIN} or T_{MAX}.

Power Supply Sensitivity

The LT574A is specified using 5V and ±15V or ±12V supplies. The major effect of power supply voltage deviations from the rated values will be a small change in full-scale calibration. This change results in a proportional change in all code values.

Code Width

Code width is defined as the range of analog values for which a given output code will occur. The ideal value of a code width is equivalent to 1LSB (least significant bit) of the full-scale range. In a 10V full-scale range one LSB corresponds to 2.44mV.

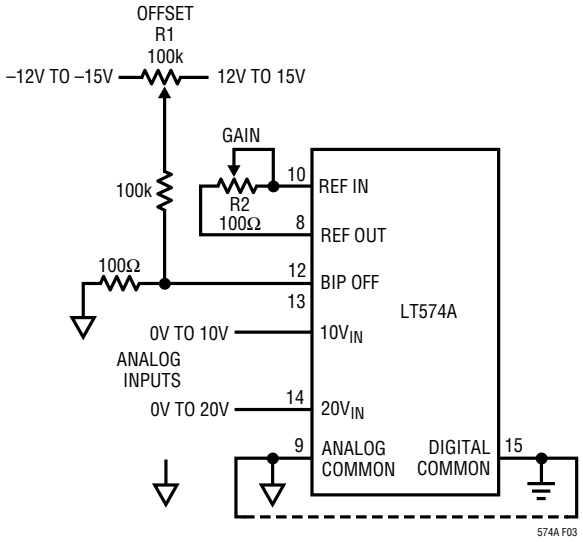


Figure 3. Unipolar Input Connections

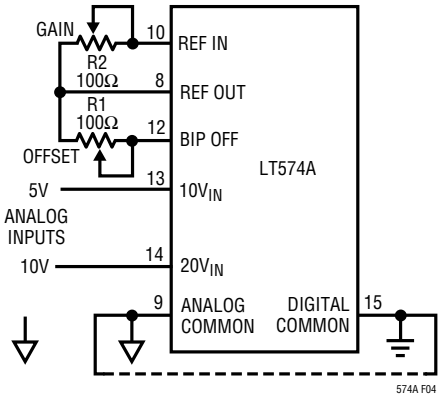


Figure 4. Bipolar Input Connections

OPERATION

Circuit Operation

The LT574A provides the complete 12-bit analog-to-digital function with no external components. A block diagram of the LT574A is shown in Figure 1. After a conversion is initiated via the control section (described later) the clock is enabled and the SAR is set to 1000 0000 0000. Once a conversion is started it cannot be stopped or restarted. The output buffers go into the Hi-Z state. The SAR, driven by the internal clock, will sequence through the conversion cycle and return a signal indicating end-of-conversion to the control section. The control section then disables the clock, bring the Status output low, and enables control functions to allow data read functions via external command.

During a conversion, the internal 12-bit current-output DAC is sequenced by the SAR starting with the most significant bit (MSB) and ending with the least significant bit (LSB). At the end of the process the DAC outputs a current which accurately balances the input signal current through the 5k (10k) input resistor. The comparator looks at the summing node at every bit test. If the DAC current sum is greater than the input current, the bit is turned off;

OPERATION

if less, the bit is left on. After all 12 bits have been tested, the SAR contains a 12-bit digital representation of the analog input signal accurate to 12 bits ±0.5LSB. Two 5k input scaling resistors allow either 10V or 20V span operation. The 10k bipolar offset resistor is connected to the 10V reference for bipolar operation, or grounded for unipolar operation.

Internal 10.00V Reference

An LT1021-10 low noise, high stability, buried-zener reference is used inside the LT574A device and guarantees superior stability over time and temperature. This reference provides improved performance over other 574-type references in both voltage range and output current sourcing capability. The reference is trimmed to 10.00V ±2%. It can supply up to 8.5mA to an external load in addition to the current required by the reference input resistor (0.5mA) and the bipolar offset resistor (1mA). This is an additional 7mA over most other 574A-type devices. (The external load should not change during a conversion.) The LT574A also has an improved V_{CC} supply range; the V_{CC} input can range from 11.2V to 22V. If operating from ±12V supplies, improved driving capability eliminates the need for an external buffer to source external loads at room temperature or over the specified temperature range.

Driving the LT574A Analog Inputs

The signal source driving the LT574A input looks into a 5k or 10k impedance. However, the current drawn out of the input pins is abruptly modulated as the ADC steps through the bit tests. Low source impedance at high frequency, necessary to hold the input voltage constant through the conversion cycle, is required for 12-bit accurate conversions. The output impedance of an op amp is equal to its open-loop output impedance divided by the loop gain available at the frequency of interest. Acceptable loop gain at 500kHz is needed for use with the LT574A. An op amp can be checked for suitability by monitoring the LT574A's input with an oscilloscope while a conversion is in progress. Each of the 12 disturbances should settle in 1µs or less. Suitable op amps include the LT1055 or LT1122.

Layout Precautions and Supply Decoupling

It is critically important the LT574A power supplies be well regulated and free of high frequency noise. Noisy supplies will cause unstable output codes. If switching power supplies must be used, considerable care must be used to ensure that switching spikes are eliminated. (For more information on constructing switching power supplies suitable for use with precision analog circuits, please see Linear Technology's Application Note 29). Just a few millivolts of high frequency noise on the power supply will result in several counts of error.

Decoupling capacitors should be used on all power supply pins. V_{LOGIC} decoupling should be connected directly from pin 1 to pin 15 (digital common) and V_{CC} and V_{EE} pins should be decoupled directly to analog common (pin 9). A 4.7µF tantalum unit in parallel with a 0.1µF ceramic type makes a suitable decoupling capacitor.

The LT574A should be located as far as possible from digital circuitry on the board layout. Coupling between analog and digital lines should be minimized. If analog and digital lines must cross, they should do so at right angles. Parallel analog and digital lines should be separated by a pattern connected to common. Wire-wrap construction is not recommended; careful printed circuit layout is preferred instead.

Grounding Considerations

The analog common (pin 9) is the internal reference ground and should be connected directly to the analog reference point of the system. It is the "high quality" ground point. Pin 9 should be connected to digital common (pin 15) at the package to achieve all the high performance accuracy available from the LT574A in noisy digital environments. This single-point grounding is the preferred method for grounding mixed analog/digital systems. Be sure there are no digital ground returns on the analog side of the line; input signal returns should be isolated from digital ground and returned directly to the single-point ground at the LT574A package.

OPERATION

Range Connections

The LT574A has four standard input ranges: 0V to 10V, 0V to 20V, –5V to 5V, and –10V to 10V. To use the 10V range, connect the input signal between pins 13 and 9. To use the 20V range, connect the input signal between pins 14 and 9. In both cases, the other pin of the two is left unconnected. Full-scale and offset adjustments are shown in Figure 3. If full-scale trim is not needed, connect a 50Ω, 1% metal film resistor between pins 8 and 10. To extend the 10V range to 10.24V (2.5mV/bit) with gain trim potentiometer (R2) should be replaced by a 50Ω resistor and a 200Ω potentiometer should be placed in series with the $10V_{IN}$ pin. To obtain a full-scale range of 20.48V (5mV/bit), a 500Ω potentiometer should be used in series with pin 14. Gain trim is now implemented with these potentiometers.

Unipolar Calibration

The first transition of the LT574A occurs at a value 0.5LSB above analog common, so that the exact analog input for a given code will be halfway between the code transitions. This 0.5LSB offset is built into the LT574A. The unit will behave in this manner, within specifications, if pin 12 is connected to analog common (pin 9). Referring to Figure 3, R1 performs the offset adjust function. It should be adjusted so that the first transition falls at exactly 0.5LSB above the analog common potential (nominally ground). The circuit, as shown, will give approximately ±15mV of offset trim range. The full-scale trim is calibrated by applying a voltage 1.5LSB below full scale (9.9963V for 10V full scale) and adjusting R2 such that the unit outputs the codes 4096 and 4097 (1111 1111 1110 and 1111 1111 1111).

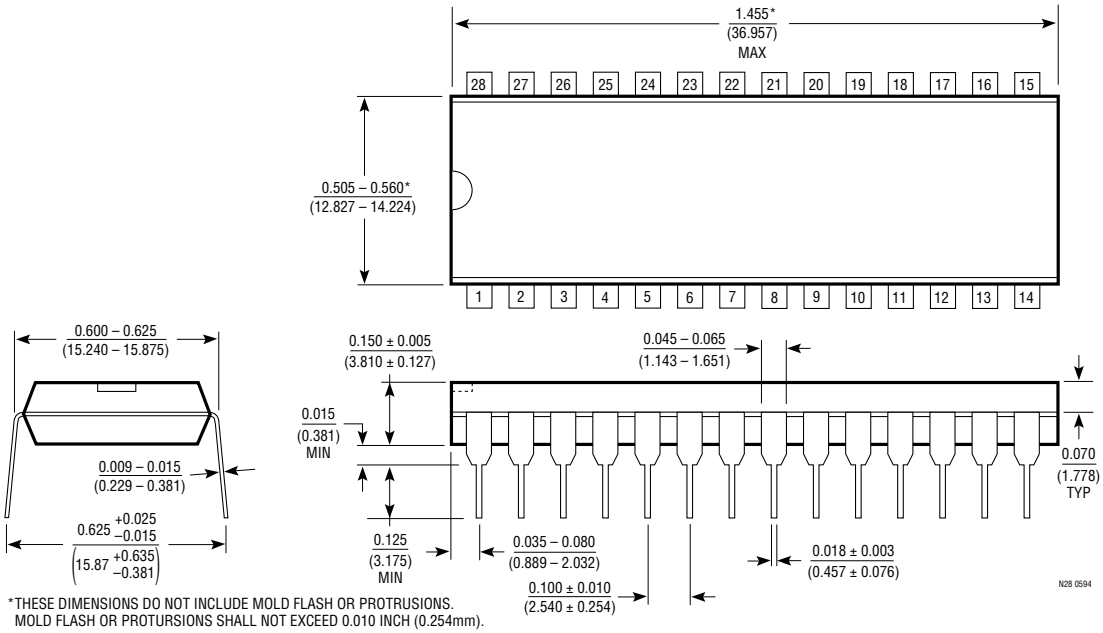
Bipolar Operation

Bipolar operation connections are shown in Figure 4. The trim potentiometers can be replaced by 50Ω, 1% resistors if offset and gain specifications are sufficient. To calibrate, apply an input signal 0.5LSB above negative full scale (0000 0000 0000 to 0000 0000 0001), then apply a signal 1.5LSB below positive full scale (4.9963V for the ±5V range) and adjust R2 so that the last transition (1111 1111 1110 to 1111 1111 1111) is output.

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

N Package
28-Lead Plastic DIP



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTURSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm).

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