T-75-11-09

FUJITSU

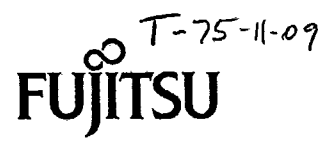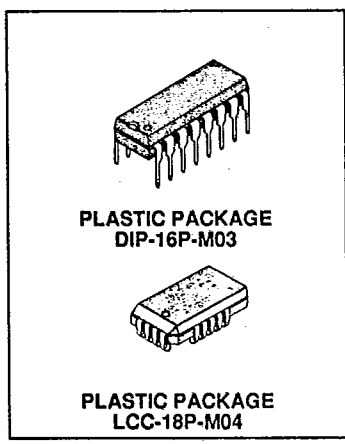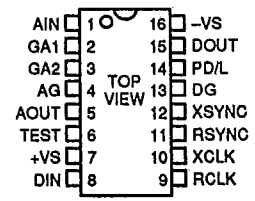=== DATA SHEET ===

MB6021A/22A/25A/26A
PCM CODEC

SINGLE CHIP CODEC WITH FILTERS

The Fujitsu CMOS MB6020A Series consists of both μ-law and A-law single-chip codec/filter IC's for either synchronous-only or sync/async operation.
These monolithic single-channel voice frequency codecs incorporate both transmit and receive circuitry that is used for PCM (pulse coded modulation) systems.
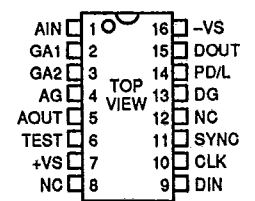
- Transmit High-pass and Low-pass Filters
- Receive Low-pass Filter with SinX/X Correction
- Anti-aliasing Filter
- Conforms to CCITT and AT&T Specifications
- Synchronous and Asynchronous Operation: MB6021A, MB6022A
- Synchronous Operation: MB6025A, MB6026A
- Serial Data Rates of 64kHz to 3.152MHz
- PLL Circuit as Internal Clock Generator
- Internal Voltage Reference
- Internal Auto-zero Circuit
- TTL Compatible Digital Interface
- Input Gain Adjust Amplifier
- Pin Selectable on-chip Analog Loopback
- μ-Law: MB6021A, MB6025A
- A-Law: MB6022A, MB6026A
- Package
  16-pin Plastic DIP Package (Suffix: –P) : MB6021A/22A/25A/26A
  18-pin Plastic LCC Package (Suffix: –PD) : MB6021A/22A

**PLASTIC PACKAGE
DIP-16P-M03**

**PLASTIC PACKAGE
LCC-18P-M04**

5

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Pin MB6021A MB6022A		Pin MB6025A MB6026A	Value		Unit
		DIP	PLCC		Min	Max	
Positive Supply Voltage	+VS	7	8	7	–0.3	–7	V
Negative Supply Voltage	–VS	16	18	16	–7	–0.3	V
Analog Input Voltage	V_{AIN}	1	1	1	–VS–0.3	+VS+0.3	V
Digital Input Voltage	V_{DIN1}	8,9,10 11,12	9,10,11 12,13	9,10,11	–0.3	+VS+0.3	V
Digital Input Voltage	V_{DIN2}	6,14	7,16	6,14	–VS–0.3	+VS+0.3	V
Storage Temperature	T_{STG}				–55	150	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN ASSIGNMENT

```
        AIN  [ 1 O    16 ]  –VS
        GA1  [ 2       15 ]  DOUT
        GA2  [ 3  TOP  14 ]  PD/L
        AG   [ 4  VIEW 13 ]  DG
       AOUT  [ 5       12 ]  XSYNC
       TEST  [ 6       11 ]  RSYNC
        +VS  [ 7       10 ]  XCLK
        DIN  [ 8        9 ]  RCLK
```
MB6021A, MB6022A

```
        AIN  [ 1 O    16 ]  –VS
        GA1  [ 2       15 ]  DOUT
        GA2  [ 3  TOP  14 ]  PD/L
        AG   [ 4  VIEW 13 ]  DG
       AOUT  [ 5       12 ]  NC
       TEST  [ 6       11 ]  SYNC
        +VS  [ 7       10 ]  CLK
        NC   [ 8        9 ]  DIN
```
MB6025A, MB6026A

PLCC Pin Assignment: Please see page 19.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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MB6021A
MB6022A
MB6025A
MB6026A

T-75-11-09
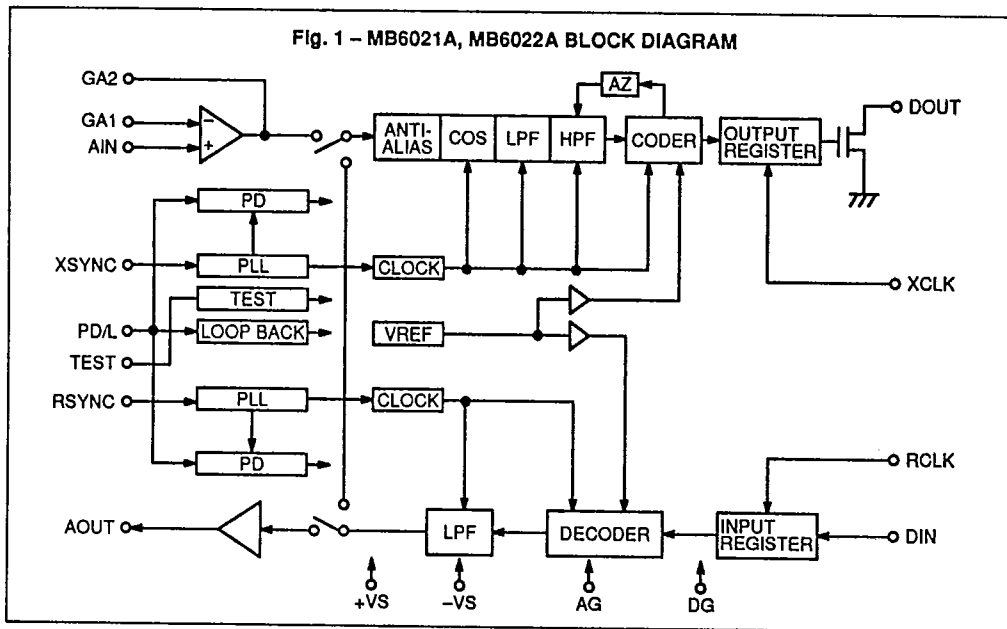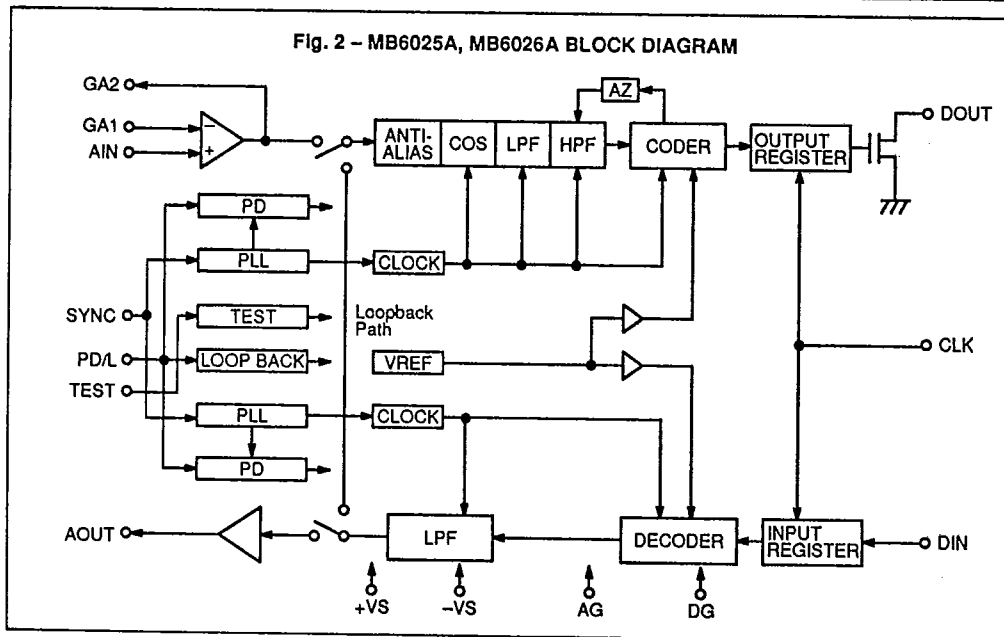
Fig. 1 – MB6021A, MB6022A BLOCK DIAGRAM

Fig. 2 – MB6025A, MB6026A BLOCK DIAGRAM

MB6021A
MB6022A
MB6025A
MB6026A

FUNCTIONAL DESCRIPTION

T-75-11-09

The simplified block diagram of the MB6021A and MB6022A is shown in Figure 1, and the block diagram for the MB6025A and MB6026A is shown in Figure 2. The transmit section (upper half) is composed of an input gain amplifier, an anti-aliasing filter (ANTI-ALIAS), a band-pass filter (COS, LPF and HPF), and a compressing coder (CODER). An auto-zero circuit (AZ) is also included in this section. The receive section (lower half) is composed of an expanding decoder (DECODER) and a low-pass filter (LPF).

TRANSMIT SECTION

Analog signals are input to an operational amplifier to provide gain adjustment. This amplifier is followed by a 2nd order analog anti-aliasing filter (ANTI-ALIAS). This filter provides attenuation of 40dB (typical) at the 256kHz effective clock frequency of the following switched capacitor cosine filter (COS). From the cosine filter, the signals enter a 5th order low-pass filter (LPF) clocked at 128kHz, followed by a 3rd order high-pass filter (HPF) clocked at 8kHz. The resulting band-pass characteristics meet both the D3/D4 specification and the CCITT G.712 recommendation. The output of the high-pass filter is then sampled by the coder (CODEC) at 8kHz. This coder transforms the analog signals into 8-bit words using compressing law. The encoded PCM data is then output serially from the OUTPUT REGISTER at a frequency determined by the external clock, 64kHz to 3.152MHz. An auto-zero circuit (AZ) is utilized for DC offset correction.

RECEIVE SECTION

This filter smooths the decoded signals and corrects for SinX/X attenuation caused by the 8kHz sample and hold operation. The decoder (DECODER) reconstructs the analog signals from the PCM data using expanding law. The decoder is followed by a 5th order low pass filter (LPF). This filter smooths the decoded signals and corrects them for the SinX/X attenuation due to the 8kHz sampling and holding operation.

INTERNAL CLOCK
(MB6021A, MB6022A)
Two independent phase locked loops (PLL) generate internal clocks for the transmit and receive sections from the respective synchronization clocks (XSYNC and RSYNC).

(MB6025A, MB6026A)
The phase locked loop (PLL) generates internal clocks for the transmit and receive sections from the synchronization clock (SYNC).

ANALOG LOOPBACK MODE

The analog loopback mode allows all decoding and coding functions to be exercised without using the analog input (AIN) and analog output (AOUT). In this mode, a digital input signal is decoded and internally routed to the transmit filters.
The output is available from the digital output (DOUT). The analog output (AOUT) is forced to the analog ground (AG) level. The analog loopback mode is selected by connecting the PD/L input to the negative supply voltage (–VS).

POWER DOWN MODE
(MB6021A, MB6022A)
Two power down modes are provided. The transmit and receive sections independently go into power down operation in the absense of the respective synchronization clock (XSYNC and RSYNC). If the external power down input (PD/L) is connected to a TTL low level, both the transmit and receive section are powered down regardless of the synchronization clocks. During power down operation, AOUT is forced to the level of AG, and DOUT goes into a high-impedance state.
(MB6025A, MB6026A)
Two power down modes are provided. The device enters power down mode when the synchronization clock (SYNC) is stopped. Also, when the external power down input (PD/L) is forced to a TTL low level, power down mode is initiated regardless of the state of the SYNC clock. During power down mode, AOUT is forced to the level of AG, and DOUT goes into a high impedance state.

TEST MODE
If TEST pin is connected to –VS, test mode allows independent evalution of the coder and decoder. In this mode, AIN is internally connected to the input of the coder and its output is available on the DOUT pin. Also, the output of the decoder is made available on pin AOUT.

MB6021A
MB6022A
MB6025A
MB6026A

PIN DESCRIPTION

MB6021A, MB6022A			MB6025A, MB6026A		Description
Pin Name	Pin No.		Pin Name	Pin No.	
	DIP	PLCC			
AIN	1	1	AIN	1	Analog Input This is an input pin for analog signals to be filtered and coded.
GA1 GA2	2 3	2 3	GA1 GA2	2 3	Gain Adjust 1 Gain Adjust 2 These pins are provided for adjusting the gain of transmit section. GA1 and GA2 are the inverting input and output of the amplifier, respectively. GA2 can drive a load impedance of 10kΩ or more and 50pF or less.
AG	4	4	AG	4	Analog Ground All analog signals are referenced to this pin.
NC	–	5	–	4	No connection
AOUT	5	6	AOUT	5	Analog Output This pin outputs the decoded and filtered analog signals. It can drive a load impedance of 3kΩ or greater, and 100pF or less. This output is forced to AG level in the analog loopback mode and power down mode.
TEST	6	7	TEST	6	TEST If this pin is at the TTL low level or left open, normal operation mode is selected. If this pin is connected to –VS, the test mode is selected. In this mode, AIN is internally connected to the input of the coder and its output is available on the DOUT pin. Also the output of the decoder is directly available on the AOUT pin. Apply voltage should not exceed 2.0V.
+VS	7	8	+VS	7	Positive Voltage Supply, +5V ±5%
DIN	8	9	–	–	Digital Input This is a TTL compatible input to the decoder and accepts an eight-bit data word into the shift register on the falling edge of RCLK.
–	–	–	NC	8	No connection
RCLK	9	10	–	–	Receive Clock This TTL compatible input defines the bit rate on the receive PCM highway. The device can operate with clock rates of 64kHz to 3.152MHz. The digital PCM codes are accepted on the falling edge of the clock.
–	–	–	DIN	9	Digital Input This is a TTL compatible input to the decoder and accepts an eight-bit data word into the shift register on the falling edge of CLK.
XCLK	10	11	–	–	Transmit Clock This TTL compatible input defines the bit rate on the transmit PCM highway. The device can operate with bit rates of 64kHz to 3.152MHz. The digital PCM codes are shifted out of the digital output (DOUT) pin on the rising edge of the XCLK.

MB6021A
MB6022A
MB6025A
MB6026A

T-75-11-09

PIN DESCRIPTION (Cont'd)

MB6021A, MB6022A			MB6025A, MB6026A		Description
Pin Name	Pin No.		Pin Name	Pin No.	
	DIP	PLCC			
–	–	–	CLK	10	**Bit Clock** This TTL compatible input defines the bit rate on the PCM highway. The device can operate with bit rates of 64kHz to 3.152MHz. The digital PCM codes are shifted out of the digital output (DOUT) pin on the rising edge of the clock and shifted into the digital input (DIN) pin on the falling edge.
RSYNC	11	12	–	–	**Receive Synchronization Clock** This TTL compatible input defines the beginning of the receive timeslot on the receive PCM highway. It must be synchronized with RCLK. The clock rate is typically 8kHz and its duration can be equal to or more than one RCLK cycle.
–	–	–	SYNC	11	**Synchronization Clock** This TTL compatible input defines the beginning of the transmit and receive timeslot on the PCM highway. It must be synchronized with CLK. The clock rate is typically 8kHz and its duration can be equal to or more than one CLK cycle.
XSYNC	12	13	–	–	**Transmit Synchronization Clock** This TTL compatible input defines the beginning of the transmit timeslot on the transmit PCM highway. It must be synchronized with XCLK. The clock rate is typically 8kHz and its duration can be equal to or more than one XCLK cycle.
NC	–	14	NC	12	No Connection
DG	13	15	DG	13	**Digital Ground** All digital signals are reference to this pin.
PD/L	14	16	PD/L	14	**Power Down/Analog Loopback** This three level input is provided fot the selection of power down mode or analog loopback mode. If this pin is at the TTL high level, the normal operation is selected. If this pin is at the TTL low level, the device is powered down regardless of the synchronization clocks. If this pin is connected to –VS, the analog loopback mode is selected. In this mode, the output of the receive filter is internally connected to the input of the transmit filter and AOUT is forced to AG level.
DOUT	15	17	DOUT	15	**Digital Output** This is a TTL compatible open-drain output. A pull-up resistor greater than 0.5kΩ must be connected to +VS. PCM digital codes are shifted out of the device on the rising edges of XCLK in a serial format. This output goes into high-impedance state when eight bits are shifted out of the output shift register.
–VS	16	18	–VS	16	Negative Voltage Supply, –5V ±5%

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MB6021A
MB6022A
MB6025A
MB6026A

T-75-11-09

RECOMMENDED OPERATING CONDITIONS

Rating	Pin		Symbol	Value			Unit
	DIP	PLCC		Min	Typ	Max	
Positive Supply Voltage	7	8	$+V_S$	+4.75	+5.0	+5.25	V
Negative Supply Voltage	16	18	$-V_S$	−5.25	−5.0	−4.75	V
Digital Output Load Resistance	15	17	R_{DL}	0.5			KΩ
Digital output Load Capacitance	15	17	C_{DL}			144	pF
Analog Output Load Resistance	5	6	R_L	3			KΩ
Analog Output Load Capacitance	5	6	C_L			100	pF
Operating Temperature			T_{OP}	0	25	70	°C

DC CHARACTERISTICS
(Recommended operating conditions unless otherwise noted.)

Parameter	Conditions	Pin MB6021A MB6022A		Pin MB6025A MB6026A	Symbol	Value			Unit
		DIP	PLCC			Min	Typ	Max	
Positive Supply Current	Operating	7	8	7	$+I_{VS}$		7.0	10.0	mA
Negative Supply Current	Operating	16	18	16	$-I_{VS}$	−10.0	−5.0		mA
Positive Supply Current Power Down Mode	XSYNC=RSYNC=VIL SYNC=VIL	7	8	7	$+I_{VSST}$		1.0	2.0	mA
	PD/L=VIL						0.3	1.0	mA
Negative Supply Current Power Down Mode	XSYNC=RSYNC=VIL SYNC=VIL	16	18	16	$-I_{VSST}$	−0.5	−0.1		mA
	PD/L=VIL					−0.5	−0.1		mA

MB6021A
MB6022A
MB6025A
MB6026A

DC CHARACTERISTICS (Cont'd)

T-75-11-09

Parameter	Conditions	Pin MB6021A/22A		Pin MB6025A/26A	Symbol	Value			Unit
		DIP	PLCC			Min	Typ	Max	
Digital Input High Voltage		8, 9, 10 11, 12, 14	9, 10, 11 12, 13, 16	9, 10, 11, 14	V_{IH}	2.0		+VS	V
Digital Input Low Voltage		8, 9, 10 11, 12, 14	9, 10, 11 12, 13, 16	9, 10, 11, 14	V_{IL}	0		0.8	V
Digital Input High Current		8, 9, 10 11, 12, 14	9, 10, 11 12, 13, 16	9, 10, 11, 14	I_{IH}			10	μA
Digital Input Low Current		8, 9, 10 11, 12, 14	9, 10, 11 12, 13, 16	9, 10, 11, 14	I_{IL}			10	μA
Digital Input Capacitance		8, 9, 10 11, 12, 14	9, 10, 11 12, 13, 16	9, 14	C_{DIN1}			10	pF
Digital Input Capacitance		--	--	10, 11	C_{DIN2}			20	pF
Digital Output Low Voltage	$R_{OL}=0.5k\Omega$ $+I_{OL}=0.4mA$	15	17	15	V_{OL1}			0.4	V
Digital Output Leakage Current		15	17	15	I_{LO}			10	μA
Digital Output Capacitance		15	17	15	C_{DOUT}			12	pF
Analog Input Offset Voltage		1	1	1	A_{INOFF}	−200	0	200	mV
Analog Input Resistance		1	1	1	R_{AIN}	300			kΩ
Analog Input Capacitance		1	1	1	C_{AIN}			10	pF
Analog Output Offset Voltage		5	6	5	A_{OUTOFF}	−150		150	mV
Analog Output Resistance		5	6	5	R_{AOUT}		10	30	Ω
Pull Down Current	$V_{IH}=+2.0V$	6	7	6	I_{PLD}	0		80	μA

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MB6021A
MB6022A
MB6025A
MB6026A

AC CHARACTERISTICS (MB6021A, MB6022A)
(Recommended operating conditions unless otherwise noted.)

Parameter	Conditions	Pin No.		Symbol	Values			Unit
		DIP	PLCC		Min	Typ	Max	
Digital Input Rise Time	0.8V→2.0V	8, 9, 10 11, 12	9, 10, 11 12, 13	t_r			50	ns
Digital Input Fall Time	2.0V→0.8V	8, 9, 10 11, 12	9, 10, 11 12, 13	t_f			50	ns
Shift Clock Frequency		9, 10	10, 11	F_c	64		3152	kHz
Shift Clock High Width	$V_{IH}=2.0V$	9, 10	10, 11	t_{WCH}	140			ns
Shift Clock Low Width	$V_{IL}=0.8V$	9, 10	10, 11	t_{WCL}	140			ns
Synchronization Frequency		11, 12	12, 13	F_s		8		kHz
Synchronization High Width	$V_{IH}=2.0V$	11, 12	12, 13	t_{WSH}	$1/F_c$ (F_c: MHz)		117	μs
XSYNC to XCLK Delay		10, 12	11, 13	t_{SX}	100			ns
XCLK to XSYNC Delay		10, 12	11, 13	t_{XS}	50			ns
RSYNC to RCLK Delay		9, 11	10, 12	t_{SR}	100			ns
RCLK to RSYNC Delay		9, 11	10, 12	t_{RS}	50			ns
RCLK to DIN Delay		8, 9	9, 10	t_{RD}	50			ns
DIN to RCLK Delay		8, 9	9, 10	t_{DR}	50			ns
XCLK or XSYNC to DOUT Delay	Note1 BIT1	10, 12, 15	11, 13, 17	t_{ZD}	30		200	ns
XCLK to DOUT Delay	Note1 BIT2-8	10, 15	11, 17	t_{XD}	30		200	ns
XCLK to DOUT Disable Time	High-Z	10, 15	11, 17	t_{DZ}	30		200	ns
DOUT Fall Time		15	17	t_{OF}	10		100	ns

Note 1 : DOUT Load Conditions: $R_{DL}=0.5k\Omega$, $C_{DL}=144pF$, $+I_{OL}=0.4mA$

MB6021A
MB6022A
MB6025A
MB6026A

AC CHARACTERISTICS (MB6025A, MB6026A)   T-75-11-09
(Recommended operating conditions unless otherwise noted.)

Parameter	Conditions	Pin	Symbol	Min	Typ	Max	Unit
Digital Input Rise Time	0.8V→2.0V	9, 10, 11	t_r			50	ns
Digital Input Fall Time	2.0V→0.8V	9, 10, 11	t_f			50	ns
Shift Clock Frequency		10	F_c	64		3152	kHz
Shift Clock High Width	V_{IH}=2.0V	10	t_{WCH}	140			ns
Shift Clock Low Width	V_{IL}=0.8V	10	t_{WCL}	140			ns
Synchronization Frequency		11	F_s		8		kHz
Synchronization High Width	V_{IH}=2.0V	11	t_{WSH}	$1/F_c$ (F_c: MHz)		117	μs
SYNC to CLK Delay		10, 11	t_{SC}	100			ns
CLK to SYNC Delay		10, 11	t_{CS}	50			ns
CLK to DIN Delay		9, 10	t_{CI}	50			ns
DIN to CLK Delay		9, 10	t_{IC}	50			ns
SYNC to DOUT Delay	Note1 BIT1	10, 11, 15	t_{ZO}	30		200	ns
CLK or SYNC to DOUT Delay	Note1 BIT2-8	10, 15	t_{CO}	30		200	ns
CLK to DOUT Disable Time	Note 1	10, 15	t_{OZ}	30		200	ns
DOUT Fall Time	Note 1	15	t_{Of}	10		100	ns

Note 1 : DOUT Load Conditions: R_{OL}=0.5kΩ, C_{OL}=144pF, +I_{OL}=0.4mA

5-29

MB6021A
MB6022A
MB6025A
MB6026A

T-75-11-09

Fig. 3 – MB6021A, MB6022A TIMING DIAGRAM
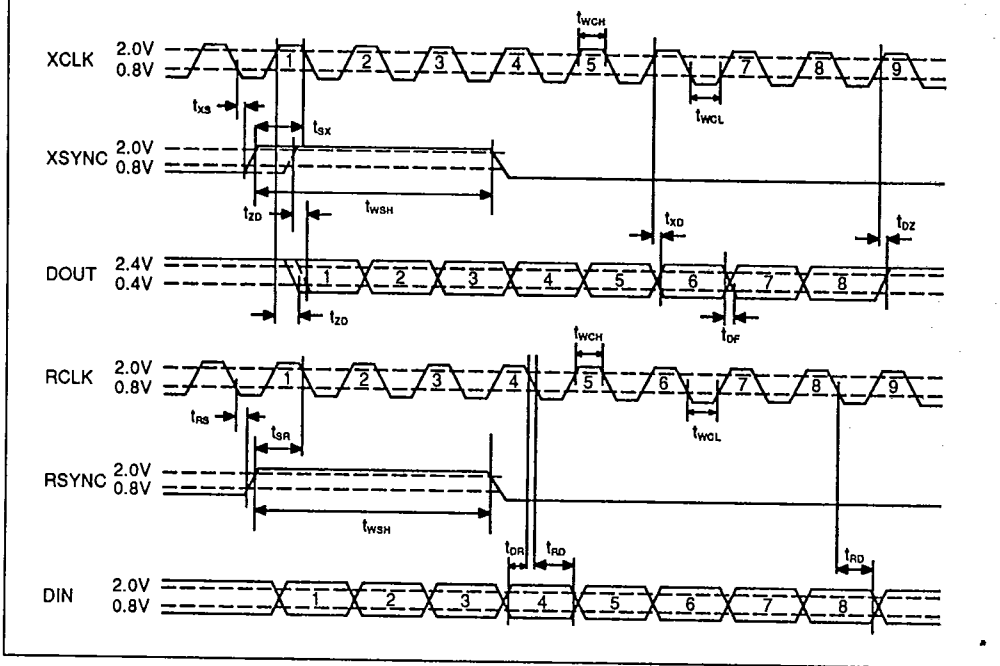
Fig. 4 – MB6025A, MB6026A TIMING DIAGRAM
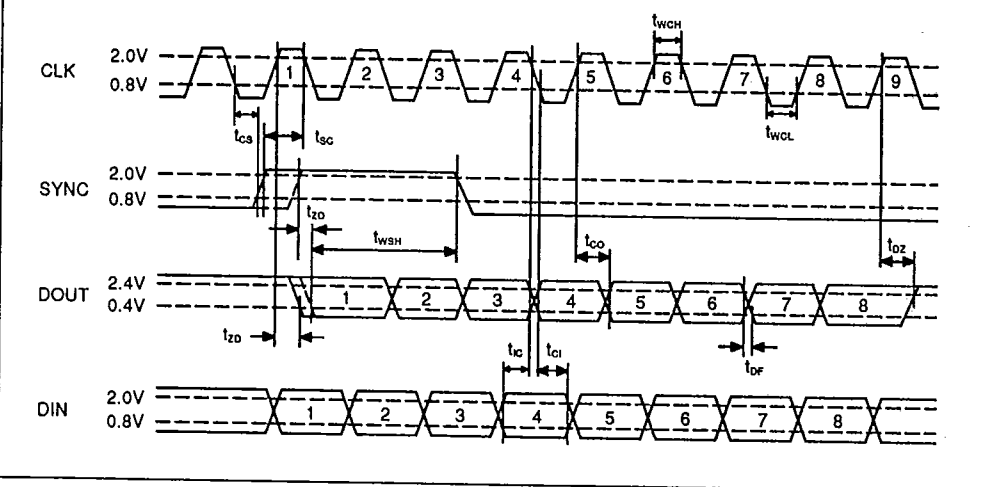
TRANSMISSION CHARACTERISTICS OF μ-LAW (MB6021A, MB6025A)

T-75-11-09

(Recommended operating conditions unless otherwise noted.)

Parameter	Conditions		Symbol	Value			Unit
				Min	Typ	Max	
Signal to Distortion (A to A)	1020Hz tone (C Message)	+3 to −30dBm0 −40dBm0 −45dBm0	SDA	35.0 30.0 25.0			dB dB dB
Signal to Distortion (A to D)	1020Hz tone (C Message)	+3 to −30dBm0 −40dBm0 −45dBm0	SDX	36.0 31.0 26.0			dB dB dB
Signal to Distortion (D to A)	1020Hz tone (C Message)	+3 to −30dBm0 −40dBm0 −45dBm0	SDR	36.0 31.0 26.0			dB dB dB
Gain Tracking (A to A)	1020Hz tone	+3 to −40dBm0 −40 to −50dBm0 −50 −55dBm0	GTA	−0.4 −0.8 −2.0		0.4 0.8 2.0	dB dB dB
Gain Tracking (A to D)	1020Hz tone	+3 to −40dBm0 −40 to −50dBm0 −50 to −55dBm0	GTX	−0.2 −0.4 −0.8		0.2 0.4 0.8	dB dB dB
Gain Tracking (D to A)	1020Hz tone	+3 to −40dBm0 −40 to −50dBm0 −50 to −55dBm0	GTR	−0.2 −0.4 −0.8		0.2 0.4 0.8	dB dB dB
Frequency Response (A to A)	0 − 60Hz 60 − 300Hz 300 − 3000Hz 3000 − 3400Hz 3400 − 4600Hz 4.6 − 12kHz Relative to 0dBm0, 820Hz		FRA	24.0 −0.2 −0.2 −0.2 Note 1 64.0		0.3 1.6	dB dB dB dB dB dB
Frequency Response (A to D)	0 − 60Hz 60 − 300Hz 300 − 3000Hz 3000 − 3400Hz 3400 − 4600Hz 4.6 − 12kHz Relative to 0dBm0, 820Hz		FRX	24.0 −0.1 −0.1 −0.1 Note 2 32.0		0.15 0.8	dB dB dB dB dB dB
Frequency Response (D to A)	0 − 300Hz 300 − 3000Hz 3000 − 3400Hz 3400 − 4600Hz 4.6 − 12kHz Relative to 0dBm0, 820Hz		FRR	−0.1 −0.1 −0.1 Note2 32.0		0.15 0.8	dB dB dB dB dB dB

Note 1 : $29 (1- \sin \frac{\pi (4000 -f)}{1200})$ Note 2: $14.5 (1- \sin \frac{\pi (4000 -f)}{1200})$

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MB6021A
MB6022A
MB6025A
MB6026A

T-75-11-09

TRANSMISSION CHARACTERISTICS OF μ-LAW (MB6021A, MB6025A) (Cont'd)

Parameter	Conditions	Symbol	Value			Unit
			Min	Typ	Max	
Idle Channel Noise (A to A)	C Message	ICNA		−80	−72.0	dBm0c
Idle Channel Noise (A to D)	C Message	ICNX		−83	−74.0	dBm0c
Idle Channel Noise (D to A)	C Message	ICNR		−83	−78.0	dBm0c
Crosstalk (A to A)	1020Hz, 0dBm0	CTA			−66	dB
Crosstalk (D to D)	1020Hz, 0dBm0	CTD			−66	dB
Absolute Level	Overload Level 3.17dBm0	VABS		2.500		Vop
Analog Input Level	1020Hz, 0dBm0 ±VS=±5.0V, T_A=25°C	AIL		1.227		Vrms
Analog Output Level	1020Hz, 0dBm0 ±VS=±5.0V, T_A=25°C	AOL	1.206	1.227	1.248	Vrms
Gain Accurancy (A to A)	1020Hz, 0dBm0 Internal VREF	GAA	−0.5	0	+0.5	dB
	±VS=±5.0V, T_A=25°C		−0.3	0	+0.3	dB
Gain Accurancy (A to D)	1020Hz, 0dBm0 Internal VREF	GAX	−0.25	0	+0.25	dB
	±VS=±5.0V, T_A=25°C Variation with power Supply Variation with Temperature		−0.15	0 ±0.02 ±0.001	+0.15	dB dB dB/°C
Gain Accurancy (D to A)	1020Hz, 0dBm0 Internal VREF	GAR	−0.25	0	+0.25	dB
	±VS=±5.0V, T_A=25°C Variation with power Supply Variation with Temperature		−0.15	0 ±0.02 ±0.001	+0.15	dB dB dB/°C
Propagation Delay (A to A)	FC≥1544kHz	PDA			540	μs

MB6021A
MB6022A
MB6025A
MB6026A

TRANSMISSION CHARACTERISTICS OF μ-LAW (MB6021A, MB6025A) (Cont'd)

Parameter	Conditions	Symbol	Value			Unit
			Min	Typ	Max	
Delay to Distortion (A to A)	500 – 600Hz 600 – 1000Hz 1000 – 2600Hz 2600 – 2800Hz 1020Hz, 0dBm0 Relative to Minimum Delay	DDA			1.5 0.75 0.25 1.5	ms ms ms ms
PSRR (+VS) (A to A)	0<f≤50kHz Idle Channel Noise (C Message) +VS +50mVop AIN=AG	PSRRA+	25	30		dB
PSRR (–VS) (A to A)	0<f≤50kHz Idle Channel Noise (C Message) –VS +50mVop AIN=AG	PSRRA–	35	40		dB
Intermoduration (A to A)	AIN a. 0.47kHz, –10dBm0 b. 0.32kHz, –10dBm0 AOUT (2a–b)	IMA1			–38	dB
Intermoduration (A to A)	AIN a. 1.02kHz, –9dBm0 b. 0.05kHz, –23dBm0 AOUT (a–b)	IMA2			–52	dBm0
Signal Frequency Noise (A to A)	0 – 4kHz 4 – 200kHz AIN=AG	SFNA			–70 –50	dBm0 dBm0
Discrimination (A to A)	AIN=0dBm0 4.6 – 200kHz	DISA	30			dB
In Band Spurious (A to A)	2nd, 3rd Harmonic AIN=0dBm0, 700 – 1100Hz	IBSA	43			dB

5

MB6021A
MB6022A
MB6025A
MB6026A

TRANSMISSION CHARACTERISTICS OF A-LAW
(MB6022A, MB6026A)

(Recommended operating conditions unless otherwise noted.)

Parameter	Conditions		Symbol	Value			Unit
				Min	Typ	Max	
Signal to Distortion (A to A)	CCITT G. 712 Method 2 1020Hz tone P Message	+3 to –30dBm0 –40dBm0 –45dBm0	SDA	35.0 30.0 25.0			dB dB dB
	CCITT G. 712 Method 1	–3dBm0 –6 to –27dBm0 –34dBm0 –40dBm0 –55dBm0		28.0 35.5 33.5 28.5 13.5			dB dB dB dB dB
Signal to Distortion (A to D)	CCITT G. 712 Method 2 1020Hz tone P Message	+3 to –30dBm0 –40dBm0 –45dBm0	SDX	36.0 31.0 26.0			dB dB dB
	CCITT G. 712 Method 1	–3dBm0 –6 to –27dBm0 –34dBm0 –40dBm0 –55dBm0		30.0 36.0 34.0 29.5 14.5			dB dB dB dB dB
Signal to Distortion (D to A)	CCITT G. 712 Method 2 1020Hz tone P Message	+3 to –30dBm0 –40dBm0 –45dBm0	SDR	36.0 31.0 26.0			dB dB dB
	CCITT G. 712 Method 1	–3dBm0 –6 to –27dBm0 –34dBm0 –40dBm0 –55dBm0		30.0 36.0 34.0 29.5 14.5			dB dB dB dB dB

MB6021A
MB6022A
MB6025A
MB6026A

TRANSMISSION CHARACTERISTICS OF A-LAW (MB6022A, MB6026A) (Cont'd)

T-75-11-09

Parameter	Conditions		Symbol	Value			Unit
				Min	Typ	Max	
Gain Tracking (A to A)	CCITT G. 712 Method 2 1020Hz tone	+3 to −40dBm0 −40 to −50dBm0 −50 to −55dBm0	GTA	−0.4 −0.8 −2.0		0.4 0.8 2.0	dB dB dB
	CCITT G. 712 Method 1	−10 to −55dBm0 −55 to −60dBm0		−0.5 −1.0		0.5 1.0	dB dB
Gain Tracking (A to D)	CCITT G. 712 Method 2 1020Hz tone	+3 to −40dBm0 −40 to −50dBm0 −50 to −55dBm0	GTX	−0.2 −0.4 −0.8		0.2 0.4 0.8	dB dB dB
	CCITT G. 712 Method 1	−10 to −50dBm0 −50 to −55dBm0 −55 to −60dBm0		−0.25 −0.4 −0.8		0.25 0.4 0.8	dB dB dB
Gain Tracking (D to A)	CCITT G. 712 Method 2 1020Hz tone	+3 to −40dBm0 −40 to −50dBm0 −50 to −55dBm0	GTR	−0.2 −0.4 −0.8		0.2 0.4 0.8	dB dB dB
	CCITT G. 712 Method 1	−10 to −50dBm0 −50 to −55dBm0 −55 to −60dBm0		−0.25 −0.4 −0.8		0.25 0.4 0.8	dB dB dB
Frequency Response (A to A)	0 − 60Hz 60 − 300Hz 300 − 3000Hz 3000 − 3400Hz 3400 − 4600Hz 4.6 − 12kHz Relative to 0dBm0, 820Hz		FRA	24.0 −0.2 −0.2 −0.2 Note 1 64.0		0.3 1.6	dB dB dB dB dB dB
Frequency Response (A to D)	0 − 60Hz 60 − 300Hz 300 − 3000Hz 3000 − 3400Hz 3400 − 4600Hz 4.6 − 12kHz Relative to 0dBm0, 820Hz		FRX	24.0 −0.1 −0.1 −0.1 Note 2 32.0		0.15 0.8	dB dB dB dB dB dB
Frequency Response (D to A)	0 − 300Hz 300 − 3000Hz 3000 − 3400Hz 3400 − 4600Hz 4.6 − 12kHz Relative to 0dBm0, 820Hz		FRR	−0.1 −0.1 −0.1 Note2 32.0		0.15 0.8	dB dB dB dB dB dB

Note 1 : $29 (1− \text{Sin} \frac{\pi (4000−f)}{1200})$ Note 2: $14.5 (1− \text{Sin} \frac{\pi (4000−f)}{1200})$

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MB6021A
MB6022A
MB6025A
MB6026A

T-75-11-09

TRANSMISSION CHARACTERISTICS OF A-LAW (MB6022A, MB6026A) (Cont'd)

Parameter	Conditions	Symbol	Value			Unit
			Min	Typ	Max	
Idle Channel Noise (A to A)	P Message	ICNA		−80	−72.0	dBm0p
Idle Channel Noise (A to D)	P Message	ICNX		−83	−74.0	dBm0p
Idle Channel Noise (D to A)	P Message	ICNR		−83	−78.0	dBm0p
Crosstalk (A to A)	1020Hz, 0dBm0	CTA			−66	dB
Crosstalk (D to D)	1020Hz, 0dBm0	CTD			−66	dB
Absolute Level	Overload Level 3.14dBm0	VABS		2.500		Vop
Analog Input Level	1020Hz, 0dBm0 Internal VREF ±VS=±5.0V, T_A=25°C	AIL		1.231		Vrms
Analog Output Level	1020Hz, 0dBm0 Internal VREF ±VS=±5.0V, T_A=25°C	AOL	1.210	1.231	1.252	Vrms
Gain Accurancy (A to A)	1020Hz, 0dBm0 Internal VREF	GAA	−0.5	0	+0.5	dB
	±VS=±5.0V, T_A=25°C		−0.3	0	+0.3	dB
Gain Accurancy (A to D)	1020Hz, 0dBm0 Internal VREF	GAX	−0.25	0	+0.25	dB
	±VS=±5.0V, T_A=25°C Variation with power Supply Variation with Temperature		−0.15	0 ±0.02 ±0.001	+0.15	dB dB dB/°C
Gain Accurancy (D to A)	1020Hz, 0dBm0 Internal VREF	GAR	−0.25	0	+0.25	dB
	±VS=±5.0V, T_A=25°C Variation with power Supply Variation with Temperature		−0.15	0 ±0.02 ±0.001	+0.15	dB dB dB/°C
Propagation Delay (A to A)	FC≥1544kHz	PDA			540	μs

TRANSMISSION CHARACTERISTICS OF A-LAW (MB6022A, MB6026A) (Cont'd)

T-75-11-09

Parameter	Conditions	Symbol	Value			Unit
			Min	Typ	Max	
Delay to Distortion (A to A)	500 – 600Hz 600 – 1000Hz 1000 – 2600Hz 2600 – 2800Hz 1020Hz, 0dBm0 Relative to Minimum Delay	DDA			1.5 0.75 0.25 1.5	ms ms ms ms
PSRR (+VS) (A to A)	0<f≤50kHz Idle Channel Noise (P Message) +VS +50mVop AIN=AG	PSRRA+	25	30		dB
PSRR (–VS) (A to A)	0<f≤50kHz Idle Channel Noise (P Message) –VS +50mVop AIN=AG	PSRRA–	35	40		dB
Intermoduration (A to A)	AIN a. 0.47kHz, –10dBm0 b. 0.32kHz, –10dBm0 AOUT (2a–b)	IMA1			–38	dB
Intermoduration (A to A)	AIN a. 1.02kHz, –9dBm0 b. 0.05kHz, –23dBm0 AOUT (a–b)	IMA2			–52	dBm0
Single Frequency Noise (A to A)	0 – 4kHz 4kHz – 200kHz AIN=AG	SFNA			–70 –50	dBm0 dBm0
Discrimination (A to A)	AIN=0dBm0 4.6kHz – 200kHz	DISA	30			dB
In Band Spurious (A to A)	2nd, 3rd Harmonic AIN=0dBm0, 700 – 1100Hz	IBSA	43			dB

5

MB6021A
MB6022A
MB6025A
MB6026A

PACKAGE DIMENSIONS
PLASTIC DIP (Suffix: –P)

16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(Case No. : DIP-16P-M03)

INDEX-1

INDEX-2

$766^{+.008}_{-.012}$ $(19.45^{+0.20}_{-0.30})$

$.260 \pm .010$
(6.60 ± 0.25)

$.300$ (7.62)
TYP

15° MAX

$047^{+.012}_{-0}$
$(1.20^{+0.30}_{-0})$

$047^{+.012}_{-0}$
$(1.20^{+0.30}_{-0})$

$.010^{+.004}_{-.0004}$
$(0.25^{+0.11}_{-0.01})$

$.183$ (4.65) MAX

$.118$ (3.00) MIN

$.050$ (1.27)
MAX

$.100$ (2.54)
TYP

$.018^{+.006}_{-.002}$
$(0.45^{+0.14}_{-0.05})$

$.020$ (0.51) MIN

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Dimensions in
inches (millimeters)

5

MB6021A
MB6022A
MB6025A
MB6026A

PACKAGE DIMENSIONS

18-LEAD PLASTIC LEADED CHIP CARRIER
(Case No. : LCC-18P-M04)

.322 ± .005
(8.18 ± 0.13)
.285 ± .003
(7.24 ± 0.08)

.134 +.006/-.002 (3.40 +0.15/-0.05)

.060(1.52) MIN
.025(0.64) MIN

INDEX
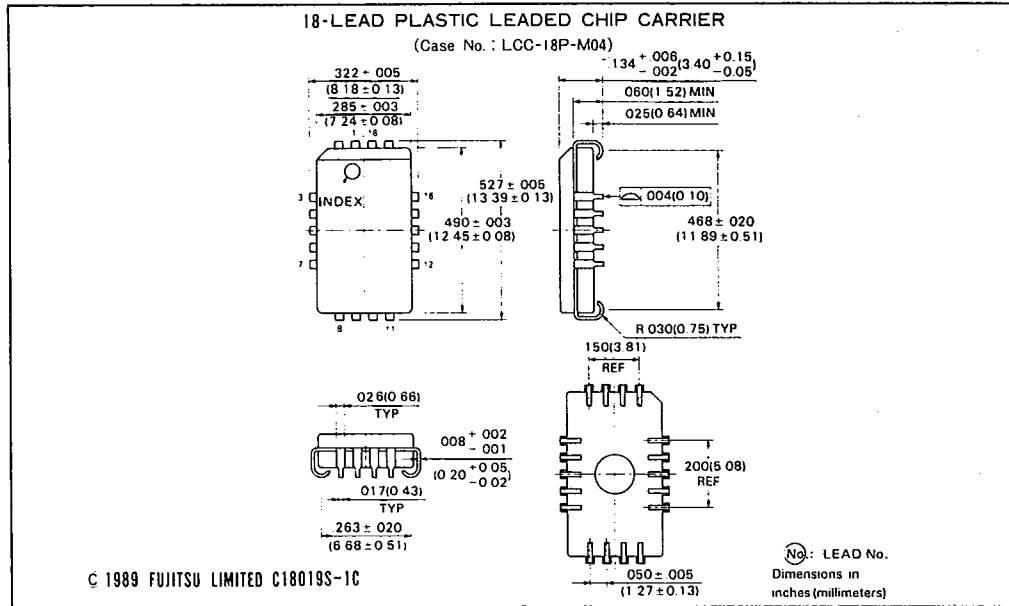
.527 ± .005
(13.39 ± 0.13)
.490 ± .003
(12.45 ± 0.08)

.004(0.10)

.468 ± .020
(11.89 ± 0.51)

R.030(0.75) TYP

.150(3.81)
REF

.026(0.66)
TYP

.008 +.002/-.001
(0.20 +0.05/-0.02)

.017(0.43)
TYP

.263 ± .020
(6.68 ± 0.51)

.200(5.08)
REF

.050 ± .005
(1.27 ± 0.13)

No. : LEAD No.
Dimensions in
inches (millimeters)

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PIN ASSIGNMENT

| | GA1 | AIN | –VS | DOUT | |
| | 2 | 1 | 18 | 17 | |

GA2 | 3
AG | 4
NC | 5
AOUT | 6
TEST | 7

(TOP VIEW)

16 | PD/L
15 | DG
14 | NC
13 | XSYNC
12 | RSYNC

| 8 | 9 | 10 | 11 |
| +VS | DIN | RCLK | XCLK |

MB6021A, MB6022A