

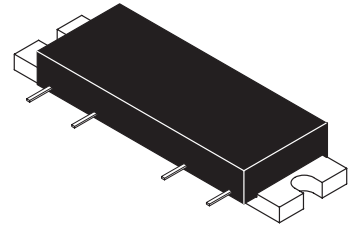
The RF Line
Cellular Band
RF Linear LDMOS Amplifier

Designed for ultra-linear amplifier applications in 50 ohm systems operating in the cellular frequency band. A silicon FET Class A design provides outstanding linearity and gain. In addition, the excellent group delay and phase linearity characteristics are ideal for the most demanding analog or digital modulation systems, such as TDMA and CDMA.

- Third Order Intercept: 50 dBm Typ
- Power Gain: 31 dB Typ (@ f = 880 MHz)
- Excellent Phase Linearity and Group Delay Characteristics
- Ideal for Feedforward Base Station Applications
- For Use in TDMA and CDMA Multi-Carrier Applications

MHL9838

800–925 MHz
8.0 W, 31 dB
RF LINEAR LDMOS AMPLIFIER



CASE 301AP-02, STYLE 1

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	30	Vdc
RF Input Power	P_{in}	+6	dBm
Storage Temperature Range	T_{stg}	-40 to +100	$^\circ\text{C}$
Operating Case Temperature Range	T_C	-20 to +100	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($V_{DD} = 28 \text{ Vdc}$, $T_C = 25^\circ\text{C}$; 50 Ω System)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current	I_{DD}	—	770	800	mA
Power Gain (f = 880 MHz)	G_p	30	31	32	dB
Gain Flatness (f = 800–925 MHz)	G_F	—	0.1	0.3	dB
Power Output @ 1 dB Comp. (f = 880 MHz)	$P_{out} \text{ 1 dB}$	—	39	—	dBm
Input VSWR (f = 800–925 MHz)	$VSWR_{in}$	—	1.2:1	1.5:1	
Output VSWR (f = 800–925 MHz)	$VSWR_{out}$	—	1.2:1	1.5:1	
Third Order Intercept (f1 = 879 MHz, f2 = 884 MHz)	ITO	49	50	—	dBm
Noise Figure (f = 925 MHz)	NF	—	3.7	4.5	dB

TYPICAL CHARACTERISTICS

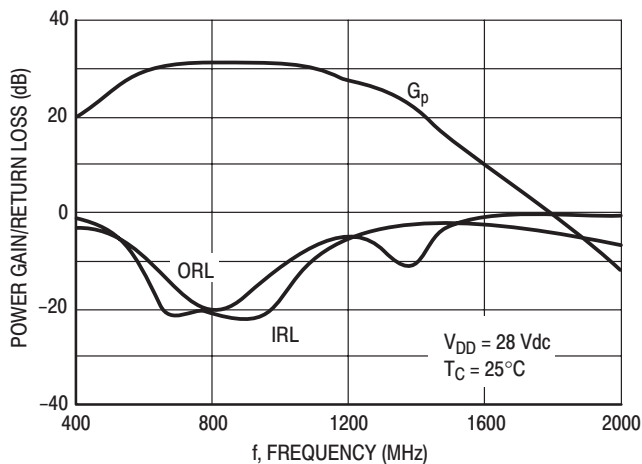


Figure 1. Power Gain, Input Return Loss, Output Return Loss versus Frequency

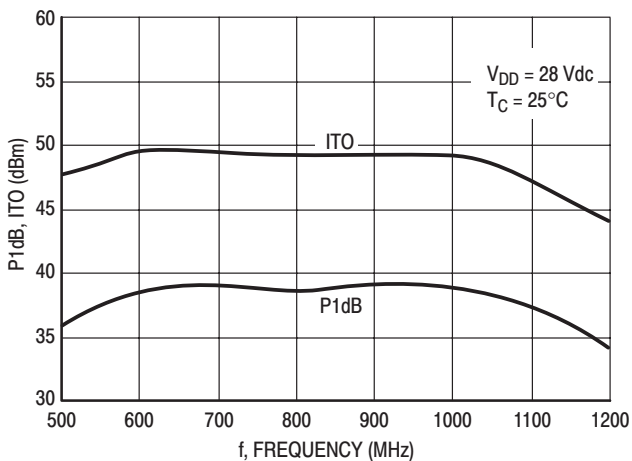


Figure 2. P1dB, ITO versus Frequency

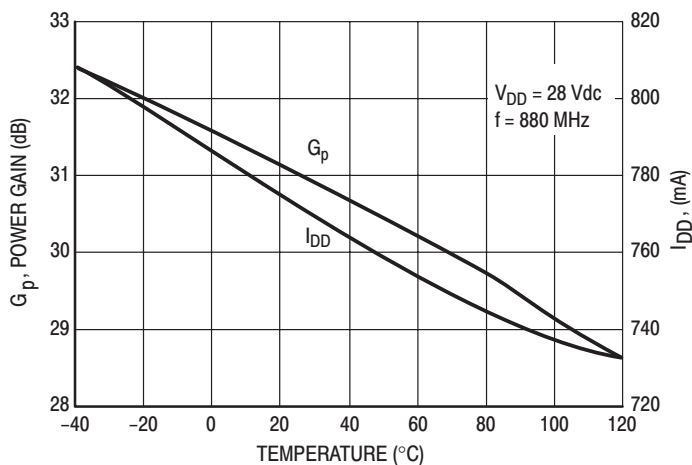


Figure 3. Power Gain, I_{DD} versus Temperature

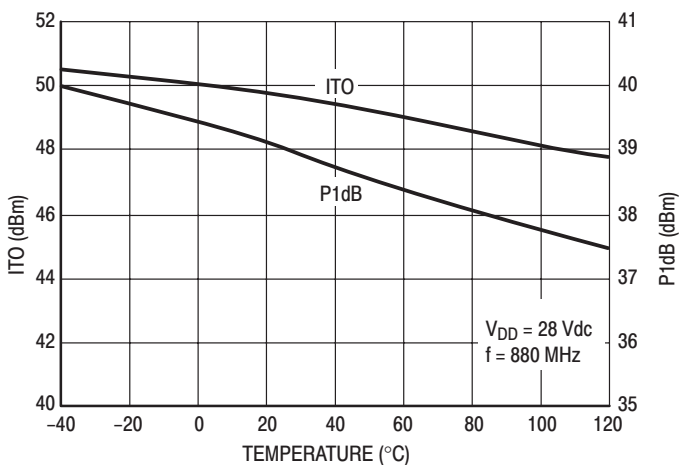


Figure 4. ITO, P1dB versus Temperature

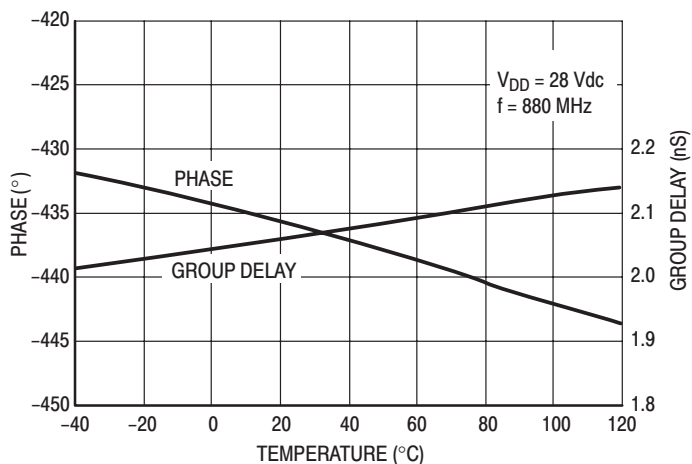


Figure 5. Phase⁽¹⁾, Group Delay⁽¹⁾ versus Temperature

⁽¹⁾In Production Test Fixture

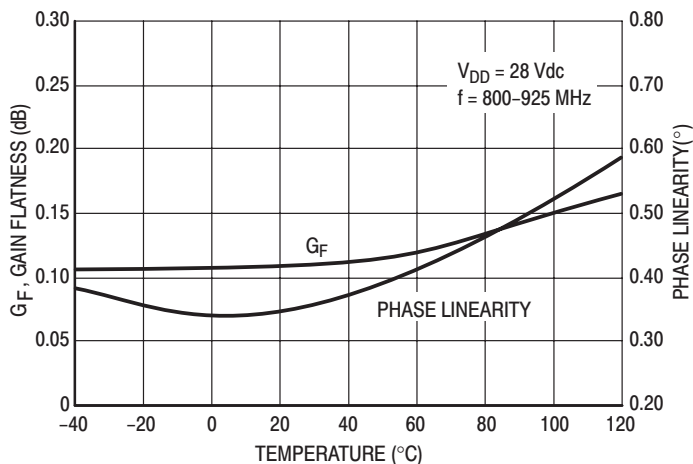


Figure 6. Gain Flatness, Phase Linearity versus Temperature

TYPICAL CHARACTERISTICS

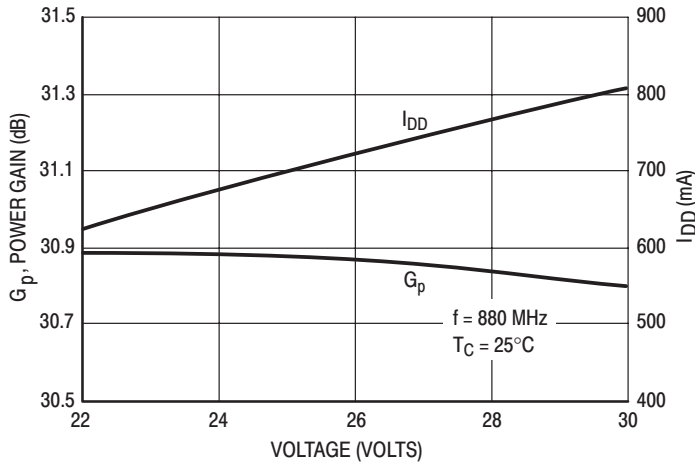


Figure 7. Power Gain, I_{DD} versus Voltage

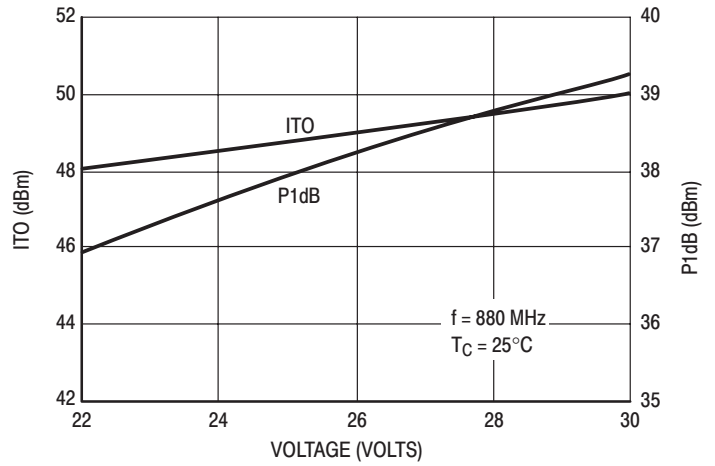


Figure 8. ITO, P1dB versus Voltage

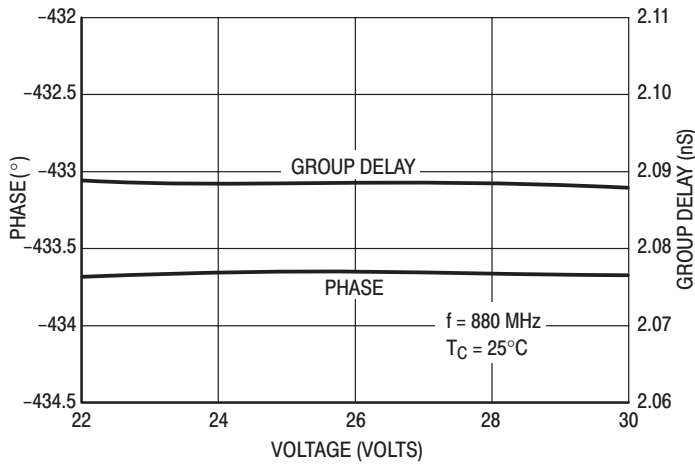


Figure 9. Phase⁽¹⁾, Group Delay⁽¹⁾ versus Voltage
⁽¹⁾In Production Test Fixture

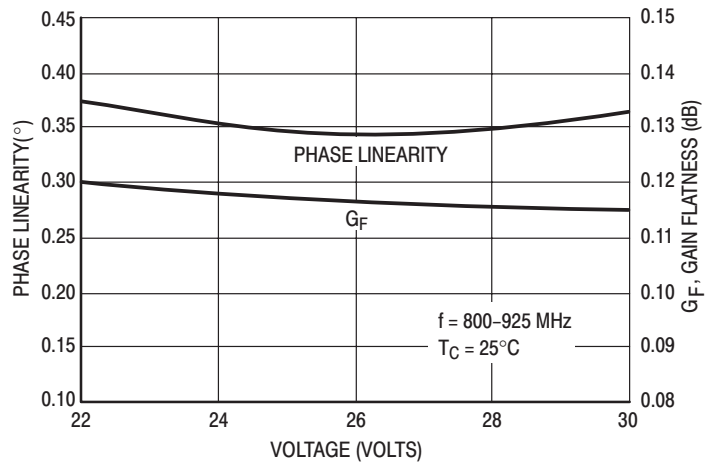
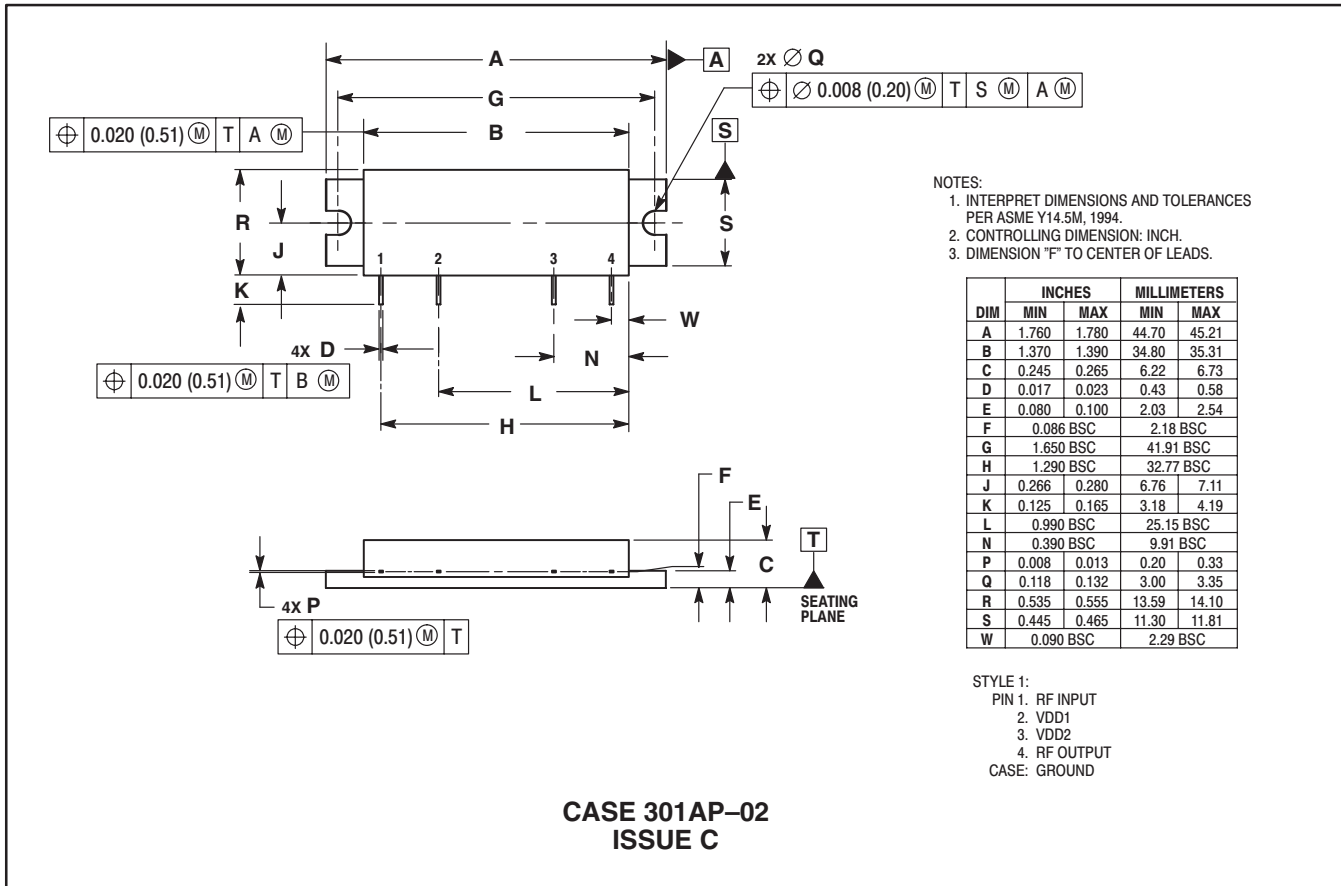



Figure 10. Phase Linearity, Gain Flatness versus Voltage

Freescale Semiconductor, Inc.

PACKAGE DIMENSIONS



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