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NT3980

TFT LCD Source Driver

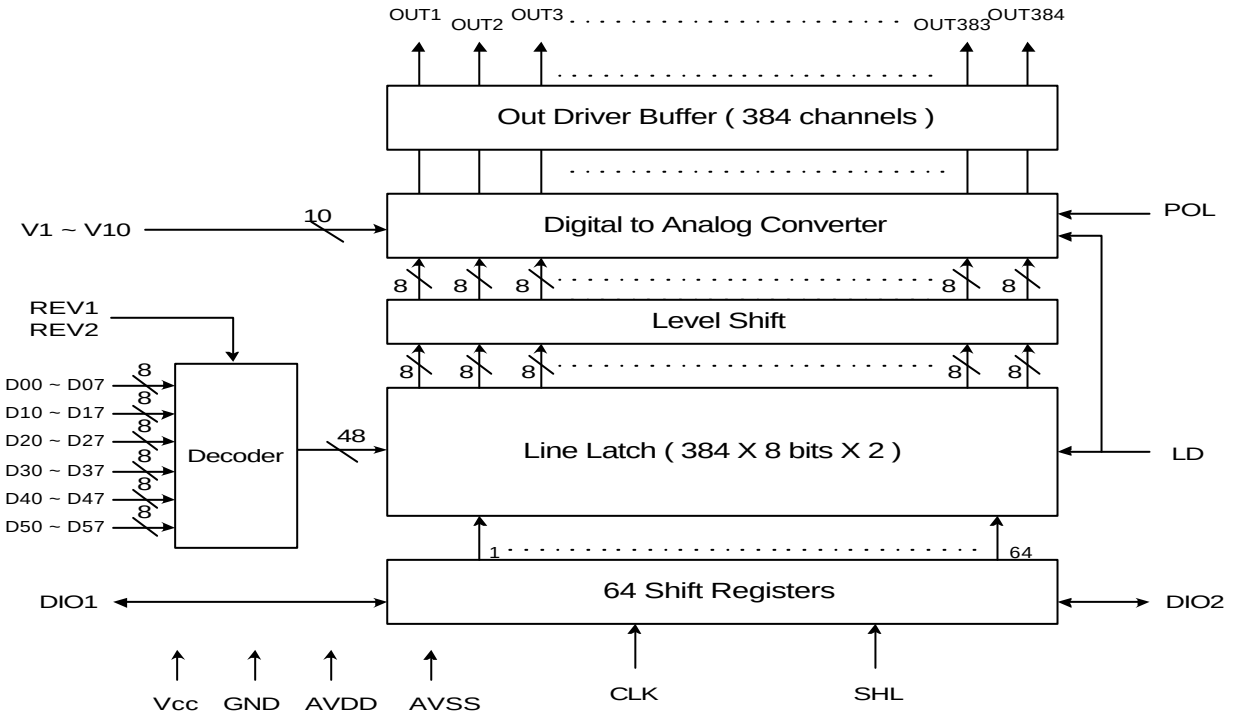
Features

- Output: 384 output channels
- 8-bit resolution /256 gray scales
- Dot inversion with polarity control
- V1 ~ V10 for adjusting Gamma correction
- Power for analog circuit: 7 ~ 10V
- Output dynamic range: 0.1V ~ AVDD-0.1
- Power consumption of analog circuit: 6mA
- Operating frequency: 70MHz(Vcc:3.0V~3.6V)
  45MHz(Vcc:2.5V~3.0V)
- Output deviation: ±2mv
- Data inversion for reducing EMI
- Cascade function with bi-direction shift control
- CMOS silicon gate (p-type substrate)
- TCP package

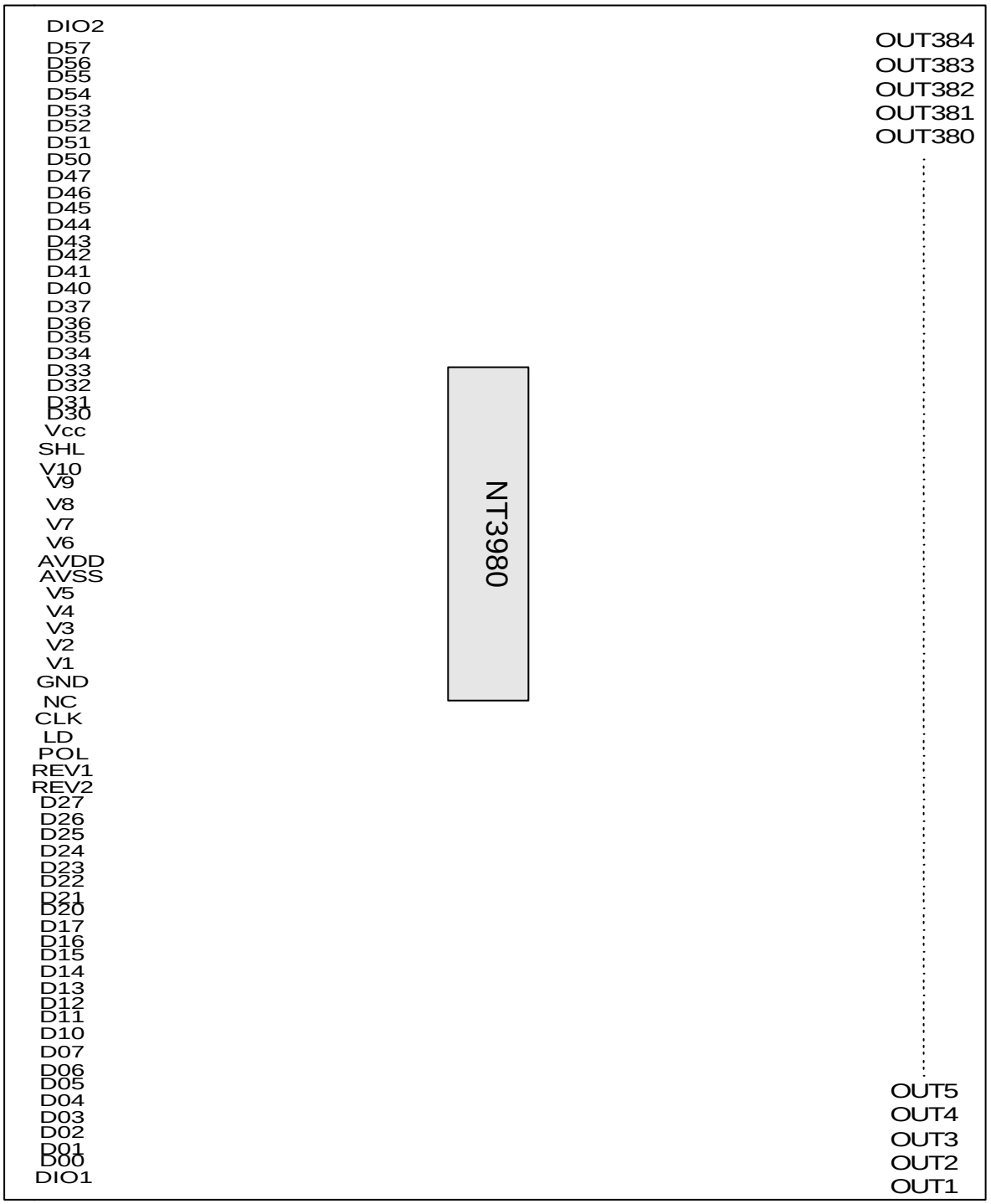
General Description

The NT3980 is a data driver IC for a color TFT LCD panel, XGA and SXGA applications. It receives 8 bit per-pixel digital display data,and generates output voltage for 256 grayscales ,enabling a maximum of 16.77M display colors . For better performance, dot inversion and a wide range voltage output, 10V, are designed in this chip, and for reducing EMI, data inversion control is used. This chip supplies 10 sections of voltage-reference for Gamma correction.

Block diagram



NT3980 TCP (Top view)



Pin Description

<table>
<tr><th>Designation</th><th>I/O</th><th>Description</th></tr>
<tr><td>D07 ~ D00
D17 ~ D10
D27 ~ D20
D37 ~ D30
D47 ~ D40
D57 ~ D50</td><td>I</td><td>Data input. For six 8-bit data,2 pixels, of color data (R, G, B)
DX7 : MSB; DX0 : LSB</td></tr>
<tr><td>REV1
REV2</td><td>I</td><td>Controls whether data are inverted or not.
When “REVx”=1 the data will be inverted. EX. “00” → “FF”, “07” → “F8”, “15” → “EA”, and so on.
REV1: control D0x to D2x ,REV2: control D3x to D5x .
(These two pins can be connected together on TCP.)</td></tr>
<tr><td>V1 ~ V10</td><td>I</td><td>Gamma correction reference voltage. The voltage of these pins must be AVSS< V10< V9< V8<V7<V6; V5<V4<V3<V2<V1< AVDD</td></tr>
<tr><td>OUT1 ~ OUT384</td><td>O</td><td>Output drive signals;</td></tr>
<tr><td>SHL</td><td>I</td><td>Selects left or right shift;
SHL=“1” : DIO1→OUT1,2,3,4,5,6→OUT7,8,9,10,11,12--→OUT379,380,381,382,383,384= DIO2
SHL=“0” : DIO1=OUT1,2,3,4,5,6←OUT7,8,9,10,11,12←-- OUT379,380,381,382,383,384←DIO2
<table>
<tr><th>SHL</th><th>DIO1</th><th>DIO2</th><th>SHIFT</th></tr>
<tr><td>1</td><td>Input</td><td>Output</td><td>Right</td></tr>
<tr><td>0</td><td>Output</td><td>Input</td><td>Left</td></tr>
</table></td></tr>
<tr><td>DIO1
DIO2</td><td>I/O</td><td>Start pulse signal input/output
When SHL is applied high (SHL=”1”), a start high-pulse on DIO1 is latched at the rising edge of the CLK. Then the data are latched serially onto internal latches at the rising edge of the CLK. After all line latches are filled with data, 64 clocks, a pulse is shifted out through the DIO2 pin at the rising edge of the CLK. This function can cascade two or more devices for dot expansion. In normal applications, the DIO2 signal of the first device is connected to the DIO1 of the second stage, the DIO2 of the second one is connected to the DIO1 of the third, and so on, like a daisy chain.
In contrast, when SHL is applied low, a start pulse inputs on DIO2, and a pulse outputs through DIO1.
*Remark : The input pulse-width of DIO1/2 may exceed 1 clock-cycle.</td></tr>
<tr><td>LD</td><td>I</td><td>Latches the polarity of outputs and switches the new data to outputs.
1.At the rising edge, the pin latches the “POL” signal to control the polarity of the outputs.
2.This pin also controls the switch of the line registers that switches the new incoming data to outputs.
*Remark: The LD may switch the new data to outputs at anytime even if the line data are not completely full.</td></tr>
<tr><td>CLK</td><td>I</td><td>Clock input; latching data onto the line latches at the rising edge .
After a start pulse input, display data latching is halted automatically after 64 clock cycles.
*Remark: At least one CLK cycle is necessary during the high-level period of LD.</td></tr>
<tr><td>POL</td><td>I</td><td>Polarity selector for the dot-inversion control. Available at the rising edge of LD.
“POL” value is latched at the rising edge of “LD” to control the polarity of the even or odd outputs.
“POL=1” indicates that even outputs are of positive polarity with a voltage range from V1~V5, and odd outputs are of negative polarity with a voltage range from V6 to V10. On the other hand, if LD receives low level “POL”, even outputs are of negative polarity and odd outputs are of positive polarity.
POL=1: Even outputs range from V1 ~ V5
Odd outputs range from V6 ~ V10
POL=0: Even outputs range from V6 ~ V10
Odd outputs range from V1 ~ V5</td></tr>
<tr><td>AVDD</td><td>I</td><td>Power supply for analog circuit;</td></tr>
<tr><td>AVSS</td><td>I</td><td>Ground pin for analog circuit</td></tr>
<tr><td>Vcc</td><td>I</td><td>Power supply for digital circuit</td></tr>
<tr><td>GND</td><td>I</td><td>Ground pin for digital circuit</td></tr>
</table>

Power on/off sequence:
This IC is a high-voltage LCD driver, so it may be damaged by a large current flow when an incorrect power sequence is used. The recommended connection sequence is to first connect the logical power, Vcc & GND and then connect the drive power, AVDD&AVSS with V1~V10. When shutting off the power, first shut off the drive power and then the logic system, or turn off all power simultaneously.

Relationship between the order of input data and output channels

(1) SHL=" 1" , shift right, a start pulse from DIO1

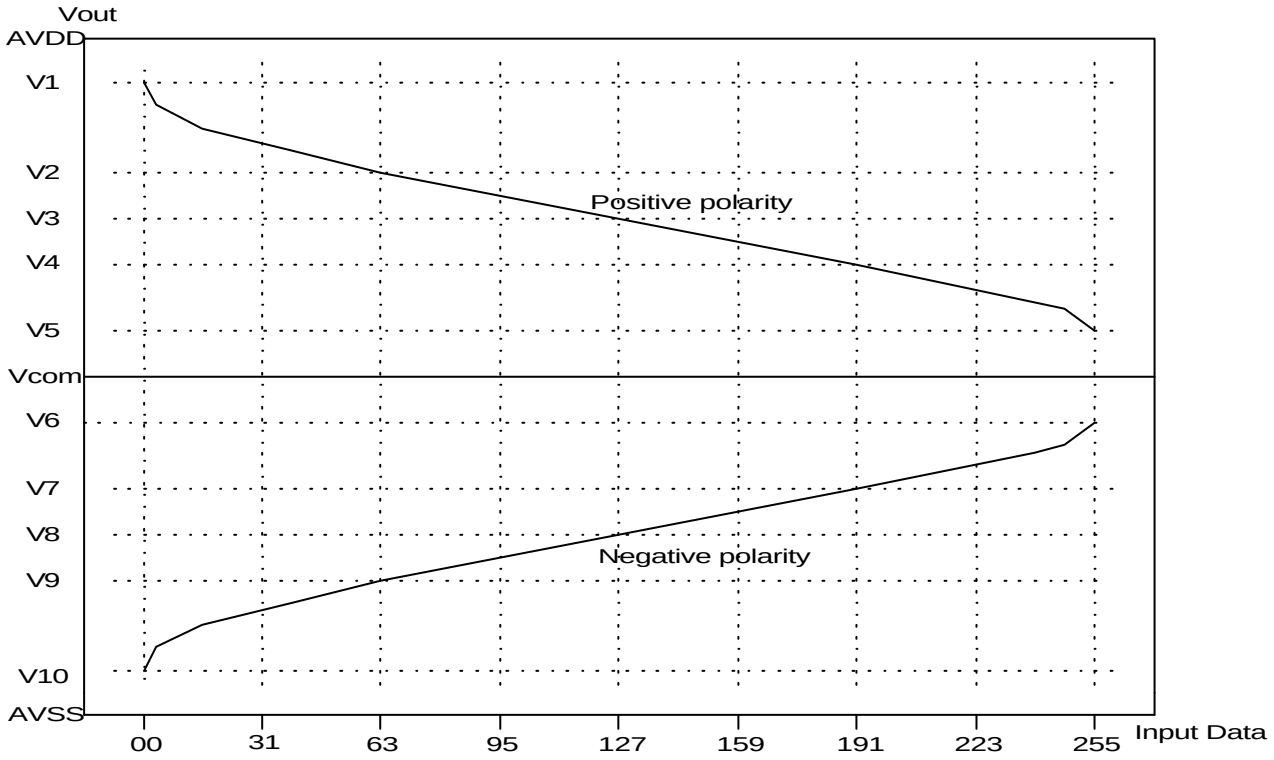
Output	OUT1	OUT2	OUT3	OUT4	OUT5	OUT6	- - -	OUT384
Order	First data						--→	Last data
Data	D07~D00	D17~D10	D27~D20	D37~D30	D47~D40	D57~D50	- - -	D57~D50

(2) SHL=" 0" , shift left, a start pulse from DIO2

Output	OUT379	OUT380	OUT381	OUT382	OUT383	OUT384	- - -	OUT6
Order	First data						--→	Last data
Data	D07~D00	D17~D10	D27~D20	D37~D30	D47~D40	D57~D50	- - -	D57~D50

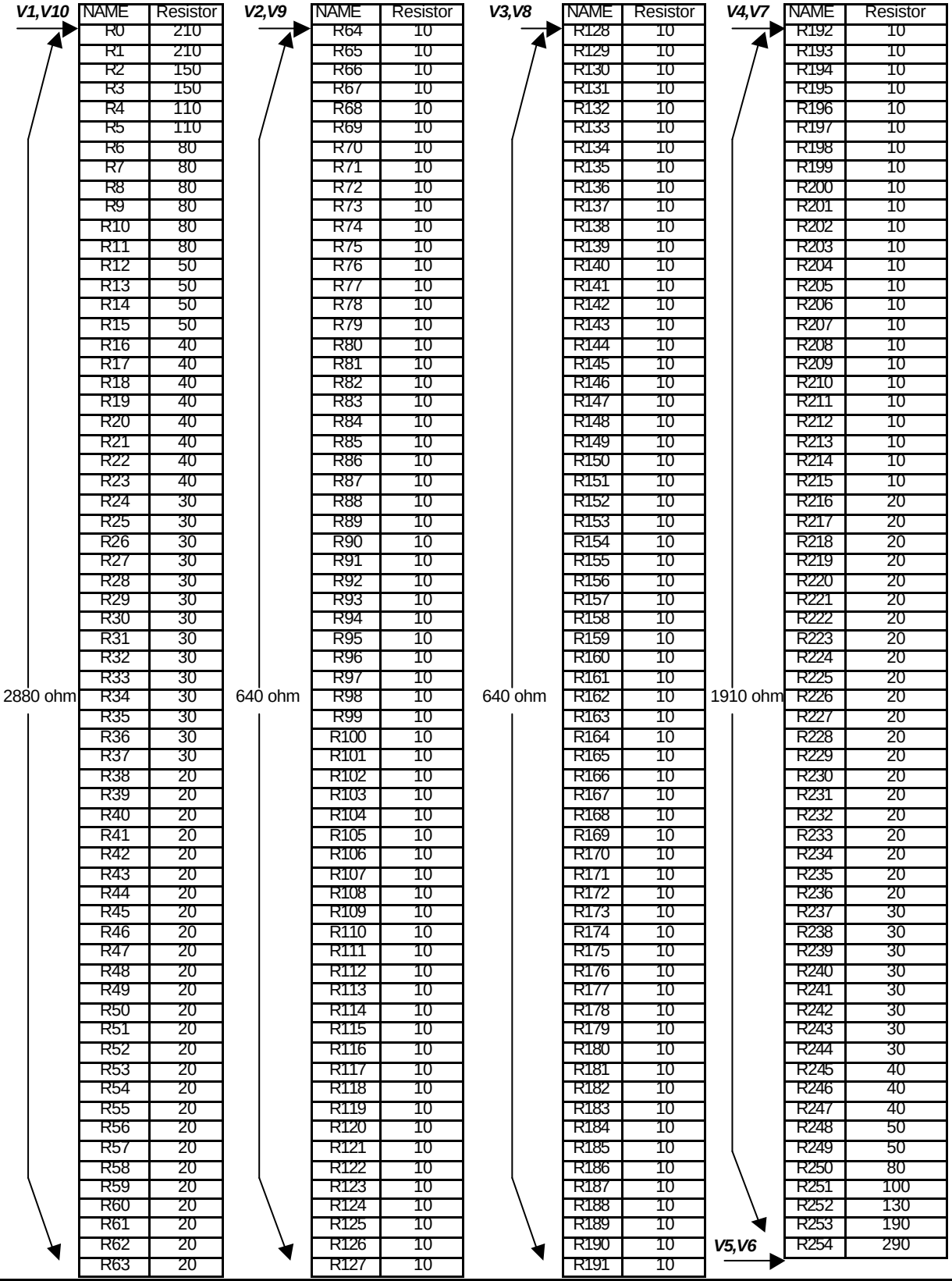
Relationship between input data and output voltage
The figure below shows the relationship among the input data and the output voltage and the polarity. The range of V1~V5 is for positive polarity, and V6 ~ V10 for negative polarity. Please refer to the following page to get the relative resistors value and voltage calculation method.

Gamma correction diagram



Remark : AVDD-0.1>V1>V2>V3>V4>V5>AVDD/2; AVDD/2>V6>V7>V8>V9>V10>0.1

Gamma correction resistor



NAME	Resistor
R0	210
R1	210
R2	150
R3	150
R4	110
R5	110
R6	80
R7	80
R8	80
R9	80
R10	80
R11	80
R12	50
R13	50
R14	50
R15	50
R16	40
R17	40
R18	40
R19	40
R20	40
R21	40
R22	40
R23	40
R24	30
R25	30
R26	30
R27	30
R28	30
R29	30
R30	30
R31	30
R32	30
R33	30
R34	30
R35	30
R36	30
R37	30
R38	20
R39	20
R40	20
R41	20
R42	20
R43	20
R44	20
R45	20
R46	20
R47	20
R48	20
R49	20
R50	20
R51	20
R52	20
R53	20
R54	20
R55	20
R56	20
R57	20
R58	20
R59	20
R60	20
R61	20
R62	20
R63	20

NAME	Resistor
R64	10
R65	10
R66	10
R67	10
R68	10
R69	10
R70	10
R71	10
R72	10
R73	10
R74	10
R75	10
R76	10
R77	10
R78	10
R79	10
R80	10
R81	10
R82	10
R83	10
R84	10
R85	10
R86	10
R87	10
R88	10
R89	10
R90	10
R91	10
R92	10
R93	10
R94	10
R95	10
R96	10
R97	10
R98	10
R99	10
R100	10
R101	10
R102	10
R103	10
R104	10
R105	10
R106	10
R107	10
R108	10
R109	10
R110	10
R111	10
R112	10
R113	10
R114	10
R115	10
R116	10
R117	10
R118	10
R119	10
R120	10
R121	10
R122	10
R123	10
R124	10
R125	10
R126	10
R127	10

NAME	Resistor
R128	10
R129	10
R130	10
R131	10
R132	10
R133	10
R134	10
R135	10
R136	10
R137	10
R138	10
R139	10
R140	10
R141	10
R142	10
R143	10
R144	10
R145	10
R146	10
R147	10
R148	10
R149	10
R150	10
R151	10
R152	10
R153	10
R154	10
R155	10
R156	10
R157	10
R158	10
R159	10
R160	10
R161	10
R162	10
R163	10
R164	10
R165	10
R166	10
R167	10
R168	10
R169	10
R170	10
R171	10
R172	10
R173	10
R174	10
R175	10
R176	10
R177	10
R178	10
R179	10
R180	10
R181	10
R182	10
R183	10
R184	10
R185	10
R186	10
R187	10
R188	10
R189	10
R190	10
R191	10

NAME	Resistor
R192	10
R193	10
R194	10
R195	10
R196	10
R197	10
R198	10
R199	10
R200	10
R201	10
R202	10
R203	10
R204	10
R205	10
R206	10
R207	10
R208	10
R209	10
R210	10
R211	10
R212	10
R213	10
R214	10
R215	10
R216	20
R217	20
R218	20
R219	20
R220	20
R221	20
R222	20
R223	20
R224	20
R225	20
R226	20
R227	20
R228	20
R229	20
R230	20
R231	20
R232	20
R233	20
R234	20
R235	20
R236	20
R237	30
R238	30
R239	30
R240	30
R241	30
R242	30
R243	30
R244	30
R245	40
R246	40
R247	40
R248	50
R249	50
R250	80
R251	100
R252	130
R253	190
R254	290

Output Voltage VS Input Data

Data(h)	Positive polarity Output Voltage	Negative polarity Output Voltage
0	V1	V10
1	V2 + (V1 – V2) X 267/288	V10 + (V 9 – V10) X 21/288
2	V2 + (V1 – V2) X 246/288	V10 + (V 9 – V10) X 42/288
3	V2 + (V1 – V2) X 231/288	V10 + (V 9 – V10) X 57/288
4	V2 + (V1 – V2) X 216/288	V10 + (V 9 – V10) X 72/288
5	V2 + (V1 – V2) X 205/288	V10 + (V 9 – V10) X 83/288
6	V2 + (V1 – V2) X 194/288	V10 + (V 9 – V10) X 94/288
7	V2 + (V1 – V2) X 186/288	V10 + (V 9 – V10) X 102/288
8	V2 + (V1 – V2) X 178/288	V10 + (V 9 – V10) X 110/288
9	V2 + (V1 – V2) X 170/288	V10 + (V 9 – V10) X 118/288
10	V2 + (V1 – V2) X 162/288	V10 + (V 9 – V10) X 126/288
11	V2 + (V1 – V2) X 154/288	V10 + (V 9 – V10) X 134/288
12	V2 + (V1 – V2) X 146/288	V10 + (V 9 – V10) X 142/288
13	V2 + (V1 – V2) X 141/288	V10 + (V 9 – V10) X 147/288
14	V2 + (V1 – V2) X 136/288	V10 + (V 9 – V10) X 152/288
15	V2 + (V1 – V2) X 131/288	V10 + (V 9 – V10) X 157/288
16	V2 + (V1 – V2) X 126/288	V10 + (V 9 – V10) X 162/288
17	V2 + (V1 – V2) X 122/288	V10 + (V 9 – V10) X 166/288
18	V2 + (V1 – V2) X 118/288	V10 + (V 9 – V10) X 170/288
19	V2 + (V1 – V2) X 114/288	V10 + (V 9 – V10) X 174/288
20	V2 + (V1 – V2) X 110/288	V10 + (V 9 – V10) X 178/288
21	V2 + (V1 – V2) X 106/288	V10 + (V 9 – V10) X 182/288
22	V2 + (V1 – V2) X 102/288	V10 + (V 9 – V10) X 186/288
23	V2 + (V1 – V2) X 98/288	V10 + (V 9 – V10) X 190/288
24	V2 + (V1 – V2) X 94/288	V10 + (V 9 – V10) X 194/288
25	V2 + (V1 – V2) X 91/288	V10 + (V 9 – V10) X 197/288
26	V2 + (V1 – V2) X 88/288	V10 + (V 9 – V10) X 200/288
27	V2 + (V1 – V2) X 85/288	V10 + (V 9 – V10) X 203/288
28	V2 + (V1 – V2) X 82/288	V10 + (V 9 – V10) X 206/288
29	V2 + (V1 – V2) X 79/288	V10 + (V 9 – V10) X 209/288
30	V2 + (V1 – V2) X 76/288	V10 + (V 9 – V10) X 212/288
31	V2 + (V1 – V2) X 73/288	V10 + (V 9 – V10) X 215/288
32	V2 + (V1 – V2) X 70/288	V10 + (V 9 – V10) X 218/288
33	V2 + (V1 – V2) X 67/288	V10 + (V 9 – V10) X 221/288
34	V2 + (V1 – V2) X 64/288	V10 + (V 9 – V10) X 224/288
35	V2 + (V1 – V2) X 61/288	V10 + (V 9 – V10) X 227/288
36	V2 + (V1 – V2) X 58/288	V10 + (V 9 – V10) X 230/288
37	V2 + (V1 – V2) X 55/288	V10 + (V 9 – V10) X 233/288
38	V2 + (V1 – V2) X 52/288	V10 + (V 9 – V10) X 236/288
39	V2 + (V1 – V2) X 50/288	V10 + (V 9 – V10) X 238/288
40	V2 + (V1 – V2) X 48/288	V10 + (V 9 – V10) X 240/288
41	V2 + (V1 – V2) X 46/288	V10 + (V 9 – V10) X 242/288
42	V2 + (V1 – V2) X 44/288	V10 + (V 9 – V10) X 244/288
43	V2 + (V1 – V2) X 42/288	V10 + (V 9 – V10) X 246/288
44	V2 + (V1 – V2) X 40/288	V10 + (V 9 – V10) X 248/288
45	V2 + (V1 – V2) X 38/288	V10 + (V 9 – V10) X 250/288
46	V2 + (V1 – V2) X 36/288	V10 + (V 9 – V10) X 252/288
47	V2 + (V1 – V2) X 34/288	V10 + (V 9 – V10) X 254/288
48	V2 + (V1 – V2) X 32/288	V10 + (V 9 – V10) X 256/288
49	V2 + (V1 – V2) X 30/288	V10 + (V 9 – V10) X 258/288
50	V2 + (V1 – V2) X 28/288	V10 + (V 9 – V10) X 260/288
51	V2 + (V1 – V2) X 26/288	V10 + (V 9 – V10) X 262/288
52	V2 + (V1 – V2) X 24/288	V10 + (V 9 – V10) X 264/288
53	V2 + (V1 – V2) X 22/288	V10 + (V 9 – V10) X 266/288
54	V2 + (V1 – V2) X 20/288	V10 + (V 9 – V10) X 268/288
55	V2 + (V1 – V2) X 18/288	V10 + (V 9 – V10) X 270/288
56	V2 + (V1 – V2) X 16/288	V10 + (V 9 – V10) X 272/288
57	V2 + (V1 – V2) X 14/288	V10 + (V 9 – V10) X 274/288
58	V2 + (V1 – V2) X 12/288	V10 + (V 9 – V10) X 276/288
59	V2 + (V1 – V2) X 10/288	V10 + (V 9 – V10) X 278/288
60	V2 + (V1 – V2) X 8/288	V10 + (V 9 – V10) X 280/288
61	V2 + (V1 – V2) X 6/288	V10 + (V 9 – V10) X 282/288
62	V2 + (V1 – V2) X 4/288	V10 + (V 9 – V10) X 284/288
63	V2 + (V1 – V2) X 2/288	V10 + (V 9 – V10) X 286/288

Output Voltage VS Input Data

Data(h)	Positive polarity Output Voltage	Negative polarity Output Voltage
64	V2	V9
65	V3+(V2-V3) X 63/64	V9+(V8-V9) X 1/64
66	V3+(V2-V3) X 62/64	V9+(V8-V9) X 2/64
67	V3+(V2-V3) X 61/64	V9+(V8-V9) X 3/64
68	V3+(V2-V3) X 60/64	V9+(V8-V9) X 4/64
69	V3+(V2-V3) X 59/64	V9+(V8-V9) X 5/64
70	V3+(V2-V3) X 58/64	V9+(V8-V9) X 6/64
71	V3+(V2-V3) X 57/64	V9+(V8-V9) X 7/64
72	V3+(V2-V3) X 56/64	V9+(V8-V9) X 8/64
73	V3+(V2-V3) X 55/64	V9+(V8-V9) X 9/64
74	V3+(V2-V3) X 54/64	V9+(V8-V9) X 10/64
75	V3+(V2-V3) X 53/64	V9+(V8-V9) X 11/64
76	V3+(V2-V3) X 52/64	V9+(V8-V9) X 12/64
77	V3+(V2-V3) X 51/64	V9+(V8-V9) X 13/64
78	V3+(V2-V3) X 50/64	V9+(V8-V9) X 14/64
79	V3+(V2-V3) X 49/64	V9+(V8-V9) X 15/64
80	V3+(V2-V3) X 48/64	V9+(V8-V9) X 16/64
81	V3+(V2-V3) X 47/64	V9+(V8-V9) X 17/64
82	V3+(V2-V3) X 46/64	V9+(V8-V9) X 18/64
83	V3+(V2-V3) X 45/64	V9+(V8-V9) X 19/64
84	V3+(V2-V3) X 44/64	V9+(V8-V9) X 20/64
85	V3+(V2-V3) X 43/64	V9+(V8-V9) X 21/64
86	V3+(V2-V3) X 42/64	V9+(V8-V9) X 22/64
87	V3+(V2-V3) X 41/64	V9+(V8-V9) X 23/64
88	V3+(V2-V3) X 40/64	V9+(V8-V9) X 24/64
89	V3+(V2-V3) X 39/64	V9+(V8-V9) X 25/64
90	V3+(V2-V3) X 38/64	V9+(V8-V9) X 26/64
91	V3+(V2-V3) X 37/64	V9+(V8-V9) X 27/64
92	V3+(V2-V3) X 36/64	V9+(V8-V9) X 28/64
93	V3+(V2-V3) X 35/64	V9+(V8-V9) X 29/64
94	V3+(V2-V3) X 34/64	V9+(V8-V9) X 30/64
95	V3+(V2-V3) X 33/64	V9+(V8-V9) X 31/64
96	V3+(V2-V3) X 32/64	V9+(V8-V9) X 32/64
97	V3+(V2-V3) X 31/64	V9+(V8-V9) X 33/64
98	V3+(V2-V3) X 30/64	V9+(V8-V9) X 34/64
99	V3+(V2-V3) X 29/64	V9+(V8-V9) X 35/64
100	V3+(V2-V3) X 28/64	V9+(V8-V9) X 36/64
101	V3+(V2-V3) X 27/64	V9+(V8-V9) X 37/64
102	V3+(V2-V3) X 26/64	V9+(V8-V9) X 38/64
103	V3+(V2-V3) X 25/64	V9+(V8-V9) X 39/64
104	V3+(V2-V3) X 24/64	V9+(V8-V9) X 40/64
105	V3+(V2-V3) X 23/64	V9+(V8-V9) X 41/64
106	V3+(V2-V3) X 22/64	V9+(V8-V9) X 42/64
107	V3+(V2-V3) X 21/64	V9+(V8-V9) X 43/64
108	V3+(V2-V3) X 20/64	V9+(V8-V9) X 44/64
109	V3+(V2-V3) X 19/64	V9+(V8-V9) X 45/64
110	V3+(V2-V3) X 18/64	V9+(V8-V9) X 46/64
111	V3+(V2-V3) X 17/64	V9+(V8-V9) X 47/64
112	V3+(V2-V3) X 16/64	V9+(V8-V9) X 48/64
113	V3+(V2-V3) X 15/64	V9+(V8-V9) X 49/64
114	V3+(V2-V3) X 14/64	V9+(V8-V9) X 50/64
115	V3+(V2-V3) X 13/64	V9+(V8-V9) X 51/64
116	V3+(V2-V3) X 12/64	V9+(V8-V9) X 52/64
117	V3+(V2-V3) X 11/64	V9+(V8-V9) X 53/64
118	V3+(V2-V3) X 10/64	V9+(V8-V9) X 54/64
119	V3+(V2-V3) X 9/64	V9+(V8-V9) X 55/64
120	V3+(V2-V3) X 8/64	V9+(V8-V9) X 56/64
121	V3+(V2-V3) X 7/64	V9+(V8-V9) X 57/64
122	V3+(V2-V3) X 6/64	V9+(V8-V9) X 58/64
123	V3+(V2-V3) X 5/64	V9+(V8-V9) X 59/64
124	V3+(V2-V3) X 4/64	V9+(V8-V9) X 60/64
125	V3+(V2-V3) X 3/64	V9+(V8-V9) X 61/64
126	V3+(V2-V3) X 2/64	V9+(V8-V9) X 62/64
127	V3+(V2-V3) X 1/64	V9+(V8-V9) X 63/64

Output Voltage VS Input Data

Data(h)	Positive polarity Output Voltage	Negative polarity Output Voltage
128	V3	V8
129	V4+(V3-V4) X 63/64	V8+(V7-V8) X 1/64
130	V4+(V3-V4) X 62/64	V8+(V7-V8) X 2/64
131	V4+(V3-V4) X 61/64	V8+(V7-V8) X 3/64
132	V4+(V3-V4) X 60/64	V8+(V7-V8) X 4/64
133	V4+(V3-V4) X 59/64	V8+(V7-V8) X 5/64
134	V4+(V3-V4) X 58/64	V8+(V7-V8) X 6/64
135	V4+(V3-V4) X 57/64	V8+(V7-V8) X 7/64
136	V4+(V3-V4) X 56/64	V8+(V7-V8) X 8/64
137	V4+(V3-V4) X 55/64	V8+(V7-V8) X 9/64
138	V4+(V3-V4) X 54/64	V8+(V7-V8) X 10/64
139	V4+(V3-V4) X 53/64	V8+(V7-V8) X 11/64
140	V4+(V3-V4) X 52/64	V8+(V7-V8) X 12/64
141	V4+(V3-V4) X 51/64	V8+(V7-V8) X 13/64
142	V4+(V3-V4) X 50/64	V8+(V7-V8) X 14/64
143	V4+(V3-V4) X 49/64	V8+(V7-V8) X 15/64
144	V4+(V3-V4) X 48/64	V8+(V7-V8) X 16/64
145	V4+(V3-V4) X 47/64	V8+(V7-V8) X 17/64
146	V4+(V3-V4) X 46/64	V8+(V7-V8) X 18/64
147	V4+(V3-V4) X 45/64	V8+(V7-V8) X 19/64
148	V4+(V3-V4) X 44/64	V8+(V7-V8) X 20/64
149	V4+(V3-V4) X 43/64	V8+(V7-V8) X 21/64
150	V4+(V3-V4) X 42/64	V8+(V7-V8) X 22/64
151	V4+(V3-V4) X 41/64	V8+(V7-V8) X 23/64
152	V4+(V3-V4) X 40/64	V8+(V7-V8) X 24/64
153	V4+(V3-V4) X 39/64	V8+(V7-V8) X 25/64
154	V4+(V3-V4) X 38/64	V8+(V7-V8) X 26/64
155	V4+(V3-V4) X 37/64	V8+(V7-V8) X 27/64
156	V4+(V3-V4) X 36/64	V8+(V7-V8) X 28/64
157	V4+(V3-V4) X 35/64	V8+(V7-V8) X 29/64
158	V4+(V3-V4) X 34/64	V8+(V7-V8) X 30/64
159	V4+(V3-V4) X 33/64	V8+(V7-V8) X 31/64
160	V4+(V3-V4) X 32/64	V8+(V7-V8) X 32/64
161	V4+(V3-V4) X 31/64	V8+(V7-V8) X 33/64
162	V4+(V3-V4) X 30/64	V8+(V7-V8) X 34/64
163	V4+(V3-V4) X 29/64	V8+(V7-V8) X 35/64
164	V4+(V3-V4) X 28/64	V8+(V7-V8) X 36/64
165	V4+(V3-V4) X 27/64	V8+(V7-V8) X 37/64
166	V4+(V3-V4) X 26/64	V8+(V7-V8) X 38/64
167	V4+(V3-V4) X 25/64	V8+(V7-V8) X 39/64
168	V4+(V3-V4) X 24/64	V8+(V7-V8) X 40/64
169	V4+(V3-V4) X 23/64	V8+(V7-V8) X 41/64
170	V4+(V3-V4) X 22/64	V8+(V7-V8) X 42/64
171	V4+(V3-V4) X 21/64	V8+(V7-V8) X 43/64
172	V4+(V3-V4) X 20/64	V8+(V7-V8) X 44/64
173	V4+(V3-V4) X 19/64	V8+(V7-V8) X 45/64
174	V4+(V3-V4) X 18/64	V8+(V7-V8) X 46/64
175	V4+(V3-V4) X 17/64	V8+(V7-V8) X 47/64
176	V4+(V3-V4) X 16/64	V8+(V7-V8) X 48/64
177	V4+(V3-V4) X 15/64	V8+(V7-V8) X 49/64
178	V4+(V3-V4) X 14/64	V8+(V7-V8) X 50/64
179	V4+(V3-V4) X 13/64	V8+(V7-V8) X 51/64
180	V4+(V3-V4) X 12/64	V8+(V7-V8) X 52/64
181	V4+(V3-V4) X 11/64	V8+(V7-V8) X 53/64
182	V4+(V3-V4) X 10/64	V8+(V7-V8) X 54/64
183	V4+(V3-V4) X 9/64	V8+(V7-V8) X 55/64
184	V4+(V3-V4) X 8/64	V8+(V7-V8) X 56/64
185	V4+(V3-V4) X 7/64	V8+(V7-V8) X 57/64
186	V4+(V3-V4) X 6/64	V8+(V7-V8) X 58/64
187	V4+(V3-V4) X 5/64	V8+(V7-V8) X 59/64
188	V4+(V3-V4) X 4/64	V8+(V7-V8) X 60/64
189	V4+(V3-V4) X 3/64	V8+(V7-V8) X 61/64
190	V4+(V3-V4) X 2/64	V8+(V7-V8) X 62/64
191	V4+(V3-V4) X 1/64	V8+(V7-V8) X 63/64

Output Voltage VS Input Data

Data(h)	Positive polarity Output Voltage	Negative polarity Output Voltage
192	V4	V7
193	V5+(V4-V5) X 190/191	V7+(V6-V7) X 1/191
194	V5+(V4-V5) X 189/191	V7+(V6-V7) X 2/191
195	V5+(V4-V5) X 188/191	V7+(V6-V7) X 3/191
196	V5+(V4-V5) X 187/191	V7+(V6-V7) X 4/191
197	V5+(V4-V5) X 186/191	V7+(V6-V7) X 5/191
198	V5+(V4-V5) X 185/191	V7+(V6-V7) X 6/191
199	V5+(V4-V5) X 184/191	V7+(V6-V7) X 7/191
200	V5+(V4-V5) X 183/191	V7+(V6-V7) X 8/191
201	V5+(V4-V5) X 182/191	V7+(V6-V7) X 9/191
202	V5+(V4-V5) X 181/191	V7+(V6-V7) X 10/191
203	V5+(V4-V5) X 180/191	V7+(V6-V7) X 11/191
204	V5+(V4-V5) X 179/191	V7+(V6-V7) X 12/191
205	V5+(V4-V5) X 178/191	V7+(V6-V7) X 13/191
206	V5+(V4-V5) X 177/191	V7+(V6-V7) X 14/191
207	V5+(V4-V5) X 176/191	V7+(V6-V7) X 15/191
208	V5+(V4-V5) X 175/191	V7+(V6-V7) X 16/191
209	V5+(V4-V5) X 174/191	V7+(V6-V7) X 17/191
210	V5+(V4-V5) X 173/191	V7+(V6-V7) X 18/191
211	V5+(V4-V5) X 172/191	V7+(V6-V7) X 19/191
212	V5+(V4-V5) X 171/191	V7+(V6-V7) X 20/191
213	V5+(V4-V5) X 170/191	V7+(V6-V7) X 21/191
214	V5+(V4-V5) X 169/191	V7+(V6-V7) X 22/191
215	V5+(V4-V5) X 168/191	V7+(V6-V7) X 23/191
216	V5+(V4-V5) X 167/191	V7+(V6-V7) X 24/191
217	V5+(V4-V5) X 165/191	V7+(V6-V7) X 26/191
218	V5+(V4-V5) X 163/191	V7+(V6-V7) X 28/191
219	V5+(V4-V5) X 161/191	V7+(V6-V7) X 30/191
220	V5+(V4-V5) X 159/191	V7+(V6-V7) X 32/191
221	V5+(V4-V5) X 157/191	V7+(V6-V7) X 34/191
222	V5+(V4-V5) X 155/191	V7+(V6-V7) X 36/191
223	V5+(V4-V5) X 153/191	V7+(V6-V7) X 38/191
224	V5+(V4-V5) X 151/191	V7+(V6-V7) X 40/191
225	V5+(V4-V5) X 149/191	V7+(V6-V7) X 42/191
226	V5+(V4-V5) X 147/191	V7+(V6-V7) X 44/191
227	V5+(V4-V5) X 145/191	V7+(V6-V7) X 46/191
228	V5+(V4-V5) X 143/191	V7+(V6-V7) X 48/191
229	V5+(V4-V5) X 141/191	V7+(V6-V7) X 50/191
230	V5+(V4-V5) X 139/191	V7+(V6-V7) X 52/191
231	V5+(V4-V5) X 137/191	V7+(V6-V7) X 54/191
232	V5+(V4-V5) X 135/191	V7+(V6-V7) X 56/191
233	V5+(V4-V5) X 133/191	V7+(V6-V7) X 58/191
234	V5+(V4-V5) X 131/191	V7+(V6-V7) X 60/191
235	V5+(V4-V5) X 129/191	V7+(V6-V7) X 62/191
236	V5+(V4-V5) X 127/191	V7+(V6-V7) X 64/191
237	V5+(V4-V5) X 125/191	V7+(V6-V7) X 66/191
238	V5+(V4-V5) X 122/191	V7+(V6-V7) X 69/191
239	V5+(V4-V5) X 119/191	V7+(V6-V7) X 72/191
240	V5+(V4-V5) X 116/191	V7+(V6-V7) X 75/191
241	V5+(V4-V5) X 113/191	V7+(V6-V7) X 78/191
242	V5+(V4-V5) X 110/191	V7+(V6-V7) X 81/191
243	V5+(V4-V5) X 107/191	V7+(V6-V7) X 84/191
244	V5+(V4-V5) X 104/191	V7+(V6-V7) X 87/191
245	V5+(V4-V5) X 101/191	V7+(V6-V7) X 90/191
246	V5+(V4-V5) X 97/191	V7+(V6-V7) X 94/191
247	V5+(V4-V5) X 93/191	V7+(V6-V7) X 98/191
248	V5+(V4-V5) X 89/191	V7+(V6-V7) X 102/191
249	V5+(V4-V5) X 84/191	V7+(V6-V7) X 107/191
250	V5+(V4-V5) X 79/191	V7+(V6-V7) X 112/191
251	V5+(V4-V5) X 71/191	V7+(V6-V7) X 120/191
252	V5+(V4-V5) X 61/191	V7+(V6-V7) X 130/191
253	V5+(V4-V5) X 48/191	V7+(V6-V7) X 143/191
254	V5+(V4-V5) X 29/191	V7+(V6-V7) X 162/191
255	V5	V6

Absolute Maximum Ratings*

Supply voltage, Vcc	-0.3V to 5V
Supply voltage, AVDD	-0.3V to +12V
Input voltage, V1~ V10	-0.3 to AVDD+0.3
Input range(digital inputs)	-0.3 to Vcc+0.3
Storage temperature	-55°C to 110°C
Operating temperature	-30°C to 75°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or under any other conditions above those indicated in the operational sections of this specification are not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (V_{CC}=3.3V , AV_{DD}=10V, AVSS=GND=0V, T_A= -30°C~ 75°C)

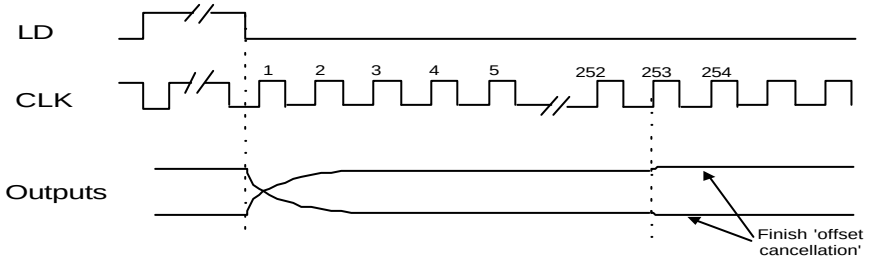
(For the digital circuit)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	Vcc	2.5	--	3.6	V	Digital power
Low Level Input Voltage	Vil	0	-	0.3xVcc	V	For the digital circuit
High Level Input Voltage	Vih	0.7xVcc	-	Vcc	V	For the digital circuit
High Level Output Voltage	Voh	0.7xVcc	-	--	V	DIO1(O), DIO2(O), Ioh=-0.4mA
Low Level Output Voltage	Vol	--	-	0.3Vcc	V	DIO1(O), DIO2(O), Iol=0.4mA
Input Leakage Current	Ii	-1	-	1	µA	For LD,CLK,SHL,Dxx,POL,REV1/2,DIO1/2
Gamma correction Current	Iref	--	800	1000	µA	For V1-V5=4.75V or V6-V10=4.75V
Digital Operating Current	Icc	-	3	6	mA	Vcc=3.6V, AVDD=9.5V,fld=50kHz,fclk=45MHz No load

(For the analog circuit)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	AVDD	7.0	--	10	V	For the analog circuit power
Input level of V1 ~ V5	Vref	AVDD/2	-	AVDD-0.1	V	Gamma correction voltage
Input level of V6 ~ V10	Vref	0.1		AVDD/2	V	Gamma correction voltage
Output Voltage Deviation	Vvd	--	±6	±12	mV	Input data ' without' offset cancellation
		--	±2	±5	mV	Input data ' with' offset cancellation (Note1)
Average output voltage dispersion	Vod	--	±5	±10	mV	OUT1 ~ OUT384,input data 00 to FF.
Dynamic Range of Output	Vdr	0.1	-	AVDD-0.1	V	OUT1 ~ OUT384
Low-Level Output Current	IOL	-150	-300	-	µA	OUT1 ~ OUT384; Vo=0.1V V.S 1.0V
High-Level Output Current	IOH	150	300	-	µA	OUT1 ~ OUT384; Vo=9.9V V.S 9V
Analog Operating Current	IDD	-	6	12	mA	Vcc=3.6V,AVDD=9.5V,fld=50kHz,fclk=45MHz No load
Input capacitance1	C1	--	5	10	pF	For Input pins ,except DIO1,DIO2
Input capacitance2	C2	--	10	15	pF	For DIO1,DIO2

(Note 1) This chip needs 253 CLK cycles to use its 'offset cancellation' function to get a precision output voltage. Please refer to the timing chart below :



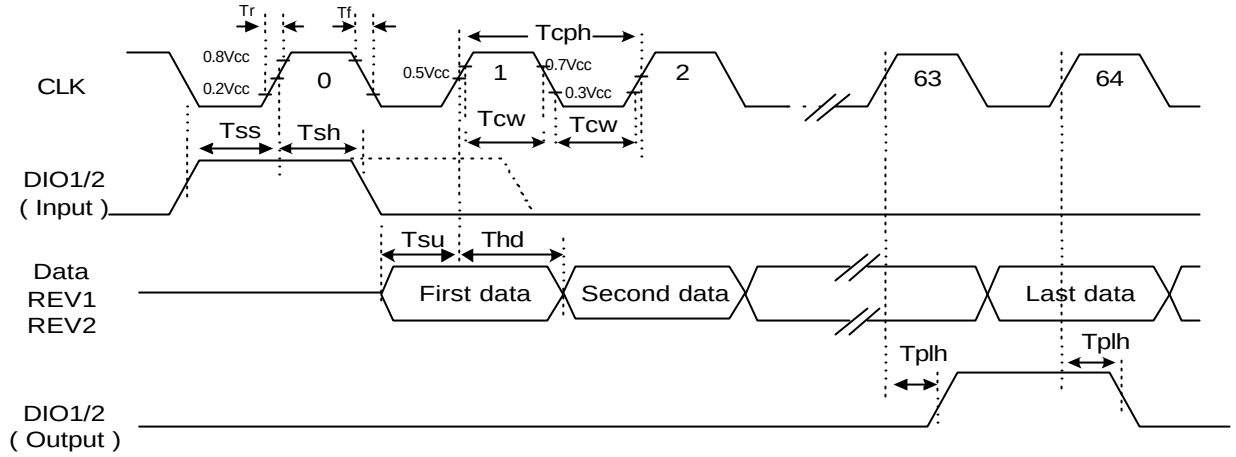
AC Electrical Characteristics 1(V_{CC} =3.0V , AV_{DD}=10V, AVSS=GND=0V, T_A= -30 ~ 75°C,Tr=Tf=2ns)

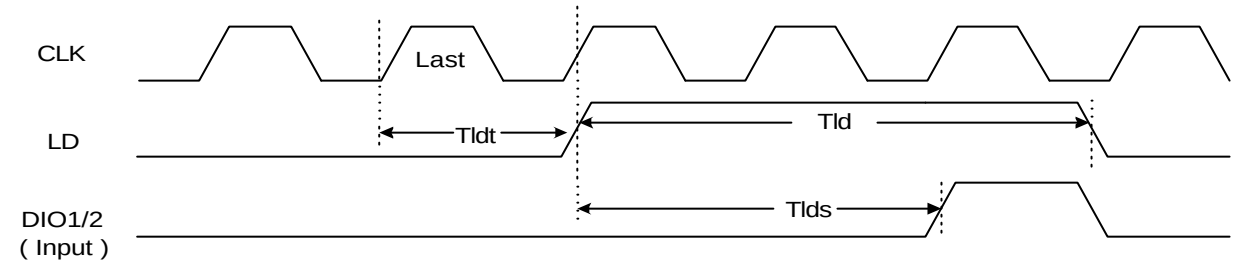
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
CLK frequency	Fclk	-	45	70	MHz	Vcc=3.0~3.6V
CLK period cycle	Tcph	14	-	-	ns	
CLK pulse width	Tcw	4	-	-	ns	
Data set-up time	Tsu	2	-	-	ns	D00 ~ D57, REV to CLK
Data hold time	Thd	2	-	-	ns	D00 ~ D57, REV to CLK
Start pulse setup time	Tss	2	--	--	ns	DIO1,DIO2 to CLK
Start pulse hold time	Tsh	2	--	--	ns	DIO1,DIO2 to CLK
LD high-level width	Tld	1	--	--	us	
Propagation delay of DIO2/1	Tplh	6	--	12	ns	CL=25pF (Output)
Time that the last data to LD	Tldt	1	-	-	Tcph	
Time that LD to DIO1/2(In)	Tlds	2	-	-	Tcph	
POL set-up time	Tpsu	5	-	-	ns	POL to LD
POL hold time	Tphd	5	-	-	ns	POL to LD
Output stable time	Tst	-	4	6	us	Final value precision below 30mV, CL=150pF,R=5k ohm ,AVDD=10V
Slew rate of outputs	Tsr	3	5	-	V/us	5% to 95% at 10V swing, CL=150pF,R=5k ohm
Output loading	CL	-	-	150	pF	

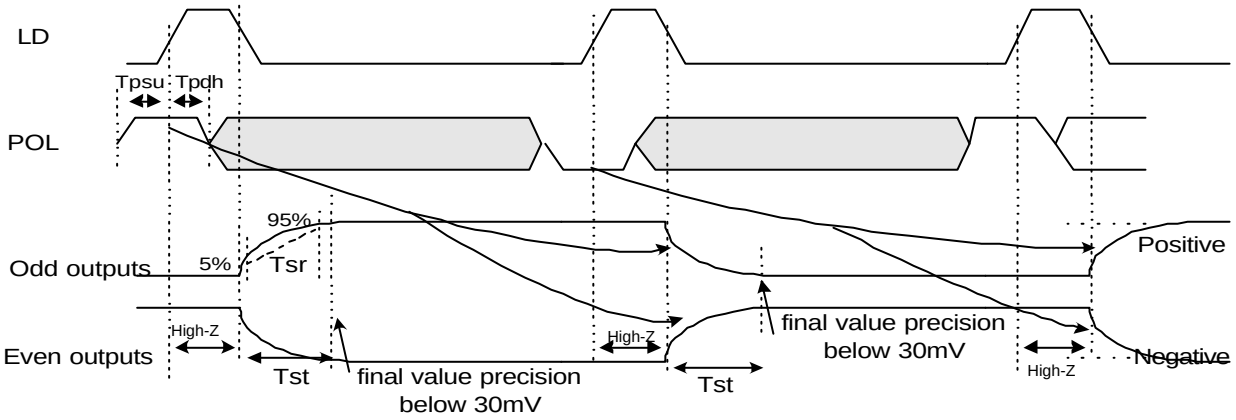
AC Electrical Characteristics 2(V_{CC} =2.5V , AV_{DD}=10V, AVSS=GND=0V, T_A= -30~75°C,Tr=Tf=3ns)

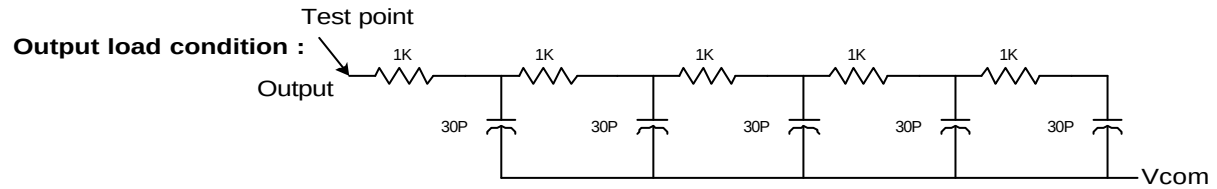
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
CLK frequency	Fclk	-	35	45	MHz	Vcc=2.5~3.0V
CLK period cycle	Tcph	22	-	-	ns	
CLK pulse width	Tcw	7	-	-	ns	
Data set-up time	Tsu	4	-	-	ns	D00 ~ D57, REV to CLK
Data hold time	Thd	4	-	-	ns	D00 ~ D57, REV to CLK
Start pulse setup time	Tss	4	--	--	ns	DIO1,DIO2 to CLK
Start pulse hold time	Tsh	4	--	--	ns	DIO1,DIO2 to CLK
LD high-level width	Tld	1	--	--	us	
Propagation delay of DIO2/1	Tplh	6	--	18	ns	CL=25pF (Output)
Time that the last data to LD	Tldt	1	-	-	Tcph	
Time that LD to DIO1/2(In)	Tlds	2	-	-	Tcph	
POL set-up time	Tpsu	5	-	-	ns	POL to LD
POL hold time	Tphd	5	-	-	ns	POL to LD
Output stable time	Tst	-	4	6	us	Final value precision below 30mV, CL=150pF,R=5k ohm ,AVDD=10V
Slew rate of outputs	Tsr	3	5	-	V/us	5% to 95% at 10V swing, CL=150pF,R=5k ohm
Output loading	CL	-	-	150	pF	

Timing Diagram









Function operation