DIGITAL VERTICAL FILTER (DVF)

GENERAL DESCRIPTION

The SAA9069 is a digital vertical line filter for use in picture-in-picture applications. The DVF accomplishes the filtering by computing the average of three horizontal video lines. The summation is carried out in the following order, 1/4 x line 1, 1/2 x line 2 and 1/4 x line 3. The DVF outputs the averaged information during the third line period. The 5-bit data is multiplied by a weighting factor and added to the output of the 201-bit long, 6-bit wide shift register which is used as a line memory to store input data or the averaged data. The most significant 5-bits are output as filtered data. The DVF has been designed for use with the Picture-in-Picture Controller (SAA9068) in digital or analogue televisions.

Features

- 201-bit shift register for storage of input data or the averaged data
- Most significant 5-bits are output as filtered data

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_{DD}	−0,5	–	7,0	V
Input voltage range		V_I	−0,5	–	V_{DD}+0,5	V
Maximum input current		I_{IM}	–	–	±10	μA
Maximum output current		I_{OM}	–	–	±10	μA
Inputs						
Input voltage LOW		V_{IL}	0	–	0,8	V
Input voltage HIGH		V_{IH}	2,0	–	V_{DD}	V
Outputs						
Output voltage LOW	I_{OL} = 2,0 mA	V_{OL}	0	–	0,4	V
Output voltage HIGH	I_{OH} = 1,5 mA	V_{OH}	V_{DD}−0,4	–	V_{DD}	V

PACKAGE OUTLINE

20-lead mini-pack; plastic (SO20; SOT163A)

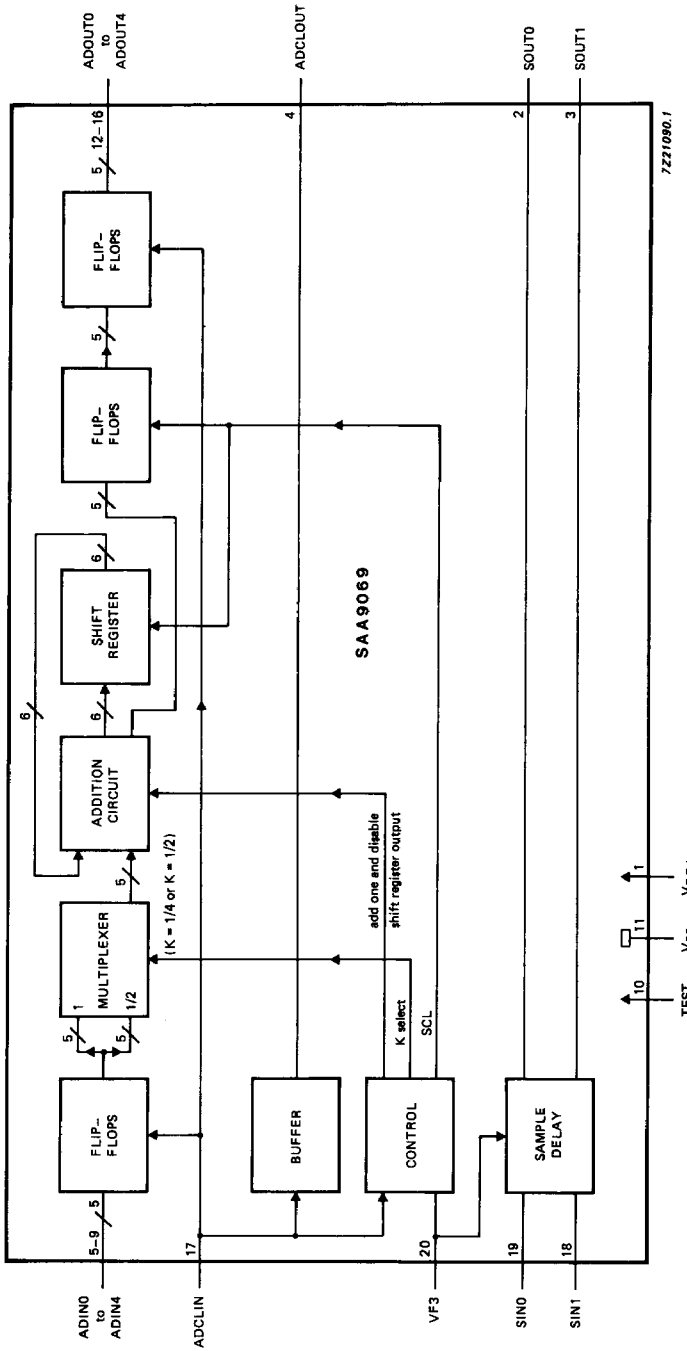

Fig. 1. Block diagram.

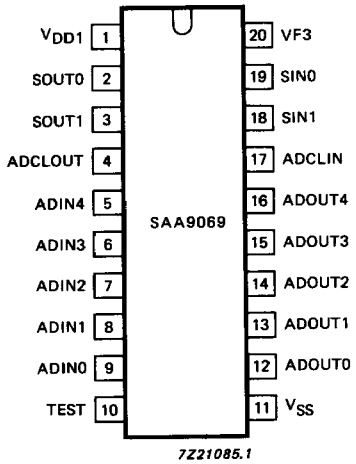

Fig. 2 Pinning diagram.

DEVELOPMENT DATA

PINNING

Power supplies

1	V_{DD1}	positive supply voltage
10	TEST	test pin; normally connected to ground
11	V_{SS}	ground (0 V)

Inputs

5 to 9	ADIN4 to ADIN0	5-bit input data from ADC (timing information shown in Fig. 4)
17	ADCLIN	clock signal from SAA9068. The signal is buffered and then fed directly to the clock input of the ADC
18 to 19	SIN1 to SIN0	control signals for analogue multiplexer from SAA9068. Delayed by 2 and 1 ADCL clock pulses, these signals are inverted and then fed to the analogue multiplexer
20	VF3	signal from SAA9068 (at line rate) used to determine the K-factor, addition sequence and provide a general reset (see Fig. 6)

Outputs

2 to 3	SOUT0 to SOUT1	regenerated SIN0 and SIN1 signals used for proper data selection (due to delay of the DVF)
4	ADCLOUT	buffered output of ADCL
12 to 16	ADOUT0 to ADOUT4	filtered 5-bit data output. Data is only valid on one of the three lines (determined by VF3)

FUNCTIONAL DESCRIPTION (see Figs 1 and 3 to 7)

The main functions of the DVF are as follows:

Multiplexing/Multiplying

The incoming 5-bit data from the ADC is clocked through a block of flip-flops and then fed to a multiplexer/multiplier where line 1 is shifted 1-bit to right (K = 1/4), line 2 is unshifted (K = 1/2) and line 3 is shifted 1-bit to right (K = 1/4). The multiplexer is controlled by a signal derived from the VF3 signal. This creates a 5-bit signal which is retained during the filtering process.

Addition

The data is then added, with 6-bits of resolution, to the output of the shift register to form the new averaged data. This data is then fed to the 6-bit shift register (the first line has a binary 1 added, which is used as a rounding factor). The 5 most significant bits of data are output to two blocks of flip-flops. The first block provides the synchronization with the shift register clock and the second block with the output clock.

Synchronization

The ADCL clock and the analogue selection control signals are received from SAA9068. These signals ensure the synchronous operation between the two devices. Whether the EDVF is used or not the phase relationship between these signals always remains the same. The buffered ADCL clock signal is used as the shift register clock, while S1 and S0 are delayed in order to derive the proper data stream from the ADC. The required ADC characteristics are shown in Fig. 5.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage range		V_{DD}	−0,5	7,0	V
Input voltage range	note 1	V_I	−0,5	V_{DD}+0,5	V
Input voltage	pin 19	V_{19-11}	−0,5	9	V
Maximum input current		I_{IM}	−	±10	mA
Maximum output current		I_{OM}	−	±10	mA
Maximum supply current in V_{SS}		I_{SS}	−	60	mA
Maximum supply current in V_{DD}		I_{DD}	−	60	mA
Maximum power dissipation per output		P	−	40	mW
Total power dissipation		P_{tot}	−	300	mW
Storage temperature range		T_{stg}	−55	+150	°C

Note

1. Input voltage should not exceed 7 V unless otherwise specified.

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HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

DC CHARACTERISTICS

V_{DD} = 5 V ± 10%; T_{amb} = 0 to 70 °C, unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply current						
Quiescent current	T_{amb} = 25 °C; all inputs to V_{DD} or V_{SS}	I_{DD}	–	–	10	μA
Inputs	all inputs					
Input voltage LOW		V_{IL}	0	–	0,8	V
Input voltage HIGH		V_{IH}	2,0	–	V_{DD}	V
Input leakage current LOW		I_{IL}	–	–	1,0	μA
Input leakage current HIGH		I_{IH}	–	–	1,0	μA
Outputs	all outputs					
Output voltage LOW	I_{OL} = –2,0 mA	V_{OL}	0	–	0,4	V
Output voltage HIGH	I_{OH} = +1,5 mA	V_{OH}	V_{DD}–0,4	–	V_{DD}	V

AC CHARACTERISTICS

V_{DD} = 5 V ± 10%; T_{amb} = 0 to 70 °C, unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Inputs	all inputs; except ADCLIN					
Input capacitance		C_I	–	–	7,5	pF
Set-up time	see Fig. 4	t_{SU}	30	–	–	ns
Hold time		t_{HD}	10	–	–	ns
ADCLIN						
Pulse frequency		f_{max}	–	5,33	–	MHz
Pulse width LOW		t_{WL}	45	–	–	ns
Pulse width HIGH		t_{WH}	65	–	–	ns
Outputs	all outputs; except ADCLOUT					
Propagation delay		t_{OD}	–	–	50	ns
Output hold		t_{OH}	0	–	–	ns
ADCLOUT						
Propagation delay	see Fig. 3	t_{OD}	–	–	30	ns

TIMING INFORMATION

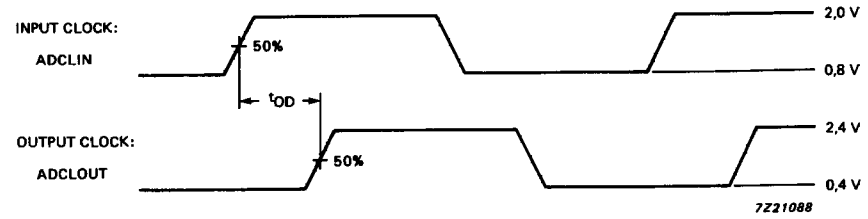

Fig. 3 Input and output clock signal phase relationship.

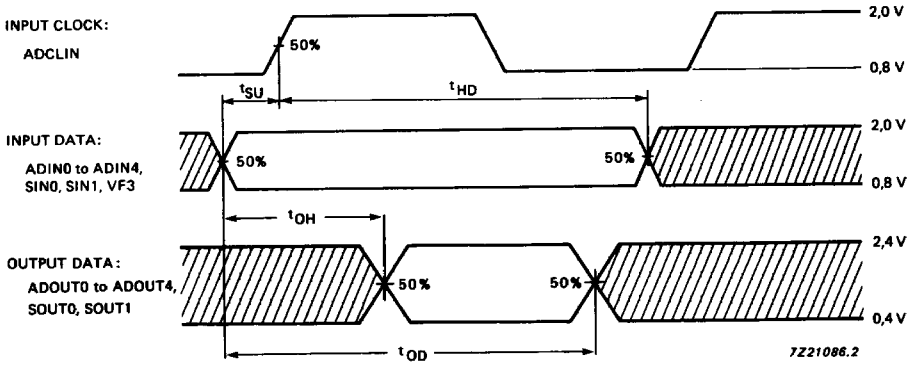

Fig. 4 Input and output data phase relationship.

DEVELOPMENT DATA

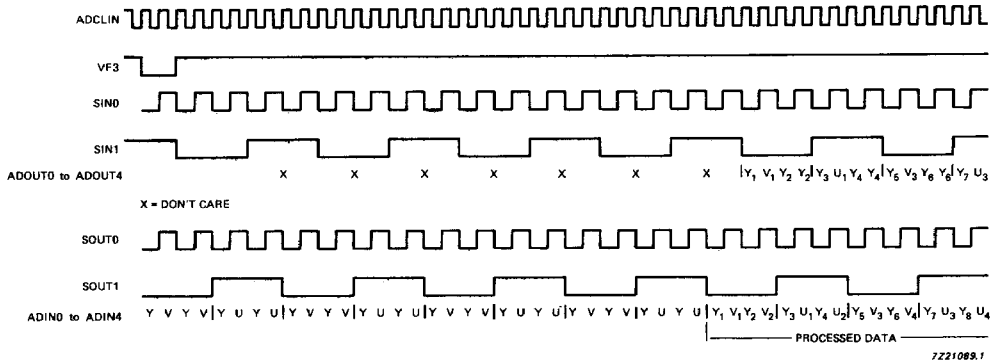

Fig. 5 Timing diagram.

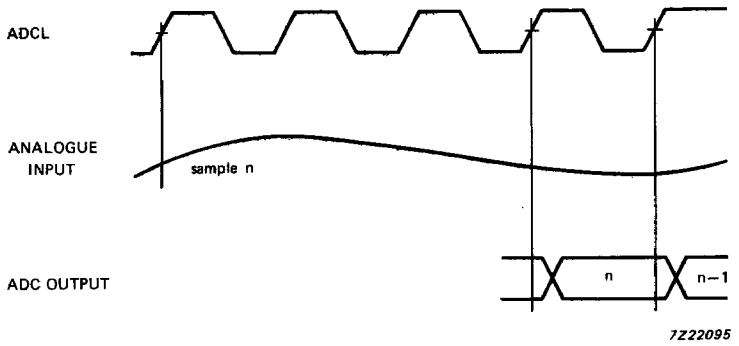

Fig. 6 ADC required.

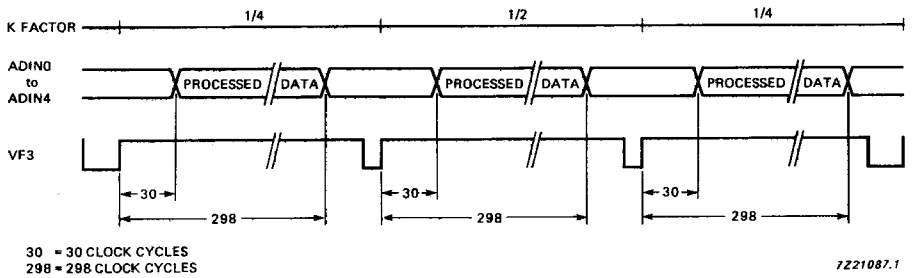

Fig. 7 Clock cycle diagram.