PLESSEY
Semiconductors

# SP8695A&B

## 200MHz ÷ 10/11

The SP8695 is a low power ECL counter with both ECL 10K and TTL compatible outputs. They divide by 10 when either control input in the 'high' state and by 11 when both are 'low' (or open circuit). The inputs are ECL II compatible but can also be AC coupled. An open collector output is provided for interfacing to TTL or CMOS.

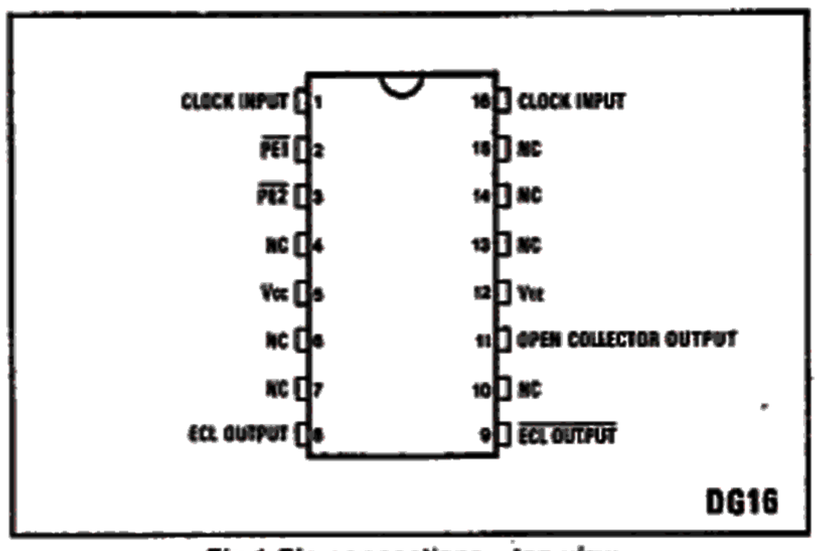



*Fig.1 Pin connections - top view*

### FEATURES

- Low Frequency Operation
- ECL and TTL/CMOS Outputs
- DC or AC Coupled Input
- Temperature Ranges:
  - A Grade: -55°C to +125°C
  - B Grade: -30°C to +70°C

### QUICK REFERENCE DATA

- Supply Voltage: +5.0V
- Power Consumption: 80mW
- Maximum Input Frequency: 200MHz

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply voltage | -8V |
| Output ECL current | 10mA |
| Storage temperature range | -55°C to +150°C |
| Max. junction temperature | +175°C |
| Max. input voltage | 2.5V p-p |
| Max. open collector output voltage | +12V |
| Max. open collector current | 15mA |

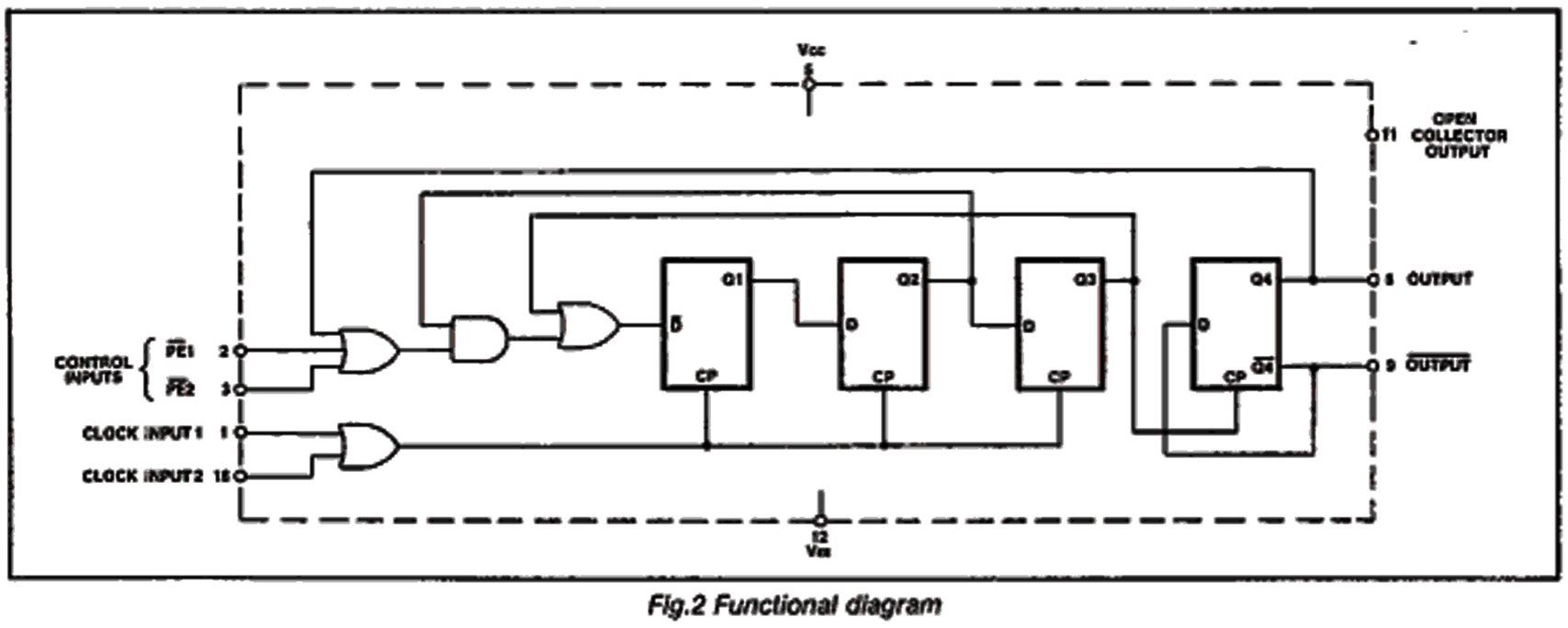



*Fig.2 Functional diagram*

## ELECTRICAL CHARACTERISTICS

### ECL OPERATION

Supply Voltage: $V_{EE}$ = -5.2V ± 0.25V $V_{CC}$ = 0V
Temperature: A grade $T_{amb}$ = -55°C to +125°C
B grade: $T_{amb}$ = -30°C to +70°C

| Characteristics | Symbol | Value | | Units | Conditions | Temperature |
|---|---|---|---|---|---|---|
| | | Min. | Max. | | | |
| Maximum frequency sinewave input | $f_{max}$ | 200 | | MHz | Input = 400-800mV p-p | Note 3 |
| Minimum frequency sinewave input | $f_{min}$ | | 2 | MHz | Input = 400-800mV | Note 4 |
| Power supply current | $I_{EE}$ | | 21 | mA | $V_{EE}$ = -5.0V | Note 3 |
| ECL output low voltage | $V_{OH}$ | -0.85 | -0.7 | V | $V_{EE}$ = -5.2V (25°C) | |
| ECL output high voltage | $V_{OL}$ | -1.8 | -1.5 | V | $V_{EE}$ = -5.2V (25°C) | |
| $\overline{PE}$ input high voltage | $V_{INH}$ | -0.93 | | V | $V_{EE}$ = -5.2V (25°C) | |
| $\overline{PE}$ input low voltage | $V_{INL}$ | | -1.62 | V | $V_{EE}$ = -5.2V (25°C) | |
| Clock to ECL output delay | $t_p$ | | 9 | ns | | Note 4 |
| Set-up time | $t_s$ | 3 | | ns | | Note 4 |
| Release time | $t_r$ | 8 | | ns | | Note 4 |

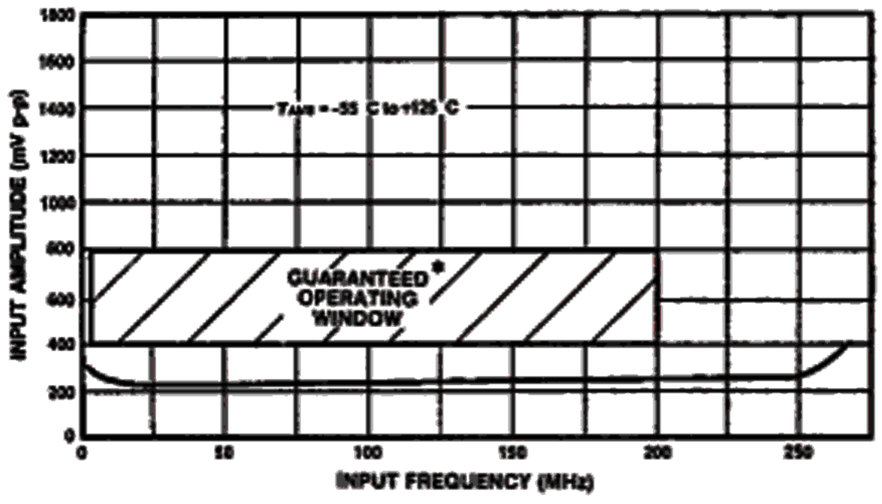
NOTES
1. Unless otherwise stated, the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The temperature coefficient of $V_{OH}$ = +1.63mV/°C, $V_{OL}$ = +0.94mV/°C and of $V_{IN}$ = +1.22mV/°C but these are not tested.
3. SP8695B tested at 25°C only.
4. Guaranteed but not tested.
5. TTL output not recommended for use above 15MHz output frequency. $C_{load} \ll 5pF$.

## ELECTRICAL CHARACTERISTICS

### TTL OPERATION

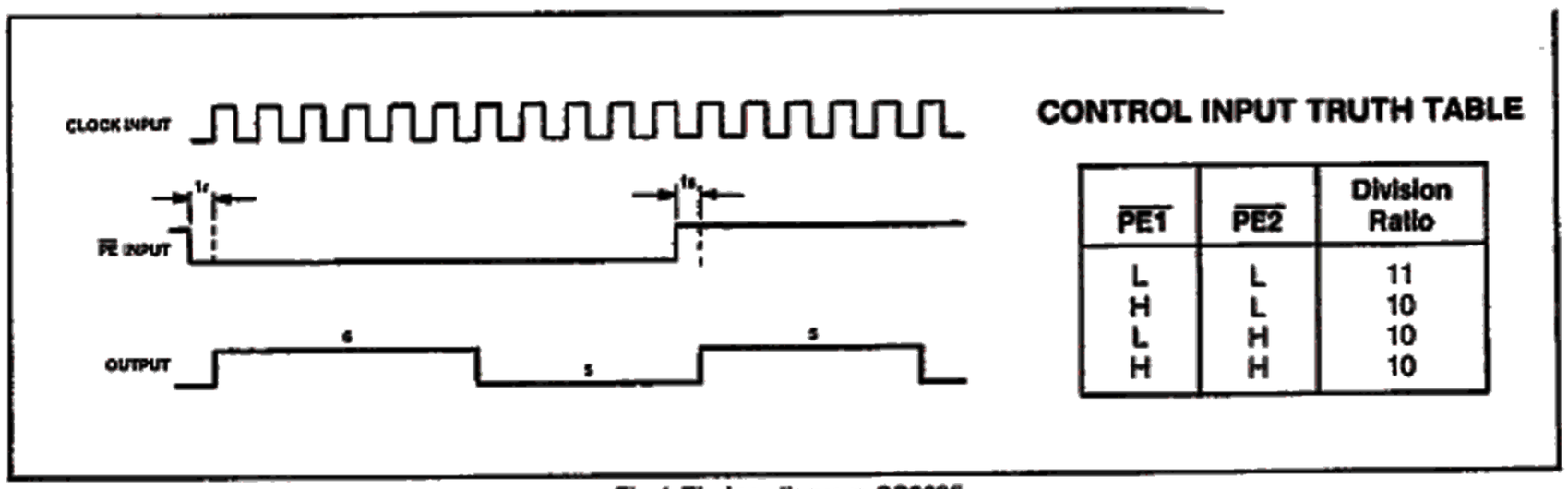
Supply Voltage: $V_{CC}$ = 5.0 ± 0.25V $V_{EE}$ = 0V
Temperature: A grade $T_{amb}$ = -55°C to +125°C
B grade $T_{amb}$ = -30°C to +70°C

| Characteristic | Symbol | Value | | Units | Conditions | Notes |
|---|---|---|---|---|---|---|
| | | Min. | Max. | | | |
| Maximum frequency sinewave input | $f_{max}$ | 200 | | MHz | Input =400 - 800mV p-p | Note 3 |
| Minimum frequency sinewave input | $f_{min}$ | | 2 | MHz | Input =400 - 800mV p-p | Note 4 |
| Power supply current | $I_{EE}$ | | 21 | mA | $V_{CC}$= 5.0V | Note 3 |
| TTL output high voltage | $V_{OH}$ | 3.75 | | V | $V_{CC}$= 5V RL = 560Ω | Note 3, 5 |
| TTL output low voltage | $V_{OL}$ | | 0.5 | V | RL = 560Ω | Note 3 |
| Clock to TTL output delay (positive going) | $t_{pLH}$ | | 32 | ns | RL = 560Ω | Note 4 |
| Clock to TTL output delay (negative going) | $t_{pHL}$ | | 18 | ns | RL = 560Ω | Note 4 |
| Set-up time | $t_s$ | 3 | | ns | | Note 4 |
| Release time | $t_r$ | 8 | | ns | | Note 4 |




*Tested as specified in table of Electrical Characteristics

*Fig.3 Typical input characteristics SP8695A*




**CONTROL INPUT TRUTH TABLE**

| $\overline{PE1}$ | $\overline{PE2}$ | Division Ratio |
|---|---|---|
| L | L | 11 |
| H | L | 10 |
| L | H | 10 |
| H | H | 10 |

*Fig.4 Timing diagram SP8695*

NOTES

The set-up time $t_s$ is defined as minimum time that can elapse between L→H transition of control input and the next L→H clock pulse transition to ensure that the ÷10 mode is obtained.

The release time $t_r$ is defined as the minimum time that can elapse between a H→L transition of control input and the next L→H clock pulse transition to ensure that the ÷11 mode is obtained.

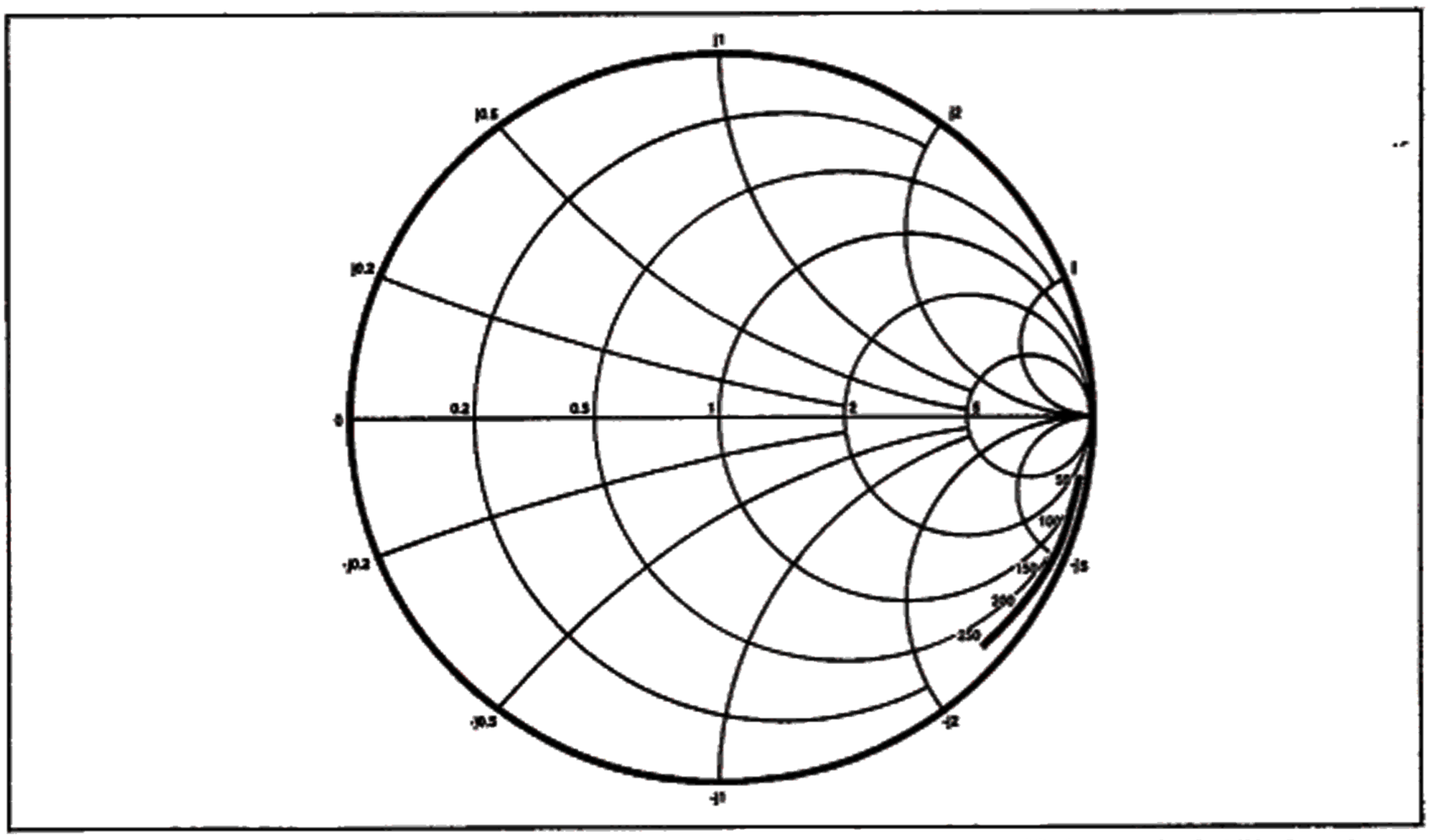



*Fig.5 Typical input impedance. Test conditions: supply voltage 5.0V, ambient temperature 25°C, frequencies in MHz, impedances normalised to 50 Ohms.*

## OPERATING NOTES

1. The clock inputs can be driven from ECL II, III and 10K. The input reference voltage (-3.8V at 25°C) is compatible with ECL II, III and 10K over the specified temperature range. The inputs can also be capacitively coupled by addition of external bias as shown in Fig. 6. Each input has an internal pull-down resistor of 10k, and unused inputs can therefore be left open circuit. They should by bypassed to RF where maximum noise immunity is required.
2. The PE control inputs are similarly ECL III/10K compatible and also have an internal 10k pull-down resistor, allowing unused inputs to be left open circuit if required.
3. The $Q_4$ and $\overline{Q}_4$ ECL outputs have internal circuitry equivalent to a 14k pull-down resistor on each output and are ECL II compatible: they can however be interfaced to ECL III/10K as shown in Fig. 8.
4. The circuit will operate down to DC but slew rate must be better than 5V/µs.
5. The input impedance of SP8695 varies as a function of frequency. See Fig. 5.
6. The TTL/CMOS output has a free collector and the high state output voltage will depend on the supply that the collector load is taken to. This should not exceed 12V. The rise and fall time of the open collector output waveform is directly proportional to load capacitance and load resistance value. Therefore load capacitance should be kept to a minimum and the load resistor kept to a minimum compatible with system power requirements. In the test configuration of Fig. 6 the output rise time is approximately 10ns and fall time is 7ns typically.

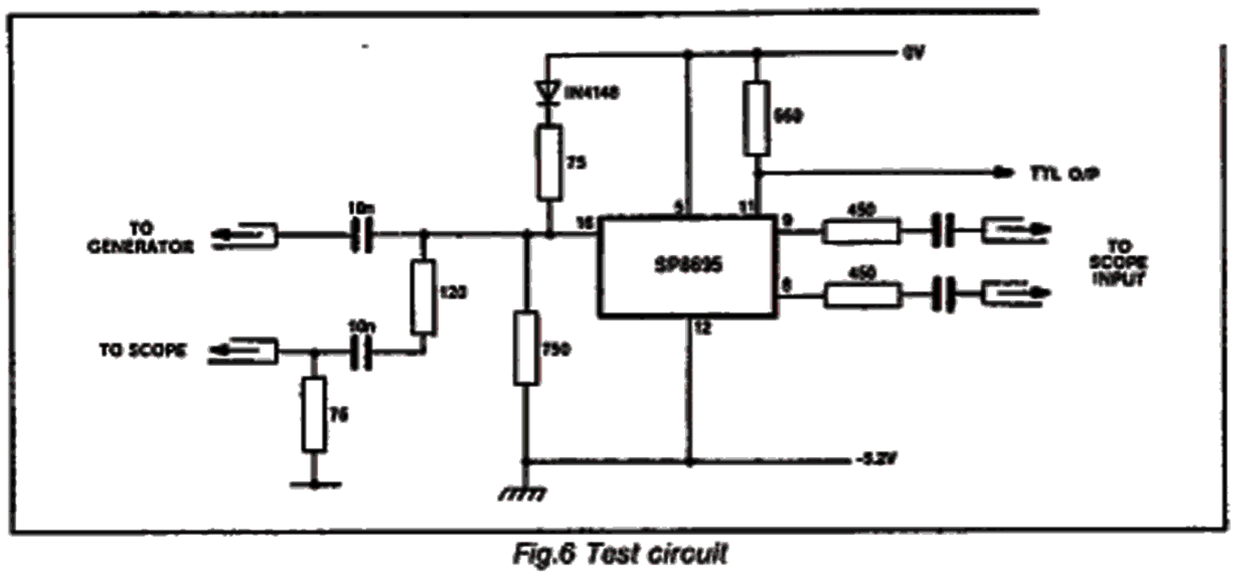



*Fig.6 Test circuit*

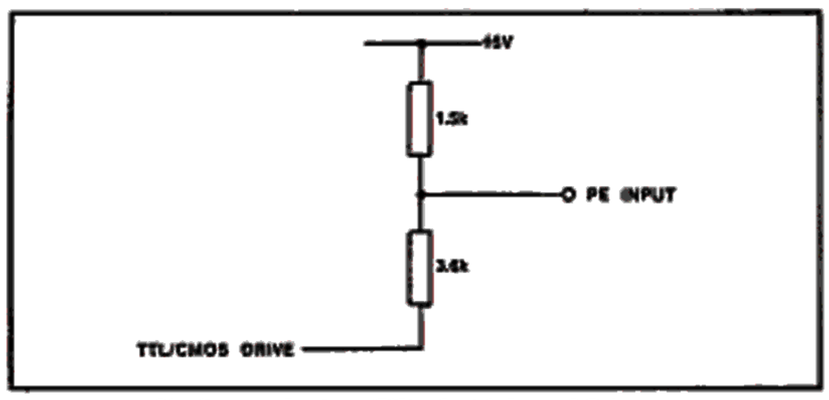



*Fig.7 Interfacing TTL/CMOS to PE inputs*

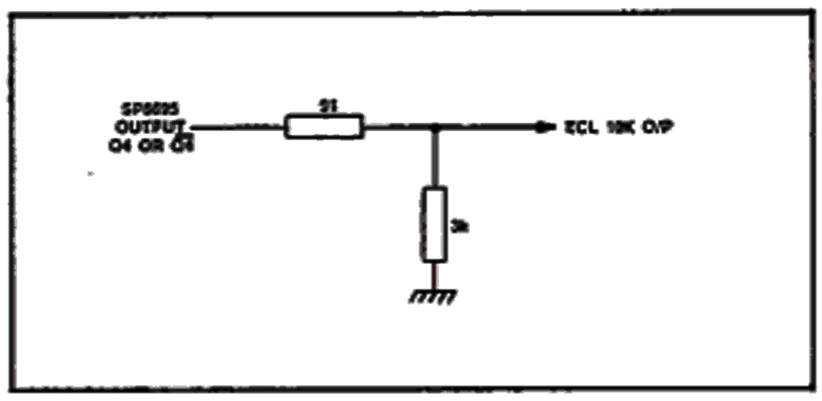



*Fig.8 Interfacing to SP8695 output to ECL 10K*

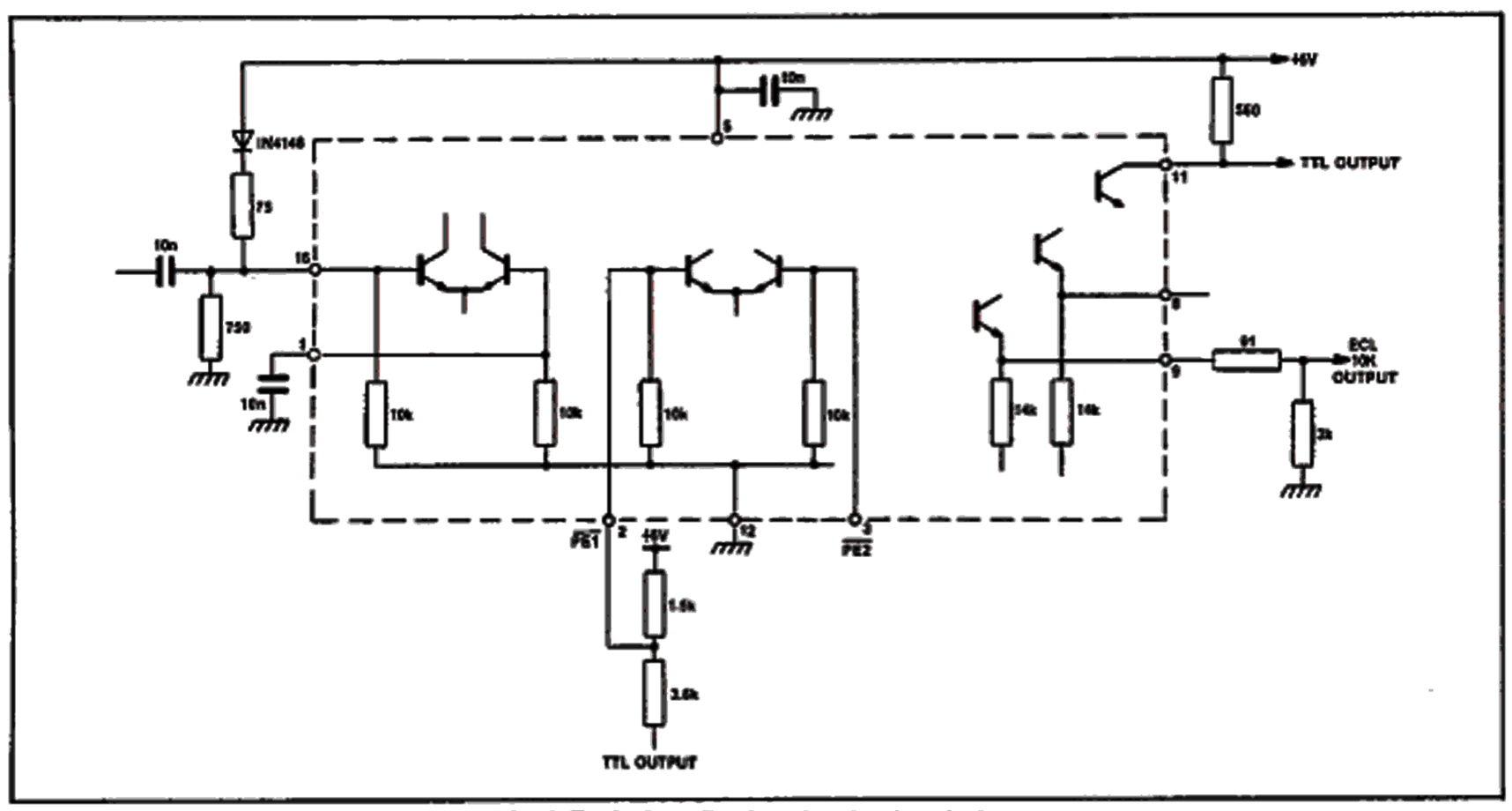



*Fig.9 Typical application showing interfacing*