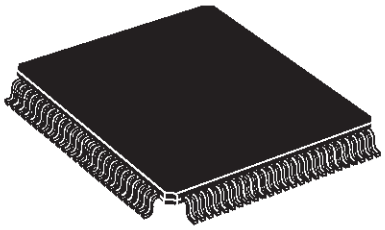
STV7617D
STV7617U

PLASMA DISPLAY PANEL SCAN DRIVER

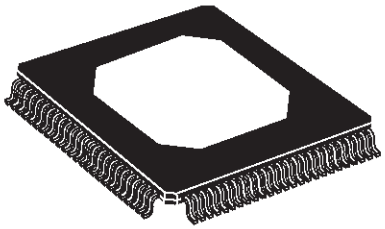
PRELIMINARY DATA

- 64/65 SELECTABLE OUTPUT PLASMA DISPLAY DRIVER
- 100V ABSOLUTE MAXIMUM SUPPLY
- 5V SUPPLY FOR LOGIC
- 100/700mA SOURCE/SINK OUTPUT
- 700mA SOURCE/SINK OUTPUT DIODE
- 65-BIT BIDIRECTIONAL SHIFT REGISTER (8MHz)
- HIGH IMPEDANCE OUTPUT CONTROL
- BCD TECHNOLOGY
- 100-PIN TQFP PACKAGE WITH INTEGRATED HEATSINK



TQFP100 (14 x 14 x 1.4mm Slug-down)
(Thin Plastic Quad Flat Pack)

ORDER CODE : STV7617D



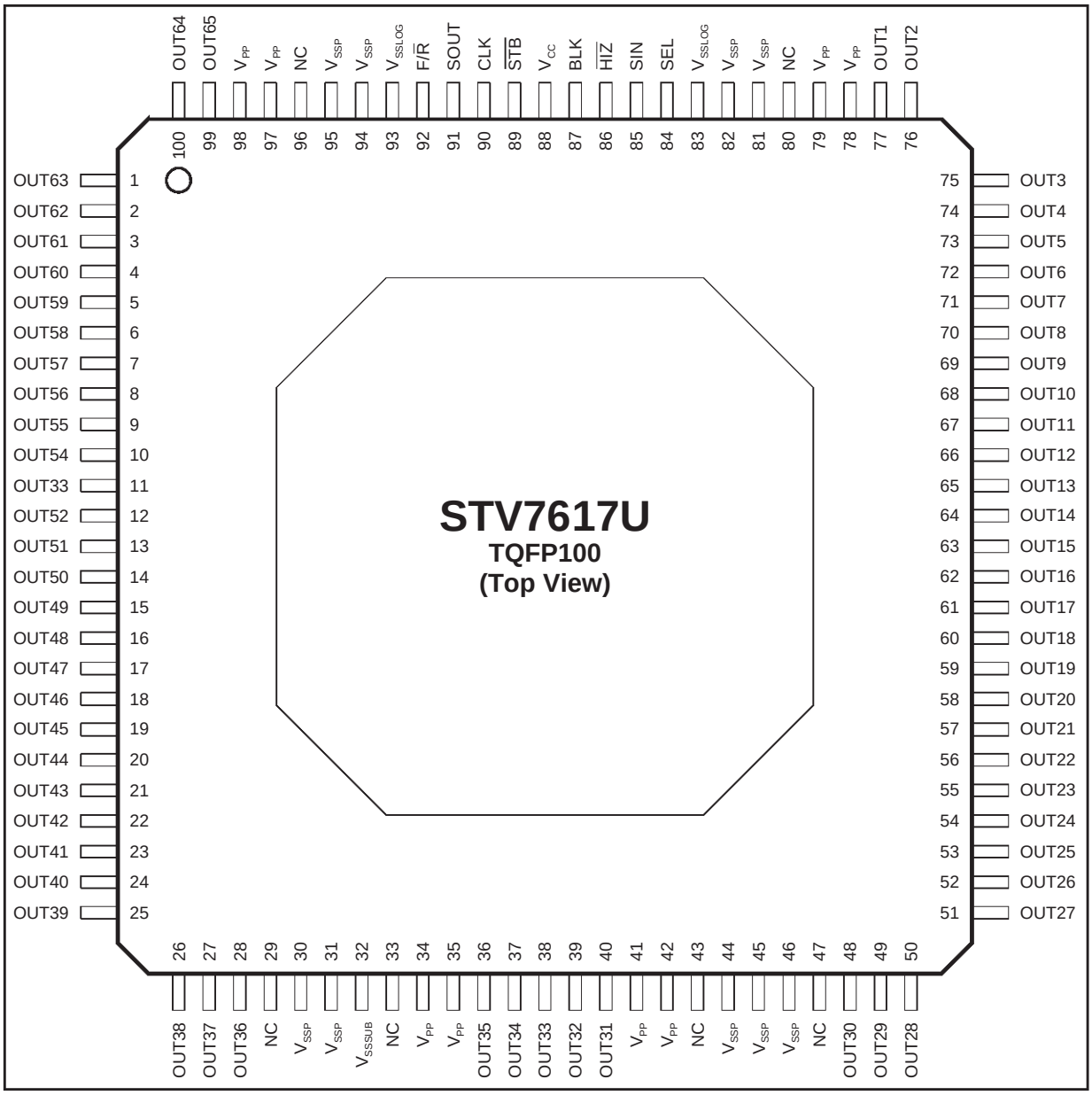
TQFP100 (14 x 14 x 1.4mm Slug-up)
(Thin Plastic Quad Flat Pack)

ORDER CODE : STV7617U

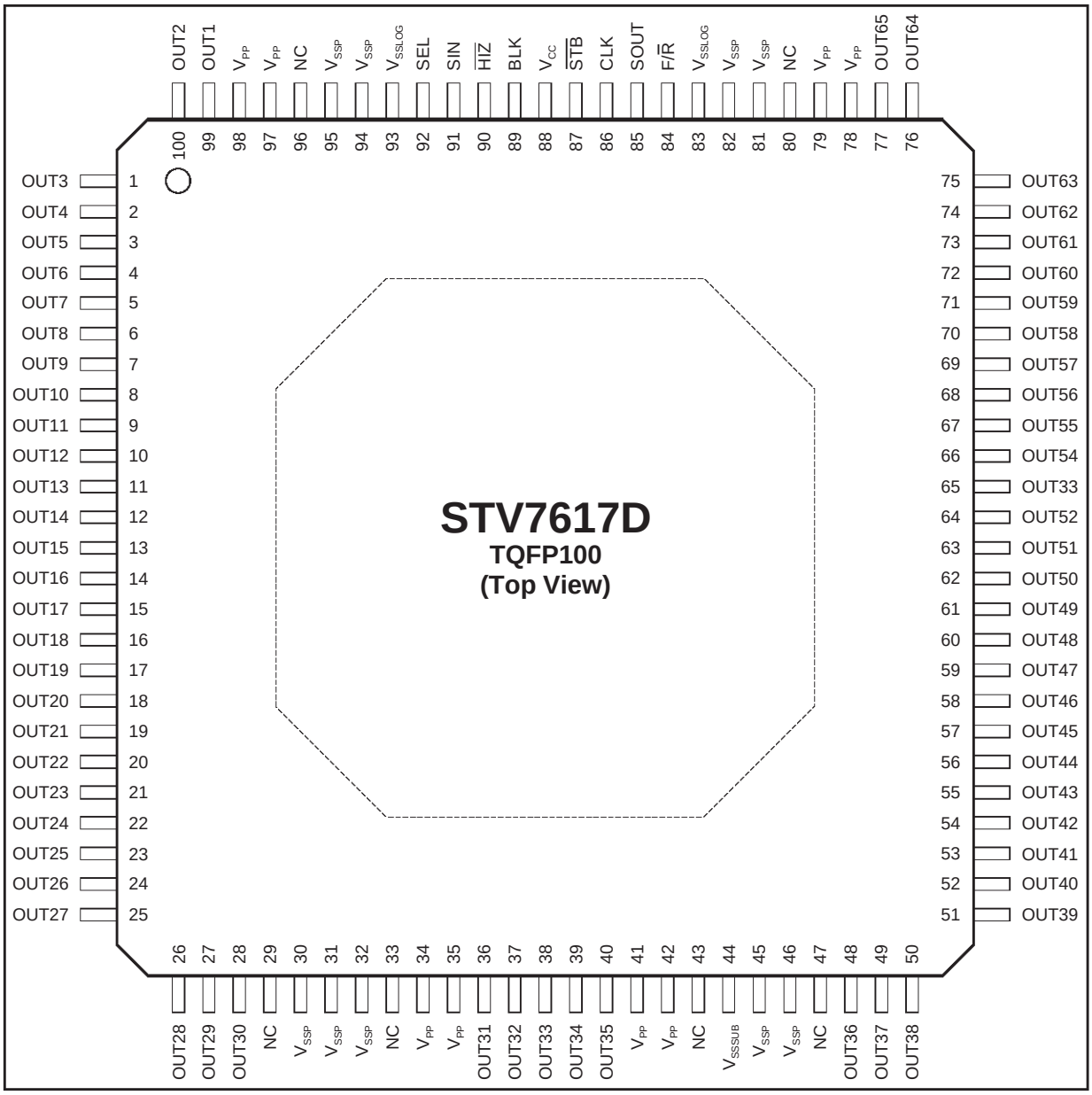
DESCRIPTION

The STV7617 is a scan driver for Plasma Display Panel (PDP) implemented in ST's proprietary BCD technology. Using a 65-bit cascadable 8MHz shift register, it drives 65 high current & high voltage outputs. The STV7617 can be configured either in 64 or 65 outputs depending on the SEL input Pin. By serialy connecting several STV7617, any vertical pixel definition can be performed. The STV7617 is supplied with a separated 90V power output supply and a 5V logic supply. All command inputs are CMOS compatible. The STV7617 package is a 100-pin TQFP with integrated heatsink located on the bottom (STV7617D) or top (STV7617U) of the package.

PIN CONNECTIONS (TQFP100 Slug-up)



PIN CONNECTIONS (TQFP100 Slug-down)



PIN ASSIGNMENT (TQFP100)

Pin Number		Symbol	Type	Function
TQFP100 Slug-up	TQFP100 Slug-down			
88	88	V_{CC}	Supply	5V Logic Supply
34-35-41-42 78-79-97-98	34-35-41-42 78-79-97-98	V_{PP}	Supply	High Voltage Supply of power outputs
30-31-44-45 46-81-82-94-95	30-31-32-45 46-81-82-94-95	V_{SSP}	Ground	Ground of power outputs
83-93	83-93	V_{SSLOG}	Ground	Logic Ground
32	44	V_{SSSUB}	Ground	Substrate Ground
77 to 48, 40 to 36, 28 to 1, 100-99	99-100, 1 to 28, 36 to 40, 48 to 77	OUT1 to OUT 65	Output	Power Output
91	85	SOUT (SIN)	Output	Shift Register Data Output
90	86	CLK	Input	Clock of data shift register
89	87	$\overline{STB}$	Input	Latch of data to outputs
87	89	BLK	Input	Power Output Blanking Control
86	90	$\overline{HIZ}$	Input	Power Output High Impedance Control
85	91	SIN (SOUT)	Input	Shift Register Data Input
84	92	SEL	Input	Selection of number of power outputs
92	84	F/$\overline{R}$	Input	Selection of shift direction
29-33-43-47-80-96	29-33-43-47-80-96	NC	-	Not connected

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PIN ASSIGNMENT (Power Outputs)

Output Number	Pin Number	
	Slug-down	Slug-up
1	77	99
2	76	100
3	75	1
4	74	2
5	73	3
6	72	4
7	71	5
8	70	6
9	69	7
10	68	8
11	67	9
12	66	10
13	65	11
14	64	12
15	63	13
16	62	14
17	61	15
18	60	18
19	59	17
20	58	18
21	57	19
22	56	20

Output Number	Pin Number	
	Slug-down	Slug-up
23	55	21
24	54	22
25	53	23
26	52	24
27	51	25
28	50	26
29	49	27
30	48	28
31	40	36
32	39	37
33	38	38
34	37	39
35	36	40
36	28	48
37	27	49
38	26	50
39	25	51
40	24	52
41	23	53
42	22	54
43	21	55
44	20	56

Output Number	Pin Number	
	Slug-down	Slug-up
45	19	57
46	18	58
47	17	59
48	16	60
49	15	61
50	14	62
51	13	63
52	12	64
53	11	65
54	10	66
55	9	67
56	8	68
57	7	69
58	6	70
59	5	71
60	4	72
61	3	73
62	2	74
63	1	75
64	100	76
65	99	77

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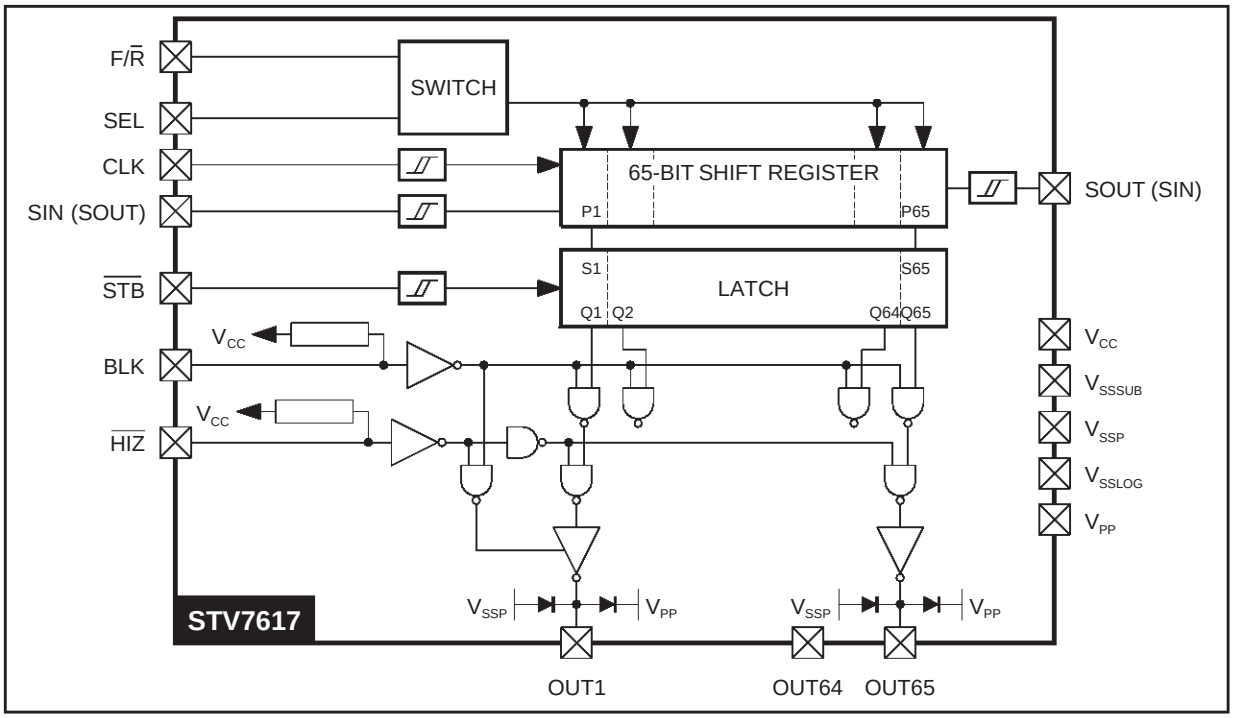
BLOCK DIAGRAM



CIRCUIT DESCRIPTION

The STV7617 contains all the logic and the power circuits necessary to drive rows of a Plasma Display Panel (PDP). Data is shifted at each low to high transition of the (CLK) shift clock. After 64 or 65 shifts (depending on SEL) the first bit presented at (SIN) is available at the serial output (SOUT). This output can be used to cascade several drivers to perform any vertical resolution. CLK, STB, SIN and SOUT inputs are Smith trigger inputs. BLK and HIZ logical inputs are internally pulled to level "1". The maximum frequency of the shift clock is 8MHz.

Shift register outputs (P1, ... P65) are transferred from the shift register into the latch stage when the latch input (STB) is at low level.

Table 1 : Output State Configuration

STB	BLK	HIZ	Output State
*	L	L	High impedance
L	L	H	Inverted copy of input data
H	L	H	Data latched
*	H	L	Low level
*	H	H	High level

Sustain current must not be sunk in the power outputs to V_{PP} when the power supply is applied and output state is in HIZ or at high state.

V_{SSSUB} and V_{SSLOG} must be connected as close as possible to the logical reference ground of the application.

Table 2 : Shift Register Truth Table

F/R	CLK	SIN	SOUT	Comments
H	Rise	In	Out	Forward Shift
H	L or H	In	Out	Steady
L	Rise	Out	In	Reverse Shift
L	L or H	Out	In	Steady

Table 3 : Power Output Configuration

SEL	F/R	Number of Outputs	Comments
L	L	64	Out1 is in Hi-Z mode (outputs 65 to 2 powered)
L	H	64	Out65 is in Hi-Z mode (outputs 1 to 64 powered)
H	L	65	Out 65 to Out 1 powered
H	H	65	Out 1 to Out 65 powered

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Logic Supply (Pin 88) *	-0.3, +7	V
V_{PP}	Driver Supply (Pins 34, 35, 41, 42, 78, 79, 97, 98) *	-0.3, +100	V
V_{IN}	Logic Input Voltage (Pins 84, 86, 87, 89, 90, 91, 92) *	-0.3, V_{CC} + 0.3	V
V_{OUT}	Logic Output Voltage (Pin 85)*	-0.3, V_{CC} + 0.3	V
V_{POUT}	Driver Output Voltage (scanning mode)	-0.3, +100	V
I_{POUT}	Driver Output Current (2)(4)	-100, +700	mA
I_{DOUT}	Diode Output Current (3)(4)	±700	mA
T_{jmax}	Junction Temperature	+150	°C
T_{oper}	Operating Temperature	-20, +85	°C
T_{stg}	Storage Temperature	-50, +150	°C

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* In case of STV7617D

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th(j-a)}$	Junction-ambient Typical Thermal Resistor (1)	25	°C/W
T_{joper}	Maximum Operating Junction Temperature (1)	125	°C

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Notes : 1. For TQFP100 packaging.
2. Through one power output.
3. Through all power outputs (see test diagram) : with Power dissipation lower or equal than P_{tot} and Junction temperature lower or equal than T_{jmax} and $V_{PP} = V_{SSP}$.
4. These parameters are measured during ST's internal qualification which includes temperature characterisation on standard batches and on corners batches of the process. These parameters are not tested on the parts.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V, V_{PP} = 90V, V_{SSP} = 0V, V_{SSLOG} = 0V, V_{SSSUB} = 0V, T_{amb} = 25°C, f_{CLK} = 8MHz, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SUPPLY						
V_{CC}	Logic Supply Voltage		4.5	5	5.5	V
I_{CCH}	Logic Supply Current		-	-	100	µA
I_{CCL}	Logic Supply Current	f_{CLK} = 8MHz	-	5	-	mA
V_{PP}	Power Output Supply Voltage		20	-	90	V
I_{PPH}	Power Output Supply Current (steady outputs)		-	-	100	µA
OUTPUT						
OUT1-OUT64						
V_{POUTH}	Power Output High Level	I_{POUTH} = - 20mA	80	86	-	V
V_{POUTH}	Power Output High Level	I_{POUTH} = - 15mA, V_{PP} = 40V	30	33	-	V
V_{POUTL}	Power Output Low Level	I_{POUTL} = + 400mA	-	2.5	5	V
V_{DOUTH}	Output Diode High Level	I_{DOUTH} = + 400mA (5)(6)	-	1.7	5	V
V_{DOUTL}	Output Diode Low Level	I_{DOUTL} = - 400mA (5)(6)	-	-1.2	-5	V
SOUT						
V_{OH}	Logic Output High Level	I_{OH} = - 1mA	4	4.2	-	V
V_{OL}	Logic Output Low Level	I_{OL} = + 1mA	-	0.1	0.4	V
INPUT (CLK, $\overline{STB}$, BLK, $\overline{HIZ}$, SIN, SEL)						
V_{IH}	Input High Level		0.8 V_{CC}	-	-	V
V_{IL}	Input Low Level		-	-	0.2 V_{CC}	V
I_{IH}	High Level Input Current	$V_{IH} = V_{CC}$	-	-	10	µA
I_{IL}	Low Level Input Current CLK, SIN, STB, SEL BLK, $\overline{HIZ}$	V_{IL} = 0V	 - -	 - -	 -10 -40	 µA µA

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Notes : 5. Compatible with power dissipation and $T_{joper} \leq 125°C$.
6. See test diagram page 9.

AC TIMINGS REQUIREMENTS

(V_{CC} = 4.5V to 5.5V, T_{amb} = -20 to +85°C, input signals max leading edge & trailing edge (t_R, t_F) = 10ns)

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{WHCLK}	Duration of clock (CLK) pulse at high level	40	-	-	ns
t_{WLCLK}	Duration of clock (CLK) pulse at low level	40	-	-	ns
t_{SDAT}	Set-up Time of data input before clock (low to high) transition	10	-	-	ns
t_{HDAT}	Hold Time of data input after clock (low to high) transition	20	-	-	ns
t_{DSTB}	Minimum Delay to latch ($\overline{STB}$) after clock (low to high) transition	25	-	-	ns
t_{SSTB}	Set-up Time ($\overline{STB}$) before clock (low to high) transition	10	-	-	ns
t_{STB}	Latch ($\overline{STB}$) Low Level Pulse Duration	20	-	-	ns
t_{BLK}	Blanking (BLK) Pulse Duration	500	-	-	ns
t_{HIZ}	High Impedance ($\overline{HIZ}$) Pulse Duration	500	-	-	ns

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AC TIMING CHARACTERISTICS

(V_{CC} = 5V, V_{PP} = 90V, V_{SSP} = 0V, V_{SSLOG} = 0V, V_{SSSUB} = 0V, T_{amb} = 25°C, $V_{ILMax.}$ = 0.2V_{CC}, $V_{IHMin.}$ = 0.8V_{CC}, V_{OH} = 4.0V, V_{OL} = 0.4V, unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{CLK}	Data Clock Period	125	-	-	ns
t_{RDAT}	Logical Data Output Rise Time	-	12	-	ns
t_{FDAT}	Logical Data Output Fall Time	-	10	-	ns
t_{PHL1} t_{PLH1}	Delay of logic data output (high to low transition) after clock (CLK) transition (C_L = 10pF) Delay of logic data output (low to high transition) after clock (CLK) transition (C_L = 10pF)	- -	37 42	50 60	ns ns
t_{PHL2} t_{PLH2}	Delay of power output change (high to low transition) after clock (CLK) transition Delay of power output change (low to high transition) after clock (CLK) transition	- -	110 115	180 180	ns ns
t_{PHL3} t_{PLH3}	Delay of power output change (high to low transition) after Latch ($\overline{STB}$) transition Delay of power output change (low to high transition) after Latch ($\overline{STB}$) transition	- -	80 95	165 165	ns ns
t_{PHL4} t_{PLH4}	Delay of power output change (high to low transition) to Blank (BLK) transition Delay of power output change (low to high transition) to Blank (BLK) transition	- -	75 75	160 160	ns ns
t_{PHZ5} t_{PLZ5}	Delay of power output change (high to Hi-Z transition) after high impedance ($\overline{HIZ}$) (6) Delay of power output change (low to Hi-Z transition) after high impedance ($\overline{HIZ}$) (6)	- -	40 80	160 160	ns ns
t_{PZH5} t_{PZL5}	Delay of power output change (Hi-Z to high transition) after high impedance ($\overline{HIZ}$) (6) Delay of power output change (Hi-Z to low transition) after high impedance ($\overline{HIZ}$) (6)	- -	75 40	160 160	ns ns
t_{ROUT}	Power Output Rise Time (7)	-	175	500	ns
t_{FOUT}	Power Output Fall Time (7)	-	35	300	ns

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Notes : 6. See test diagram page 9.
7. One output among 64, loading capacitor C_{OUT} = 200pF, other outputs at low level.

Figure 1 : AC Characteristics Waveform

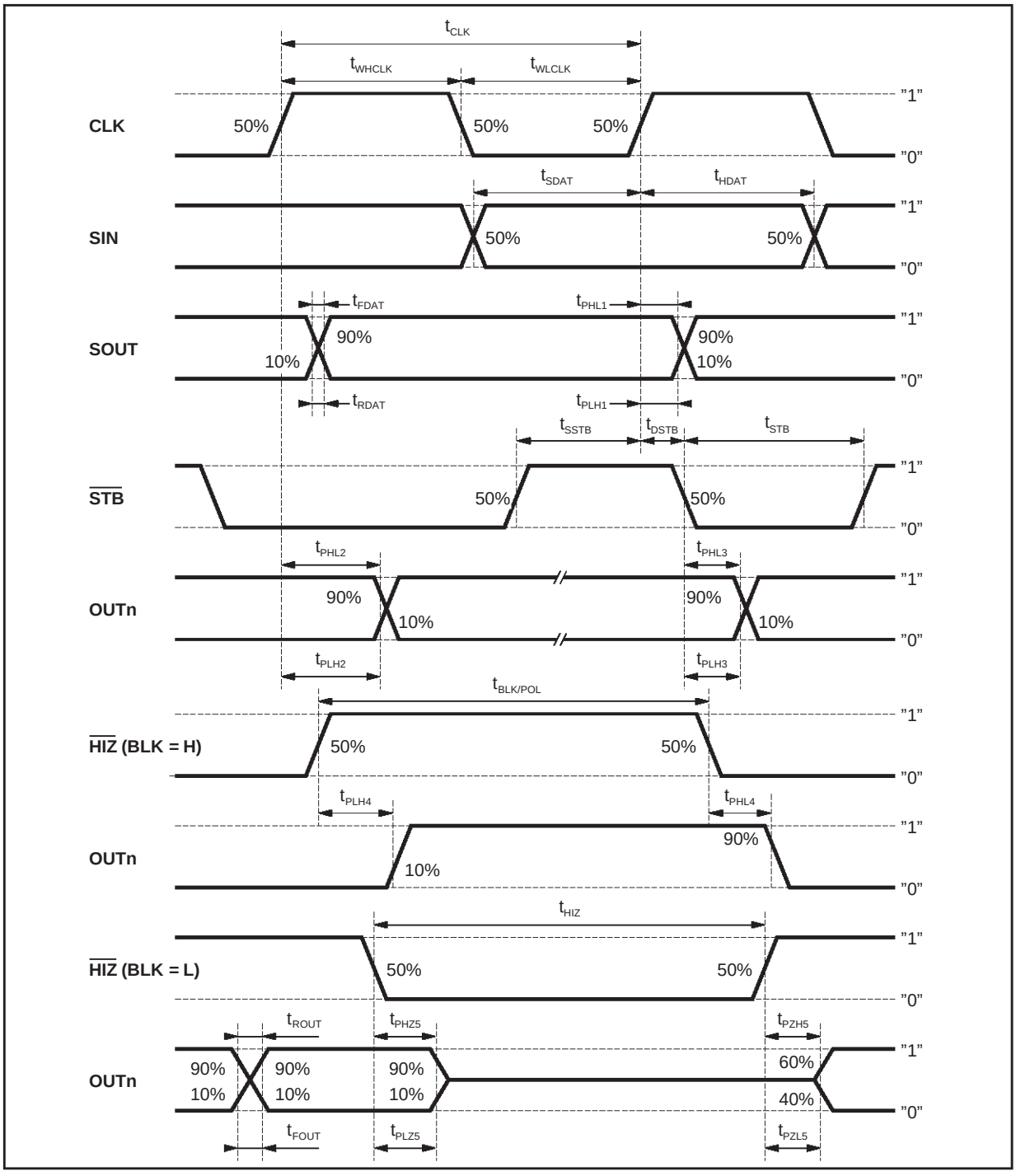
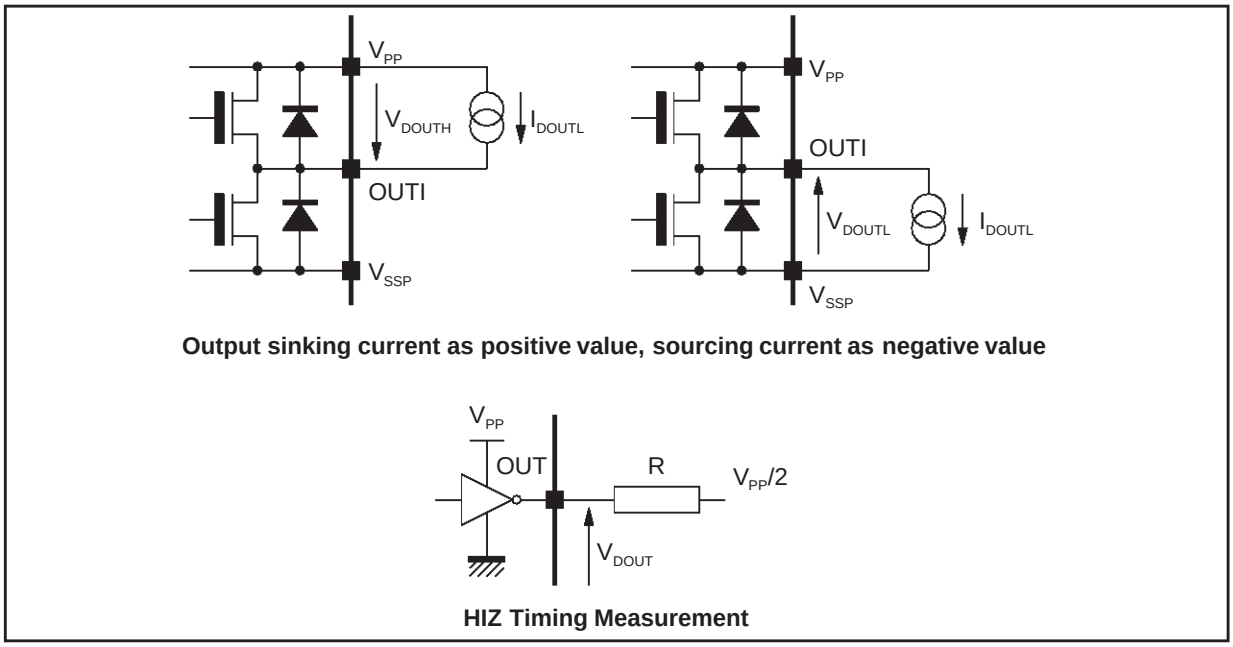


Figure 2 : Test Configuration



INPUT/OUTPUT SCHEMATICS

Figure 3 : BLK, $\overline{HIZ}$ Input

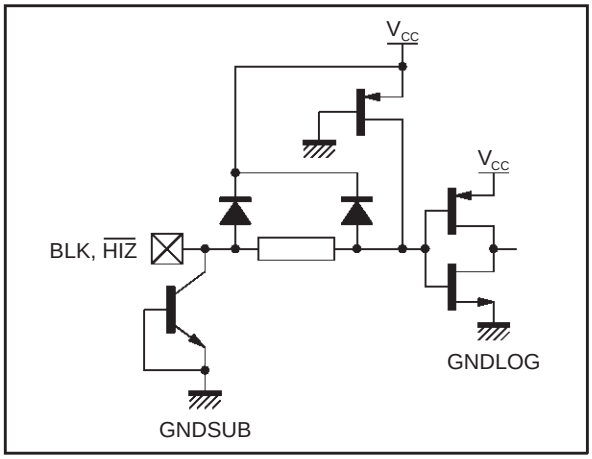


Figure 4 : F/$\overline{R}$, SEL, CLK, $\overline{STB}$ Input

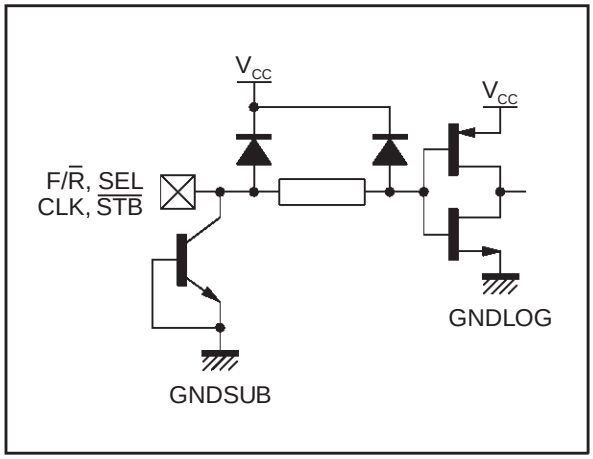


Figure 5 : SIN, SOUT Input

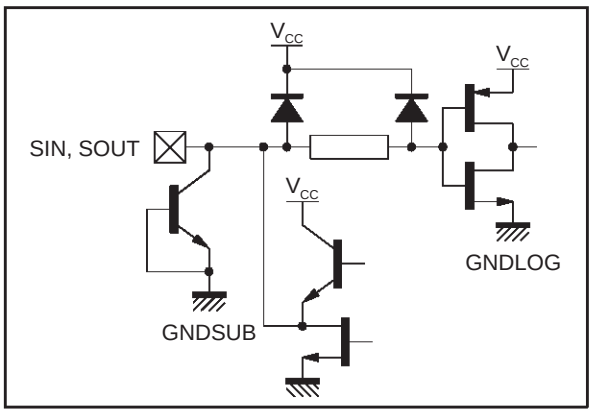
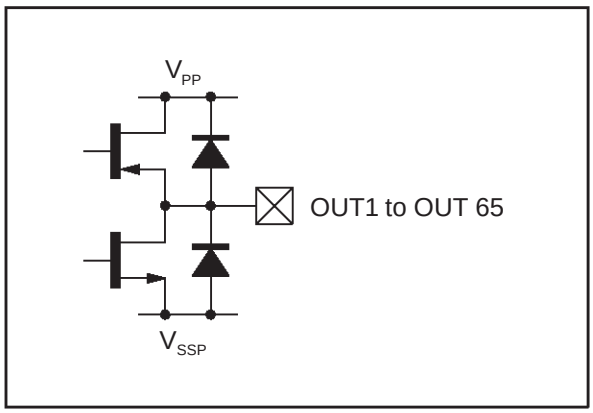
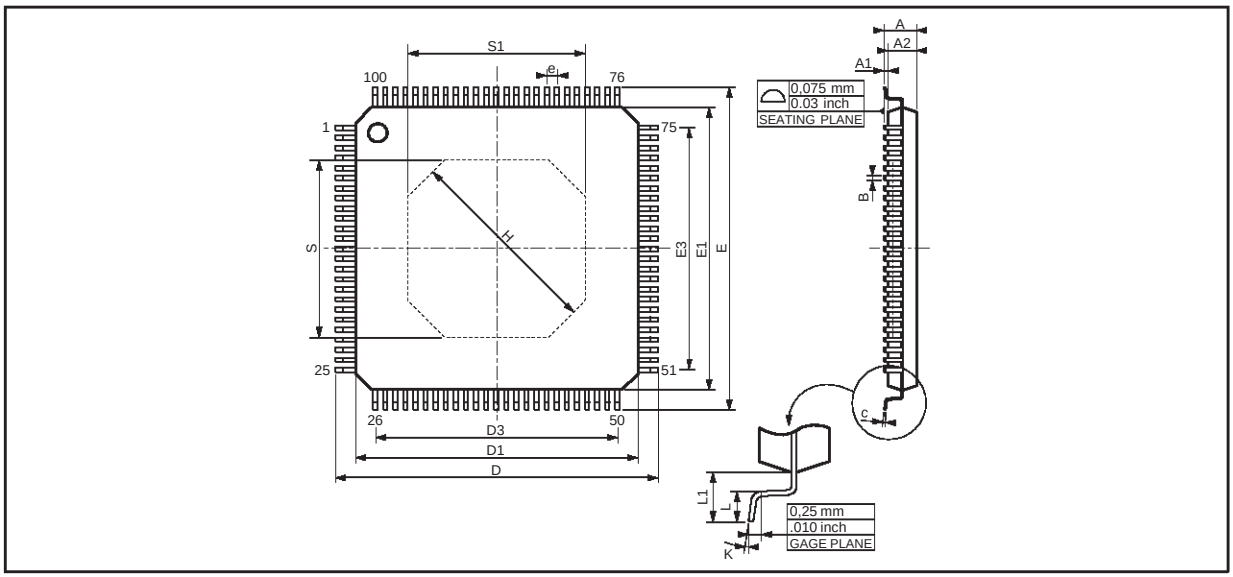


Figure 6 : Power Output



PACKAGE MECHANICAL DATA : 100 PINS - THIN PLASTIC QUAD FLAT PACK (TQFP) (Slug-down)



PM-1B.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.17	0.22	0.27	0.007	0.009	0.011
C	0.09		0.20	0.004		0.008
D		16.00			0.630	
D1		14.00			0.551	
D3		12.00			0.472	
e		0.50			0.20	
E		16.00			0.630	
E1		14.00			0.551	
E3		12.00			0.472	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
K	0^o (Min.), 7^o (Max.)					
Slug Dimension for L/Frame Pad Size 10.00 x 10.00mm						
H		9.85			0.388	
S	8.80			0.346		
S1	8.80			0.346		

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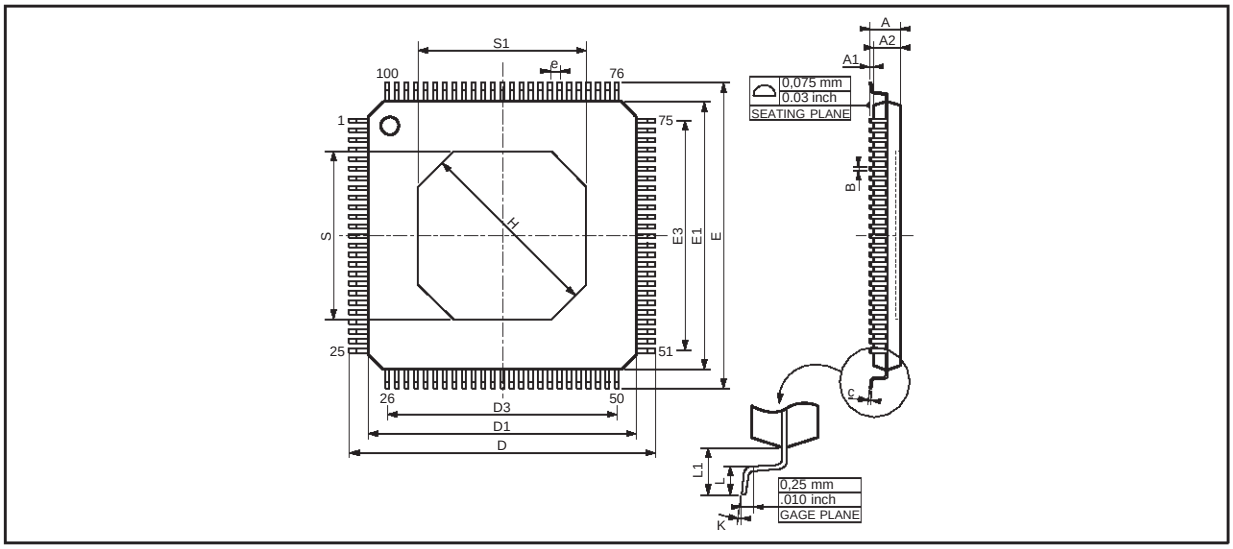
PACKAGE MECHANICAL DATA : 100 PINS - THIN PLASTIC QUAD FLAT PACK (TQFP) (Slug-up)



PM-4S.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.17	0.22	0.27	0.007	0.009	0.011
C	0.09		0.20	0.004		0.008
D		16.00			0.630	
D1		14.00			0.551	
D3		12.00			0.472	
e		0.50			0.20	
E		16.00			0.630	
E1		14.00			0.551	
E3		12.00			0.472	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
K	0^o (Min.), 7^o (Max.)					
Slug Dimension for L/Frame Pad Size 10.00 x 10.00mm						
H		9.85			0.388	
S	8.80			0.346		
S1	8.80			0.346		

4S.TBL