

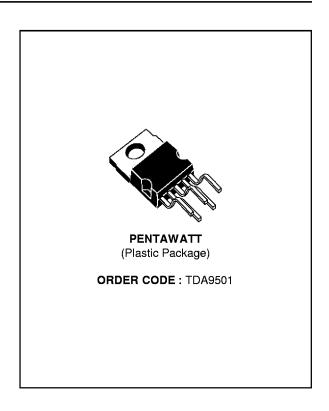
TDA9501

AC COUPLING HIGH VOLTAGE VIDEO AMPLIFIER

BANDWIDTH: 40MHzTYPICAL
 RISE AND FALLTIME: 9ns TYPICAL

SUPPLY VOLTAGE: 90VPOWER DISSIPATION: 2.3W

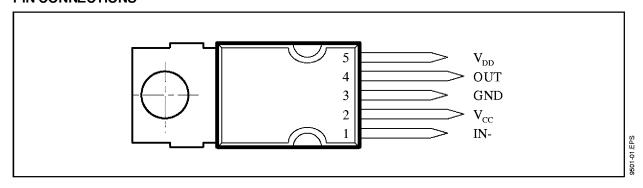
■ ESD PROTECTED



DESCRIPTION

The TDA9501 is a video amplifier designed with a high voltage Bipolar/CMOS/DMOS technology (BCD). It drives in AC coupling mode one cathode of a monitor and is protected against flashovers. It is available in Pentawatt package.

PIN CONNECTIONS

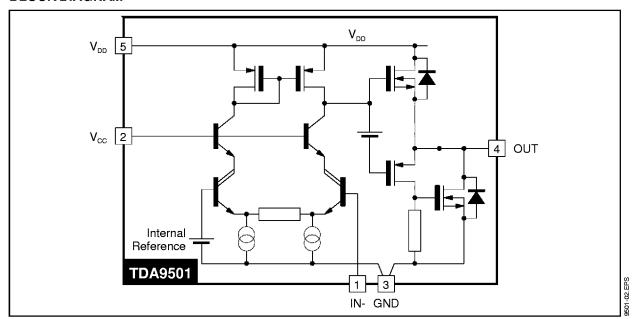


PIN CONFIGURATION

Pin N	Symbol	Function			
1	IN-	Input of the amplifier			
2	Vcc	Low Voltage Power Supply			
3	GND	Also connected to the heatsink			
4	OUT	Output driving the cathode			
5	V _{DD}	High Voltage Power Supply			

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BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{\text{OUT}}, V_{\text{DD}}$	Supply High Voltage (Pins 4-5)	100	٧
V _{CC}	Supply Low Voltage (Pin 2)	20	V
lop log	Output Current to V _{DD} (Pin 4) Output Current to Ground (Pin 4) (See note 1)	protected 80	mA
lj	Input Current (Pin 1)	50	mA
VESD	ESD Susceptibility - Human Body Model, 100pF Discharge through 1.5kΩ (see Note 2) - EIAJ Norm, 200pF Discharge through 0Ω (see Note 3)	2 300	kV V
Tj	Junction Temperature	150	°C
T _{oper}	Operating Ambient Temperature	0, +70	ိုင
T _{stg}	Storage Temperature	-20, +150	°C

Notes: 1. Pulsed current $t \leq 50 \mu s.$

2. Except $V_{DD} = 800V$.

3. Except VDD & VCC = 120V.

THERMAL DATA

Symbol	Parameter	Value	Unit
R _{th (j-c)}	Junction-Case Thermal Resistance Max.	3	°C/W
R _{th (j-a)}	Junction-Ambient Thermal Resistance Typ.	70	°C/W

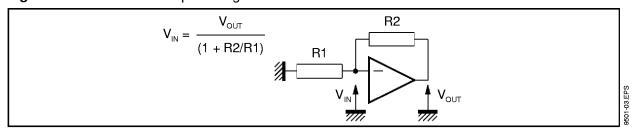
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$\textbf{ELECTRICAL CHARACTERISTICS} \ (V_{CC} = 12V, V_{DD} = 90V, T_{amb} = 25^{o}C, unless \ otherwise \ specified)$

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
V_{DD}	High Supply Voltage (Pin 5)		30		90	V
V _{CC}	Low Supply Voltage (Pin 2)		10	12	15	V
l _{DD}	High Voltage SupplyInternal DC Current (without current due to the feedback network)	V _{OUT} = 50V		10	15	mA
lcc	Low Voltage Supply Internal DC Current			5.5		mA
V _{IN}	Input Voltage	See Figure 1	3.55	3.8	4.05	V
dV_{IN}/dV_{CC}	Drift of Input Voltage versus V _{CC}			0.15		%
dV _{IN} /dT	Drift of Input Voltage versus Temperature	See Note 4		2		mV/°C
V _{SATH}	High Output Saturation Voltage (Pin 4)	I _O = -60mA		V _{DD} - 6.5		V
V _{SATL}	Low Output Saturation Voltage (Pin 4)	I _O = 60mA		17		V
ELin	Linearity Error	17V < V _{OUT} < V _{DD} - 15V		5	8	%
os	Overshoot			5		%
BW	Bandwidth at -3dB	$\label{eq:local_problem} \begin{split} &\text{Measured on CRT cathodes.} \\ &C_{\text{LOAD}} = 10 \text{pF,} \\ &\text{Rprotect} = 200 \Omega, \text{ Gain} = 20 \\ &V_{\text{OUT}} = 50 \text{V,} \Delta V_{\text{OUT}} = 20 \text{V}_{\text{PP}} \end{split}$		40		MHz
t _R , t _F	Rise and Fall Time	Measured between 10% & 90% of output pulse, $C_{LOAD} = 10pF$, Rprotect = 200Ω , Gain = 20 $V_{OUT} = 50V$, $\Delta V_{OUT} = 40V_{PP}$		9		ns
Go	Open Loop Gain	V _{OUT} = 50V		57		dB
I _{IB}	Input Bias Current (Pin 1)	V _{OUT} = 50V		10		μΑ
R _{IN}	Input Resistance	See Note 4		200		kΩ

Note 4: Characterized and not tested.

Figure 1 : Measurement of Input Voltage



TYPICAL APPLICATION

The TDA9501 consists of:

- A differential amplifier with active load,
- A DMOS output buffer,
- A bandgap voltage reference.

PC board lay-out

The best performances are obtained with a carefully designed HF PC-Board, especially for the output and input capacitors.

The feedback resistor RF must have a low parasitic capacitor ($C_F < 0.3pF$).

This parasitic capacitor CF must be compensated by a capacitor R3 (roughly 20 · C_F) connected in parallel with the input resistor R1.

The full bandwidth of the device is only obtained with well matched compensation otherwise the application will have either an integrator response with a low bandwidth or a differentiator response with too much ringing.

A diode D_P (see Figure 2) has to be connected for flashover protection.

Power dissipation

The power dissipation consists of a static part and a dynamic part. The static dissipation varies with the output voltage and the feedback resistor. The dynamic power dissipation increases with the pixel frequency.

For a signal frequency of 40MHz and 40V_{PP} output signal, the typical power dissipation is about 3.0W, for $V_{DD} = 110V$.

In first approximation, the dynamic dissipation is:

$$P_D = V_{DD} * C_{LOAD} * \Delta V_{OUT} * f$$

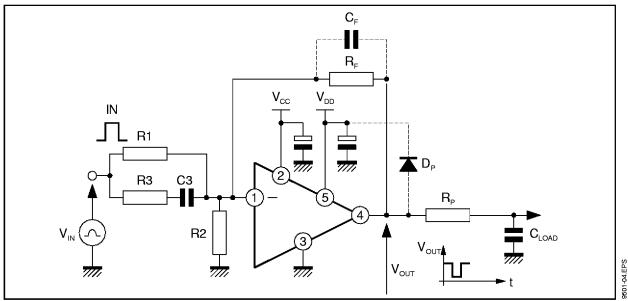
and the total dissipation is:

$$P = V_{DD} * C_{LOAD} * \Delta V_{OUT} * f + V_{DD} * I_{DD}$$
$$+ V_{CC} * I_{CC} - (V_{DD} - V_{OUT}) \frac{V_{OUT}}{R_{FEEDBACK}}$$

with f = pixel frequency

 $P = 110V \times 10pF \times 40V \times 40MHz + 110V \times 7mA$ $+12 \times 20 \text{mA} - 60^2 \text{V} / 20 \text{k}\Omega = 2.95 \text{W}$

Figure 2: Typical Evaluation Schematic



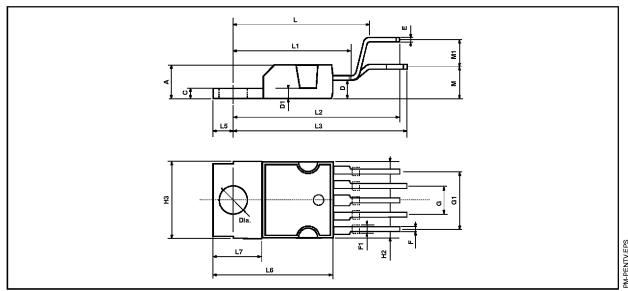
Recommended values:

 $R1 = 1k\Omega$, $R2 = 1.8k\Omega$, $R_F = 20k\Omega$, $R_P = 200\Omega$,

 $C3 = 10 \text{ to } 12pF \text{ for } C_F \# 0.5pF.$

R3 # 150Ω .

PACKAGE MECHANICAL DATA: 5 PINS - PLASTIC PENTAWATT



Dimensions	Millimeters			Inches			
Dimensions	Min.	Тур.	Max.	Min.	Тур.	Max.	
Α			4.8			0.189	
С			1.37			0.054	
D	2.4		2.8	0.094		0.110	
D1	1.2		1.35	0.047		0.053	
E	0.35		0.55	0.014		0.022	
F	0.8		1.05	0.031		0.041	
F1	1		1.4	0.039		0.055	
G		3.4		0.126	0.134	0.142	
G1		6.8		0.260	0.268	0.276	
H2			10.4			0.409	
НЗ	10.05		10.4	0.396		0.409	
L		17.85			0.703		
L1		15.75			0.620		
L2		21.4			0.843		
L3		22.5			0.886		
L5	2.6		3	0.102		0.118	
L6	15.1		15.8	0.594		0.622	
L7	6		6.6	0.236		0.260	
М		4.5			0.177		
M1		4			0.157	0.152	
Dia	3.65		3.85	0.144		0.152	

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