T-75-37-07

1. INTRODUCTION

The TMP68661 enhanced programmable communications interface (EPCI) is a universal synchoronous/asynchronous data communications controller chip that is an enhanced version of the Signetics 2651. The EPCI directly interfaces to most 8-bit MPUs and easily to the TMP68000 MPU and other 16-bit MPUs. It may be used in either a polled or interrupt driven system. Programmed instructions can be accepted from the host MPU while supporting many synchronous or asynchronous serial-data communication protocols in a full-or half-duplex mode. Special support for BISYNC is provided.

The EPCI converts parallel data characters, accepted from the microprocessor data bus, into transmit-serial data. Simultaneously, the EPCI can convert receive-serial data to parallel data characters for input to the microprocessor.

A baud-rate generator in the EPCI can be programmed either to accept an external clock or to generate transmit or receive clocks. Sixteen different baud rates can be selected under program control when operating in the internal clock mode. Each version of the EPCI (A, B, C) has a different set of baud rates.

Synchronous Operation

- Single or Double SYN Operation
- Internal or External Character Synchronization
- Transparent or Non-Transparent Mode
- Transparent Mode DLE Stuffing (Tx) and Detection (Rx)
- Automatic SYN or DLE-SYN Insertion
- SYN, DLE, and DLE-SYN Stripping
- Baud Rate : dc to 1Mbps (1×Clock)

Asynchronous Operation

- 1, 1 1/2, or 2 Stop Bits Transmitted
- Parity, Overrun, and Framing Error Detection
- Line Break Detection and Generation
- False Start Bit Detection
- Automatic Serial Echo Mode (Echoplex)
- Baud Rate : dc to 1Mbps (1×Clock)
  dc to 62.5kbps (16×Clock)
  dc to 15.625kbps (64×Clock)

Common Features

- Internal or External Baud Rate Clock ; No System Clock Required
- Three Baud Rate Sets (A, B, C) ; 16 Internal Rates for Each Set
- 5-to 8-Bit Characters Plus Parity ; Odd, Even, or No Parity
- Double Buffered Transmitter and Receiver
- Dynamic Character Length Switching
- Full-or Half-Duplex Operation
- Local or Remote Maintenance Loopback Mode
- TTL-Compatible Inputs and Outputs
- $\overline{\text{RxC}}$ and $\overline{\text{TxC}}$ Pins and Short Circuit Protection
- Three Open-Drain MOS Outputs Can Be Wire ORed
- Single 5-Volt Power Supply

Applications

- Intelligent Terminals
- Network Processors
- Front-End Processors
- Remote Data Concentrators
- Computer-to-Computer Links
- Serial Peripherals
- BISYNC Adaptors

2. OVERVIEW

The EPCI consists of six major sections (see Figure 1).

These are the transmitter, receiver, timing, operation control, modem control, and SYN/DLE control. These sections communicate with each other via an internal data bus and an internal control bus. The internal data bus interfaces to the microprocessor data bus via a data bus buffer.

2.1 OPERATION CONTROL

This functional block stores configuration and operation commands from the CPU and generates appropriate signals to various internal sections to control the overall device operation. It contains read and write circuits to permit communications with the microprocessor via the data bus and contains mode registers 1 and 2, the command register, and the status register. Details of register addressing and protocol are presented in the EPCI programming section of this data sheet.

2.2 TIMING

The EPCI contains a baud-rate generator (BRG) which is programmable to accept external transmit or receive clocks or to divide an external clock to perform data communications. The unit can generate 16 commonly used baud rates, and one of which can be selected for full-duplex operation (see Table 1).

2.3 RECEIVER

The receiver accepts serial data on the RxD pin, converts this serial input to parallel format, checks for bits or characters that are unique to the communication technique, and sends an "assembled" character to the CPU.

2.4 TRANSMITTER

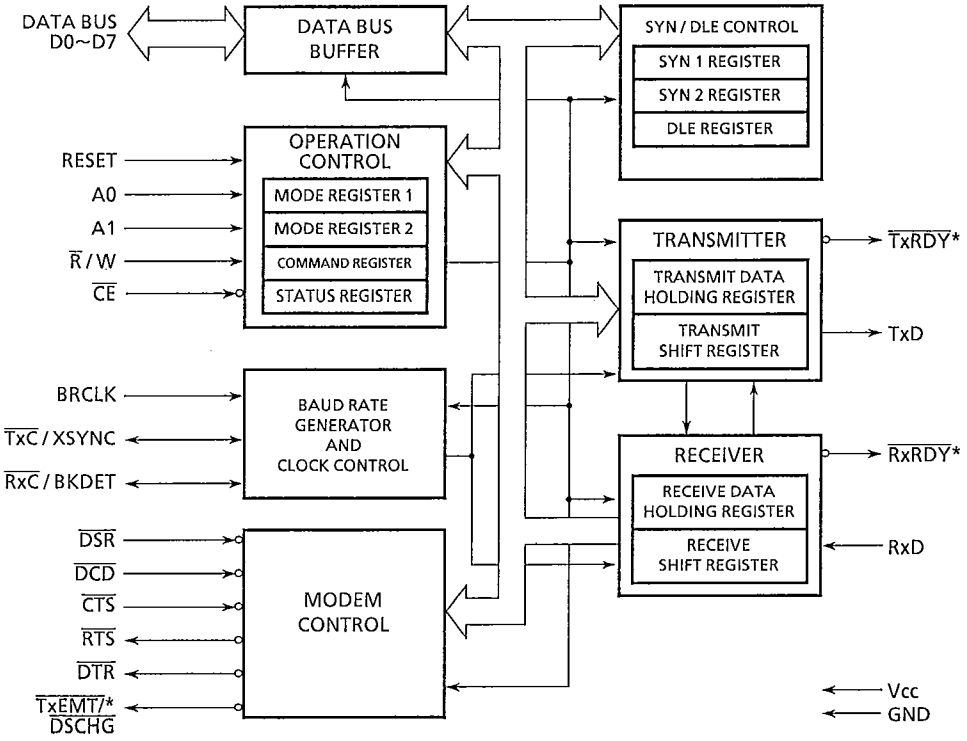
The transmitter accepts parallel data from the CPU, converts it to a serial bit stream, inserts the appropriate characters or bits (based on the communication technique) and outputs a composite serial stream of data on the TxD output pin.

2.5 MODEM CONTROL

The modem control section provides interfacing for three input signals and three output signals used for "handshaking" and status indication between the CPU and a modem.

2.6 SYN/DLE CONTROL

This section contains control circuitry and three 8-bit registers storing the SYN1, SYN2, and DLE characters provided by the CPU. These registers are used in the synchronous mode of operation to provide the characters required for synchronization, idle fill, and data transparency.



* : Open-Drain Output Pin

Figure 2.1 Block Diagram

Table 2.1 Baud-Rate Generator Characteristics

MR23~20	Baud Rate	Actual Frequency 16X Clock	Percent Error	Divisor
Set A (BRCLK = 4.9152 MHz)				
0000	50	0.8kHz	–	6144
0001	75	1.2	–	4096
0010	110	1.7598	– 0.01	2793
0011	134.5	2.152	–	2284
0100	150	2.4	–	2048
0101	200	3.2	–	1536
0110	300	4.8	–	1024
0111	600	9.6	–	512
1000	1050	16.8329	0.196	292
1001	1200	19.2	–	256
1010	1800	28.7438	– 0.19	171
1011	2000	31.9168	– 0.26	154
1100	2400	38.4	–	128
1101	4800	76.8	–	64
1110	9600	153.6	–	32
1111	19200	307.2	–	16
Set B (BRCLK = 4.9152 MHz)				
0000	45.5	0.7279kHz	0.005	6752
0001	50	0.8	–	6144
0010	75	1.2	–	4096
0011	110	1.7598	– 0.01	2793
0100	134.5	2.152	–	2284
0101	150	2.4	–	2048
0110	300	4.8	–	1024
0111	600	9.6	–	512
1000	1200	19.2	–	256
1001	1800	28.7438	– 0.19	171
1010	2000	31.9168	– 0.26	154
1011	2400	38.4	–	128
1100	4800	76.8	–	64
1101	9600	153.6	–	32
1110	19200	307.2	–	16
1111	38400	614.4	–	8
Set C (BRCLK = 5.0688 MHz)				
0000	50	0.8kHz	–	6336
0001	75	1.2	–	4224
0010	110	1.76	–	2880
0011	134.5	2.1523	0.016	2355
0100	150	2.4	–	2112
0101	300	4.8	–	1056
0110	600	9.6	–	528
0111	1200	19.2	–	264
1000	1800	28.8	–	176
1001	2000	32.081	0.253	158
1010	2400	38.4	–	132
1011	3600	57.6	–	88
1100	4800	76.8	–	66
1101	7200	115.2	–	44
1110	9600	153.6	–	33
1111	19200	316.8	3.125	16

Note : 16× clock is used in asynchronous mode. In synchronous mode, clock multiplier is 1× and BRG can be used only for $\overline{TxC}$.

3. SIGNAL DESCRIPTION

This section contains a brief description of the input and output signals. A discussion of bus operation during the various machine cycles and operations is also given.

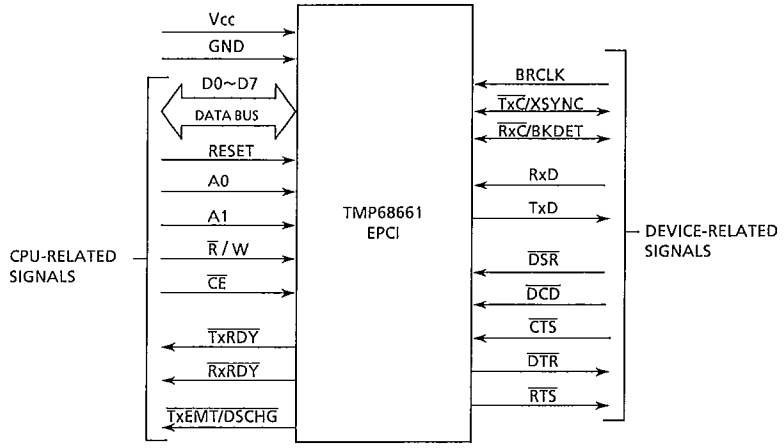


Figure 3.1 Input and Output Signals

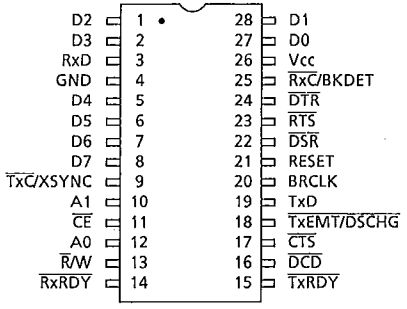


Figure 3.2 Pin Assignments

3.1 CPU-RELATED SIGNALS

The following paragraphs describe the CPU-related signals for the EPCI.

3.1.1 V_{CC} and GND

V_{CC} is the +5 volt power supply input and GND is the ground connection.

3.1.2 Reset (RESET)

When high, this input performs a master reset on the EPCI. This signal asynchronously terminates any device activity and clears the mode, command, and status registers. The device assumes the idle state and remains there until initialized with the appropriate control words.

3.1.3 Address Lines (A0~A1)

The address lines are used to select the internal EPCI registers.

3.1.4 Read/Write ($\overline{R}$/W)

When low, this input signal designates the read command and when high, the write command.

3.1.5 Chip Enable ($\overline{CE}$)

This input is the chip enable command. When low, it indicates that control and data lines to the EPCI are valid and that the operation specified by the $\overline{R}$/W, A0, and A1 inputs should be performed. When high, chip enable places the D0~D7 data bus lines in the three-state condition.

3.1.6 Data Bus (D0~D7)

This 8-bit three-state bidirectional data bus is used to transfer commands, data, and status between the EPCI and the CPU. The D0 bit is the least significant bit ; D7 the most significant bit.

3.1.7 Transmitter Ready ($\overline{TxRDY}$)

This output signal is the complement of status register bit SR0. When low, it indicates that the transmit data holding register (THR) is ready to accept a data character from the CPU. It goes high when the data character is loaded. This output is valid only when the transmitter is enabled. It is an open-drain output which can be used as an interrupt to the CPU.

3.1.8 Receiver Ready ($\overline{\text{RxRDY}}$)

This output is the complement of status register bit SR1. When low, it indicates that the receive data holding register (RHR) has a character ready for input to the CPU. It goes high when the RHR is read by the CPU, and also when the receiver is disabled. It is an open-drain output which can be used as an interrupt to the CPU.

3.1.9 Transmitter Empty ($\overline{\text{TxEMT/DSCHG}}$)

This output is the complement of status register bit SR2. When low, it indicates that the transmitter has completed serialization of the last character loaded by the CPU, or that a change of state of the DSR or DCD inputs has occurred. This output goes high when the status register is read by the CPU, if the $\overline{\text{TxEMT}}$ condition does not exist. Otherwise, the THR must be loaded by the CPU for this line to go high. It is an open-drain output which can be used as an interrupt to the CPU.

3.2 DEVICE-RELATED SIGNALS

The following paragraphs describe the device-related signals for the EPCI.

3.2.1 Baud-Rate Clock (BRCLK)

This is the clock input to the internal baud-rate generator (see Table1). This input is not required if external receiver and transmitter clocks are used.

3.2.2 Receiver Clock ($\overline{\text{RxC}}$/BKDET)

If an external receiver clock is programmed, this input controls the rate at which the character is to be received. Its frequency is 1×, 16×, or 64× the baud rate as programmed by mode register 1. Data are sampled on the rising edge of the clock. If an internal receiver clock is programmed, this pin can be a 1×/16× clock or a break detect output pin.

3.2.3 Transmitter Clock ($\overline{\text{TxC}}$/XSYNC)

If an external transmitter clock is programmed, this input controls the rate at which the character is transmitted. Its frequency is 1×, 16×, or 64× the baud rate, as programmed by mode register 1. The transmitted data changes on the falling edge of the clock. If an internal transmitter clock is programmed, this pin can be a 1×/16× clock output or an external jam synchronization input.

Note: The $\overline{\text{RxC}}$ and $\overline{\text{TxC}}$ outputs have short circuit protection (C_L=100pF maximum). Outputs become open circuited upon detection of a zero pulled high or a one pulled low.

3.2.4 Receive Data (RxD)

This signal is the serial data input to the receiver. "Mark" is high, "space" is low.

3.2.5 Transmit Data (TxD)

This signal is the serial data output to the transmitter. "Mark" is high, "space" is low. The signal will be held in mark condition when the transmitter is disabled.

3.2.6 Data Set Ready ($\overline{\text{DSR}}$)

This general-purpose input can be used for data set ready or ring indicator condition. Its complement appears as status register bit SR7. The DSR input causes a low output on $\overline{\text{TxEMT/DSCHG}}$ when its state changes if CR2 or CR0 equals one.

3.2.7 Data Carrier Detect ($\overline{\text{DCD}}$)

This input must be low in order for the receiver to operate. Its complement appears as status register bit SR6. The $\overline{\text{DCD}}$ input causes a low output on $\overline{\text{TxEMT/DSCHG}}$ when its state changes if CR2 or CR0 equals one. If $\overline{\text{DCD}}$ goes high while receiving, the $\overline{\text{RxC}}$ is internally inhibited.

3.2.8 Clear to Send ($\overline{\text{CTS}}$)

This input must be low in order for the transmitter to operate. If it goes high during transmission, the character in the transmit shift register will be transmitted before termination.

3.2.9 Data Terminal Ready ($\overline{\text{DTR}}$)

This general-purpose output is the complement of command register bit CR1. It is normally used to indicate that the data terminal is ready.

3.2.10 Request to Send ($\overline{\text{RTS}}$)

This general-purpose output is the complement of command register bit CR5. Normally $\overline{\text{RTS}}$ is used to indicate request to send. If the transmit shift register is not empty when CR5 is reset (1 or 0), then $\overline{\text{RTS}}$ will go high one $\overline{\text{TxC}}$ time after the last serial bit is transmitted.

4. OPERATION

The functional operation of the EPCI is programmed by a set of control words supplied by the CPU. These control words specify items such as synchronous or asynchronous mode, baud rate, number of bits per character, etc. The programming procedure is described in the EPCI programming section of this data sheet.

After programming, the EPCI is ready to perform the desired communications functions. The receiver performs serial-to-parallel conversion of data received from a modem or equivalent device. The transmitter converts parallel data received from the CPU to a serial bit stream. These actions are accomplished within the framework specified by the control words.

4.1 RECEIVER

The EPCI is conditioned to receive data when the DCD input is low and the RxEN bit in the command register is true. The asynchronous and synchronous modes of receiver operation are described below.

4.1.1 Asynchronous Mode

In the asynchronous mode, the receiver looks for a high-to-low (mark-to-space) trasnsition of the start bit on the RxD input line. If a transition is detected, the state of the RxD line is sampled again after a delay of one-half of a bit time. If RxD is now high, the search for a valid start bit is begun again. If RxD is still low, a valid start bit is assumed and the receiver continues to sample the input line at one bit time intervals until the proper number of data bits, the parity bit, and one stop bit have been assembled.

The data are then transferred to the receive data holding register, the RxRDY bit in the status register is set, and the $\overline{\text{RxRDY}}$ output is asserted. If the character length is less than eight bits, the high order unused bits in the holding register are set to zero. The parity error, framing error, and overrun error status bits are strobed into the status register on the positive going edge of $\overline{\text{RxC}}$ corresponding to the received character boundary.

If the stop bit is present, the receiver will immediately begin its search for the next start bit. If the stop bit is absent (framing error), the receiver will interpret a space as a start bit if it persists into the next bit time interval.

If a break condition is detected (RxD is low for the entire character as well as the stop bit), only one character consisting of all zeros (with the FE status bit SR5 set) will be transferred to the holding register. The RxD input must return to a high condition before a search for the next start bit begins.

Pin 25 ($\overline{RxC}$/BKDET) can be programmed to be a break detect output by appropriate setting of MR24~MR27. If so, a detected break will cause that pin to go high. When RxD returns to mark for one $\overline{RxC}$ time, pin 25 will go low. Refer to the break-detection timing diagram (Figure 4.3).

4.1.2 Synchronous Mode

When the EPCI is initialized into the synchronous mode, the receiver first enters the hunt mode on a zero-to-one transition of RxEN (CR2). In this mode, as data are shifted into the receiver shift register a bit at a time, the contents of the register are compared to the contents of the SYN1 register. If the two are not equal, the next bit is shifted in and the comparison is repeated. When the two registers match, the hunt mode is terminated and character assembly mode begins.

If single SYN operation is programmed, the SYN DETECT status bit is set. If double SYN operation is programmed, the first character assembled after SYN1 must be SYN2 in order for the SYN DETECT bit to be set. Otherwise, the EPCI returns to the hunt mode. (Note that the sequence SYN1-SYN1-SYN2 will not achieve synchronization.)

When synchronization has been achieved, the EPCI continues to assemble characters and transfer them to the holding register, setting the RxRDY status bit and asserting the $\overline{RxRDY}$ output each time a character is transferred. The PE and OE status bits are set as appropriate. Further receipt of the appropriate SYN sequence sets the SYN DETECT status bit.

If the SYN stripping mode is commanded, SYN characters are not transferred to the holding register. Note that the SYN characters used to establish initial synchronization are not transferred to the holding register in any case.

External jam synchronization can be achieved via pin 9 by appropriate setting of MR27~MR24. When pin 9 is an XSYNC input, the internal SYN1, SYN1-SYN2, and DLE-SYN1 detection is disabled. Each positive going signal on XSYNC will cause the receiver to establish synchronization on the rising edge of the next $\overline{RxC}$ pulse. Chracter assembly will start with the RxD input at this edge. The XSYNC signal may be lowered on the next rising edge of $\overline{RxC}$. This external synchronization will cause the SYN DETECT status bit to be set until the status register is read. Refer to XSYNC timing diagram (Figure 4.2).

4.2 TRANSMITTER

The EPCI is conditioned to transmit data when the CTS input is low and the TxEN command register bit is set. The EPCI indicates to the CPU that it can accept a character for transmission by setting the TxRDY status bit and asserting the $\overline{TxRDY}$ output. When the CPU writes a character into the transmit data holding register, these conditions are negated.

Data are transferred from the holding register to the transmit shift register when it is idle or has completed transmission of the previous character. The $\overline{\text{TxRDY}}$ conditions are then asserted again. Thus, one full character time of buffering is provided. The following paragraphs describe the asynchronous and synchronous modes of operating the transmitter.

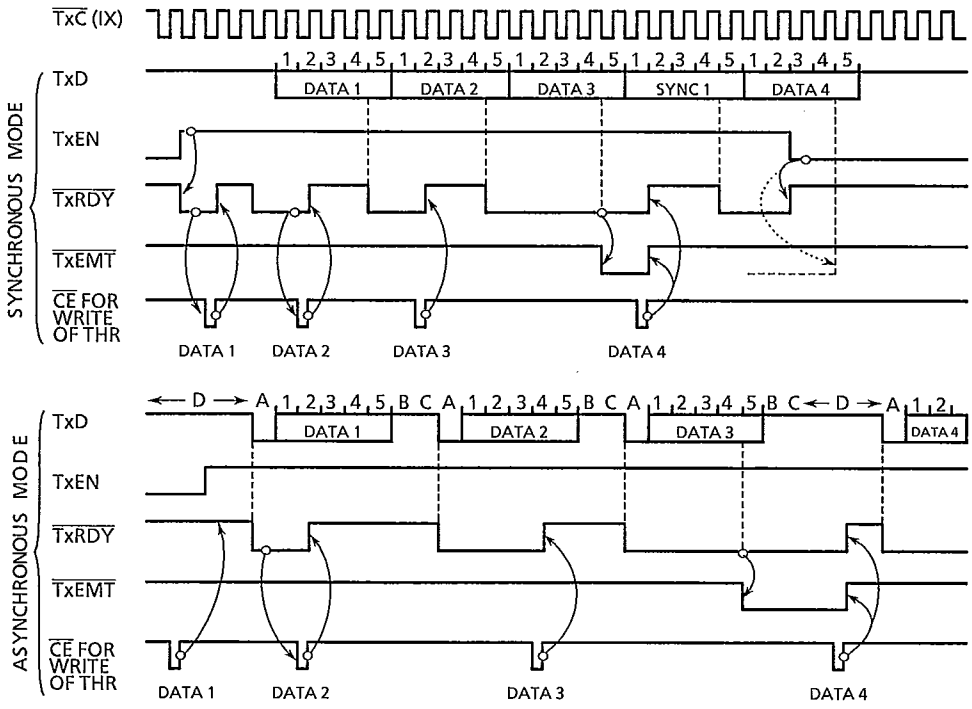
4.2.1 Asynchronous Mode

In the asynchronous mode, the transmitter automatically sends a start bit followed by the programmed number of data bits, the least significant bit being sent first. It then appends an optional odd or even parity bit and the programmed number of stop bits. If following transmission of the data bits, a new character is not available in the transmit holding register, the TxD output remains in the marking (high) condition and the $\overline{\text{TxEMT/DSCHG}}$ output and its corresponding status bit are asserted. Transmission resumes when the CPU loads a new character into the holding register. The transmitter can be forced to output a continuous low (BREAK) condition by setting the send break command bit (CR3) high.

4.2.2 Synchronous Mode

When the EPCI is initially conditioned to transmit in the synchronous mode, the TxD output remains high and the $\overline{\text{TxRDY}}$ condition is asserted until the first character to be transmitted (usually a SYN character) is loadede by the CPU. Subsequent to this, a continuous stream of characters is transmitted. No extra bits (other than parity if commanded) are generated by the EPCI unless the CPU fails to send a new character to the EPCI by the time the transmitter has completed sending the previous character.

Since synchronous communication does not allow gaps between characters, the EPCI asserts $\overline{\text{TxEMT}}$ and automatically "fills" the gap by transmitting SYN1s, SYN1-SYN2 doublets, or DLE-SYN1 doublets depending on the state of MR16 and MR17. Normal transmission of the message resumes when a new character is available in the transmit data holding register. If the SEND DLE bit in the command register is true, the DLE character is automatically transmitted prior to transmission of the message character in the THR.



Note 1 : A = Start Bit ; B = Stop Bit 1 ; C = Stop Bit 2 ; D = TxD Marking Condition.

: The $\overline{\text{TxEMT}}$ signal goes low at the beginning of the last data bit or if parity is enabled, at the beginning of the parity bit.

: This timing diagram is shown for 5-bit characters, no parity, and two stop bits (in asynchronous mode).

Figure 4.1 $\overline{\text{TxRDY}}$ and $\overline{\text{TxEMT}}$ Timing Diagram

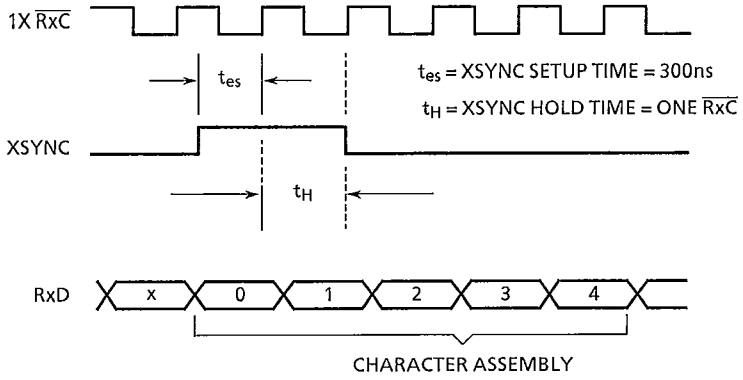
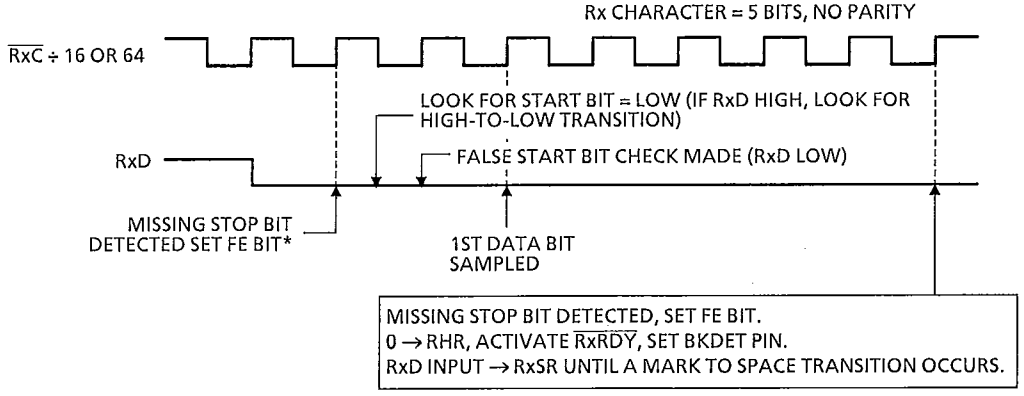
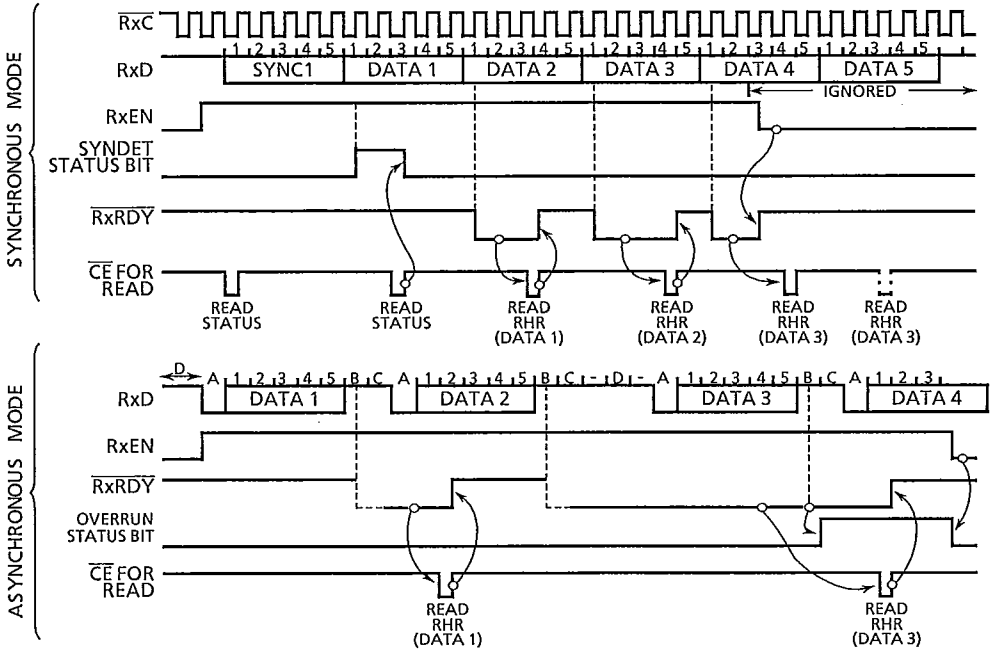


Figure 4.2 External Synchronization with XSYNC Timing Diagram



* If the Stop Bit is present, the Start Bit search will commence immediately.

Figure 4.3 Break Detection Timing Diagram



Note 1 : A=Start Bit; B=Stop Bit1; C=Stop Bit2; D=TxD Marking Condition.
2 : Only one stop bit is detected.
3 : This timing diagram is shown for 5-bit characters, no parity, and two stop bits (in asynchronous mode).

Figure 4.4 $\overline{\text{RxRDY}}$ Timing Diagram

5. EPCI PROGRAMMING

Prior to initiating data communications, the EPCI operating mode must be programmed by performing write operations to the mode and command registers. In addition, if synchronous operation is programmed, the appropriate SYN/DLE registers must be loaded. The EPCI can be reconfigured at any time during program execution. A flowchart of the initialization process is shown in Figure 5.1.

The internal registers of the EPCI are accessed by applying specific signals to the $\overline{CE}$, $\overline{R}/W$, A1, and A0 inputs. The conditions necessary to address each register are shown in Table 5.1.

Table 5.1 Register Addressing

$\overline{CE}$	A1	A0	$\overline{R}/W$	Function
1	×	×	×	Three-State Data Bus
0	0	0	0	Read Receive Holding Register
0	0	0	1	Write Transmit Holding Register
0	0	1	0	Read Status Register
0	0	1	1	Write SYN1/SYN2/DLE Registers
0	1	0	0	Read Mode Registers 1/2
0	1	0	1	Write Mode Registers 1/2
0	1	1	0	Read Command Register
0	1	1	1	Write Command Register

Note : See AC characteristics section for timing requirements.

The SYN1, SYN2, and DLE registers are accessed by performing write operations with the conditions A1=0, A0=1, and $\overline{R}/W=1$. The first operation loads the SYN1 register, the next loads the SYN2 register, and the third loads the DLE register. Reading or loading the mode registers is done in a similar manner.

The first write (or read) operation addresses mode register 1 and a subsequent operation addresses mode register 2. If more than the required number of accesses are made, the internal sequencer recycles to point at the first register. The pointers are reset to SYN1 register and mode register 1 by a RESET input or by performing a read command register operation. The pointers are unaffected by any other read or write operation.

The EPCI register formats are summarized in Tables 5.2, 5.3, 5.4 and 5.6. Mode registers 1 and 2 define the general operational characteristics of the EPCI while the command register controls the operation within this basic framework. The EPCI indicates its status in the status register. These registers are cleared when a RESET input is applied.

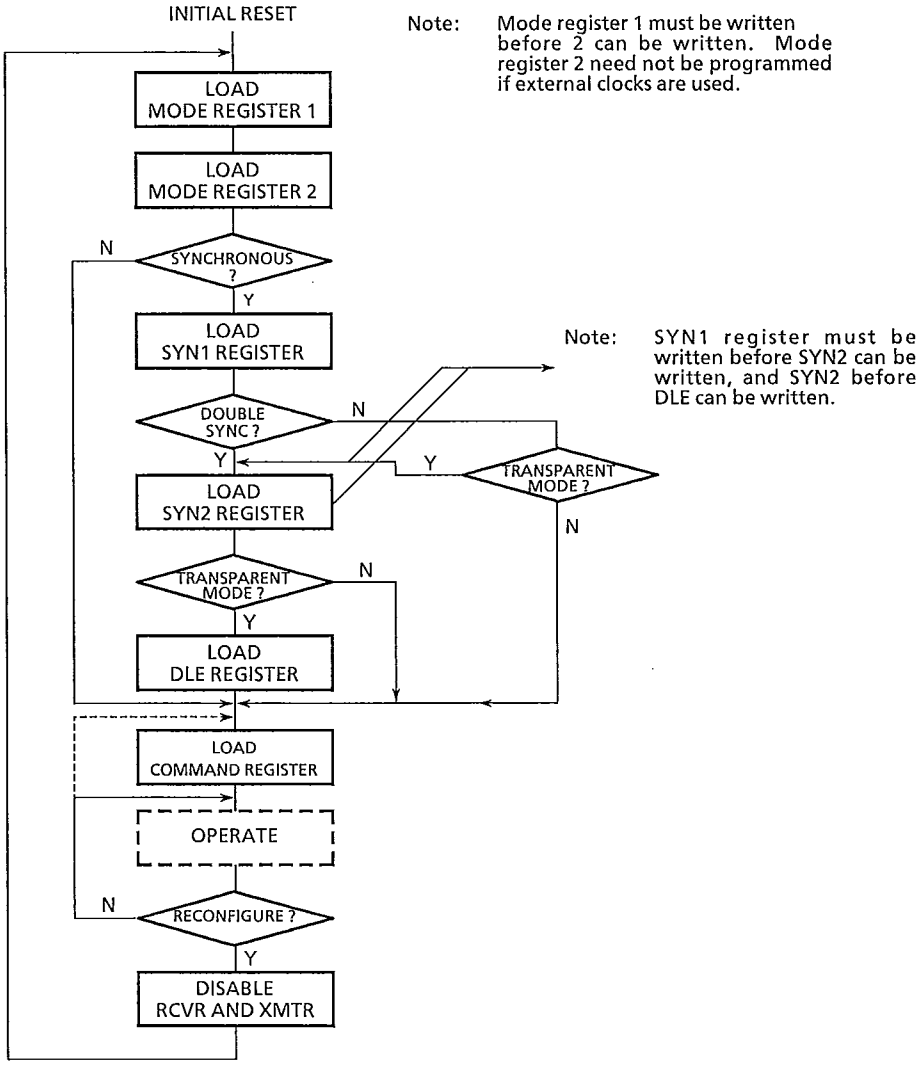


Figure 5.1 Initialization Flowchart

5.1 MODE REGISTER 1 (MR1)

Table5.3 illustrates mode register 1. Bits MR10 and MR11 select the communication format and baud-rate multiplier. The synchronous mode and 1× multiplier is specified by 00. The 1×, 16×, and 64× multipliers are programmable for asynchronous format. However, the multiplier in asynchronous format applies only if the external clock input option is selected by bits MR24 and MR25.

Bits MR12 and MR13 select a character length of 5, 6, 7, or 8bits. The character length does not include the parity bit, if programmed, and does not include the start and stop bits in asynchronous mode.

Bit MR14 controls parity generation. If enabled, a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data. Bit MR15 selects odd or even parity when parity is enabled by MR14.

In asynchronous mode, MR16 and MR17 select character framing of 1, 1.5, or 2 stop bits. If 1× baud rate is programmed, 1.5 stop bits default to 1 stop bit on transmit. In synchronous mode, MR17 controls the number of SYN characters used to establish synchronization and for character fill when the transmitter is idle. The SYN1 register alone is used if MR17 equals one, and SYN1-SYN2 are used when MR17 equals zero.

If the transparent mode is specified by MR16, the DLE-SYN1 registers are used to establish character fill and SYN detect, but the normal synchronization sequence is used to establish character synchronization. When transmitting, a DLE character in the transmit holding register will cause a second DLE character to be transmitted. The DLE stuffing eliminates the software DLE compare and stuff on each transparent mode data character. If the send DLE command (CR3) is active when a DLE is loaded into THR, only one additional DLE will be transmitted. Also DLE stripping and DLE detect (with MR14 = 0) are enabled.

The bits in the mode register affecting character assembly and disassembly (MR12 through MR16) can be changed dynamically (during the active receive/transmit operation). The character mode register affects both the transmitter and receiver ; therefore in synchronous mode, changes should be made only in half-duplex mode (when either RxEN or TxEN equals one but not when both simultaneously equal one). In asynchronous mode, character changes should be made when RxEN and TxEN equal zero or when TxEN equals one and the transmitter is marking in half-duplex mode (RxEN equals 0).

To effect assembly/disassembly of the next received/transmitted character, MR12 through MR15 must be changed within n bit times of the active going state of $\overline{\text{RxRDY/TxRDY}}$. Transparent and non-transparent mode changes (MR16) must occur within n − 1 bit times of the character to be affected when the receiver or transmitter is active (n = smaller of the new and old character lengths).

5.2 MODE REGISTER 2 (MR2)

Table5.3 illustrates mode register 2. Bits MR20, MR21, MR22, and MR23 control the frequency of the internal baudrate generator (BRG). Sixteen rates are selectable for each EPCI version (A, B, C). Versions A and B specify a 4.9152MHz TTL input at BRCLK (pin20) ; version C specifies a 5.0688MHz input.

Bits MR20~MR23 are "don't cares" if external clocks are selected (MR24 and MR25 equal zero). The individual rates are given in Table 1. Bits MR24~MR27 select the receive and transmit clock source (either the BRG or an external input) and the function at the $\overline{\text{TxC}}$/XSYNC and $\overline{\text{RxC}}$/BKDET pins (see Table 5.3).

5.3 COMMAND REGISTER

Table5.4 illustrates the command register. Bits CR0 (TxEN) and CR2 (RxEN) enable or disable the transmitter and receiver respectively. A zero-to-one transition of CR2 forces start bit search (asynchronous) or hunt mode (synchronous) on the second $\overline{\text{RxC}}$ rising edge.

Disabling the receiver causes $\overline{\text{RxRDY}}$ to go high (inactive). If the transmitter is disabled, it will complete the transmission of the character in the transmit shift register (if any) prior to terminating operation. The TxD output will then remain in the marking state (high) while $\overline{\text{TxRDY}}$ and $\overline{\text{TxEMT}}$ will go high (inactive). If the receiver is disabled, it will terminate operation immediately. Any character being assembled will be neglected. A zero to one transition of CR2 will initiate start bit search (asynchronous) or hunt mode (synchronous).

Bits CR1 (DTR) and CR5 (RTS) control the $\overline{\text{DTR}}$ and $\overline{\text{RTS}}$ outputs. Data at the outputs are the logical complement of the register data. In asynchronous mode, setting CR3 will force and hold the TxD output low (spacing condition) at the end of the current transmitted character. Normal operation resumes when CR3 is cleared. The TxD line will go high for at least one bit time before beginning transmission of the next character in the transmit data holding register.

In synchronous mode, setting CR3 causes the transmission of the DLE register contents prior to sending the character in the transmit data holding register. Since this is a one time command, CR3 does not have to be reset by software. The CR3 bit should be set when entering and exiting transparent mode and for all DLE/non-DLE character sequences.

Setting CR4 causes the error flags in the status register (SR3, SR4, and SR5) to be cleared. This is a one time command. There is no internal latch for this bit.

When CR5 (RTS) is set, the $\overline{\text{RTS}}$ pin is forced low and the transmit serial logic is enabled. A one-to-zero transition of CR5 will cause RTS to go high (inactive) one $\overline{\text{TxC}}$ time after the last serial bit has been transmitted (if the transmit shift register was not empty).

The EPCI can operate in one of the four submodes described below with each major mode (synchronous or asynchronous). The operational submode is determined by CR7 and CR6. If CR7 and CR6 equal 00, the normal mode is operational with the transmitter and receiver operating independently in accordance with the mode and status register instructions.

5.4 STATUS REGISTER

The data contained in the status register (see Table5.4) indicate receiver and transmitter conditions and modem/data set status.

The SR0 bit is the transmitter ready (TxRDY) status bit. It, and its corresponding output, are valid only when the transmitter is enabled. If equal to zero, it indicates that the transmit data holding register has been loaded by the CPU and the data has not been transferred to the transmit shift register. If set equal to one, it indicates that the holding register is ready to accept data from the CPU.

The SR0 bit is initially set when the transmitter is enabled by CR0, unless a character has previously been loaded into the holding register. It is not set when the automatic-echo or remote loopback modes are programmed. When this bit is set, the $\overline{\text{TxRDY}}$ output pin is low. In the automatic-echo and remote loopback modes, the output is held high.

The receiver ready (RxRDY) status bit, SR1, indicates the condition of the receive data holding register. If set, it indicates that a character has been loaded into the holding register from the receive shift register and is ready to be read by the CPU. If equal to zero, there is no new character in the holding register. This bit is cleared when the CPU reads the receive data holding register or when the receiver is disabled by CR2. When set, the $\overline{\text{RxRDY}}$ output is low.

The TxEMT/DSCHG bit, SR2, when set, indicates either a change of state of the $\overline{\text{DSR}}$ or $\overline{\text{DCD}}$ inputs (when CR2 or CR0 equals one) or that the transmit shift register has completed transmission of a character and no new character has been loaded into the transmit data holding register. Note that in synchronous mode, this bit will be set even though the appropriate "fill" character is transmitted.

The $\overline{\text{TxEMT}}$ output will not go active until at least one character has been transmitted. It is cleared by loading the transmit data holding register. The $\overline{\text{DSCHG}}$ condition is enabled when either TxEN or RxEN equals one. It is cleared when the status register is read by the CPU. If the status register is read twice and SR2 equals one, when SR6 and SR7 remain unchanged, then a $\overline{\text{TxEMT}}$ condition exists. When SR2 is set, the $\overline{\text{TxEMT/DSCHG}}$ output is low.

The SR3 bit, when set, indicates a received parity error when parity is enabled by MR14. In synchronous transparent mode (MR16 equals one) with parity disabled, SR3 indicates that a character matching DLE register was received and the present character is neither SYN1 nor DLE. This bit is cleared when the next character following the above sequence is loaded into RHR, when the receiver is disabled, or when a reset error command (CR4) is received.

The overrun error status bit, SR4, indicates that the previous character loaded into the receive holding register was not read by the CPU at the time a new received character was tramsferred into it. This bit is cleared when the receiver is disabled or by the reset error command, CR4.

In asynchronous mode, the SR5 bit signifies that the received character was not framed by a stop bit, i.e., only the first stop bit is checked. If RHR equals zero when SR5 equals one, a break condition is present. In synchronous nontransparent mode (MR16 equals zero), SR5 indicates receipt of the SYN1 character in single SYN mode or the SYN1-SYN2 pair in double SYN mode. In synchronous transparent mode (MR16 equals one), this bit is set upon detection of the initial synchronizing characters (SYN1 or SYN1-SYN2) and, after synchronization has been achieved, when a DLE-SYN1 pair is received. The SR5 bit is reset when the receiver is disabled, when the reset error command is given in asynchronous mode, or when the status register is read by the CPU in the synchronous mode.

The SR6 and SR7 bits reflect the conditions of the $\overline{DCD}$ and $\overline{DSR}$ inputs respectively. A low input sets the corresponding status bit and a high input clears it.

Table 5.2 Mode Register 1 (MR1)

<table>
<tr><th colspan="2">MR17 MR16</th><th>MR15</th><th>MR14</th><th>MR13 MR12</th><th>MR11 MR10</th></tr>
<tr><td colspan="2">Sync/Async</td><td>Parity Type</td><td>Parity Control</td><td>Character Length</td><td>Mode and Baud Rate Factor</td></tr>
<tr><td colspan="2">Async : Stop Bit Length
00 = Invalid
01 = 1 Stop Bit
10 = 1 1/2 Stop Bits
11 = 2 Stop Bits</td><td rowspan="2">0 = Odd
1 = Even</td><td rowspan="2">0 = Disabled
1 = Enabled</td><td rowspan="2">00 = 5 Bits
01 = 6 Bits
10 = 7 Bits
11 = 8 Bits</td><td rowspan="2">00 = Synchronous 1 x Rate
01 = Asynchronous 1 x Rate
10 = Asynchronous 16 x Rate
11 = Asynchronous 64 x Rate</td></tr>
<tr><td>Sync :
Number of
SYN Char
0 = Double SYN
1 = Single SYN</td><td>Sync :
Transparency
Control
0 = Normal
1 = Transparent</td></tr>
</table>

Note : Baud rate factor in asynchronous applies only if external clock is selected. Factor is 16X if internal clock is selected. Mode must be selected (MR11, MR10) in any case.

Table 5.3 Mode Register 2 (MR2)

MR27-MR24										MR23-MR20
	TxC	RxC	Pin 9	Pin 25		TxC	RxC	Pin 9	Pin 25	Baud Rate Selection
0000	E	E	$\overline{TxC}$	$\overline{RxC}$ (Async or Sync)	0000	E	E	XSYNC1	$\overline{RxC/TxC}$ (Sync)	
0001	E	I	$\overline{TxC}$	×1 (Async or Sync)	0001	E	I	TxC	BKDET (Async)	
0010	I	E	×1	$\overline{RxC}$ (Async or Sync)	0010	I	E	XSYNC1	$\overline{RxC}$ (Sync)	
0011	I	I	×1	×1 (Async or Sync)	0011	I	I	×1	BKDET (Async)	See Baud Rates in Table 1
0100	E	E	$\overline{TxC}$	$\overline{RxC}$ (Async or Sync)	0100	E	E	XSYNC1	$\overline{RxC/TxC}$ (Sync)	
0101	E	I	$\overline{TxC}$	×16 (Async or Sync)	0101	E	I	TxC	BKDET (Async)	
0110	I	E	×16	$\overline{RxC}$ (Async or Sync)	0110	I	E	SCYNC1	$\overline{RxC}$ (Sync)	
0111	I	I	×16	×16 (Async or Sync)	0111	I	I	×16	BKDET (Async)	

Notes: 1. When pin 9 is programmed as XSYNC input, SYN1-SYN2, and DLE-SYN1 detection is disabled.
E = External clock
I = Internal clock (BRG)
1X and 16X are clock outputs

Table 5.4 Command Register (CR)

CR7 CR6	CR5	CR4	CR3	CR2	CR1	CR0
Operating Mode	Request To Send	Reset Error	Sync/Async	Receive Control (RxEN)	Data Terminal Ready	Transmit Control (TxEN)
00 = Normal Operation 01 = Async : Automatic Echo Mode Sync : SYN and/or DLE Stripping Mode 10 = Local Loopback 11 = Remote Loopback	0 = Force $\overline{RTS}$ Output High One Clock Time After TxSR Serialization 1 = Force $\overline{RTS}$ Output Low	0 = Normal 1 = Reset Error Flags in Status Register (FE, OE, PE/DLE Detect)	Async : Force Break 0 = Normal 1 = Force Break	0 = Disable 1 = Enable	0 = Force $\overline{DTR}$ Output High 1 = Force $\overline{DTR}$ Output Low	0 = Disable 1 = Enable
			Sync : Send DLE 0 = Normal 1 = Send DLE			

Table 5.5 Status Register (SR)

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
Data Set Ready	Data Carrier Detect	FE / SYNC Detect	Overrun	PE / DLE Detect	TxEMT / DSCHG	RxRDY	TxRDY
0 = $\overline{DSR}$ Input is High 1 = $\overline{DSR}$ Input is Low	0 = $\overline{DCD}$ Input is High 1 = $\overline{DCD}$ Input is Low	Async : 0 = Normal 1 = Framing Error	0 = Normal 1 = Overrun Error	Async : 0 = Normal 1 = Parity Error	0 = Normal 1 = Change in $\overline{DSR}$, or $\overline{DCD}$, or Transmit Shift Register is Empty	0 = Receive Holding Register Empty 1 = Receive Holding Register Has Data	0 = transmit Holding Register Busy 1 = Transmit Holding Register Empty
		Sync : 0 = Normal 1 = SYN Detected		Sync : 0 = Normal 1 = Parity Error or DLE Received			

5.5 AUTOMATIC-ECHO SUBMODE

In asynchronous mode with CR7 and CR6 equal to 01, the EPCI is placed in the automatic-echo mode. Clocked, regenerated received data is automatically directed to the TxD line while normal receiver operation continues. The receiver must be enabled (CR2 equals one), but the transmitter need not be enabled. The CPU-to-receiver communication continues normally, but the CPU-to-transmitter link is disabled. Only the first character of a break condition is echoed. The TxD output will go high until the next valid start is detected. The following conditions are true while in automatic-echo mode :

1. Data assembled by the receiver are automatically placed in the transmit holding register and retransmitted by the transmitter on the TxD output.
2. The transmitter is clocked by the receive clock.
3. The $\overline{TxRDY}$ output equals one.
4. The $\overline{TxEMT/DSCHG}$ pin will reflect only the data set change condition.
5. The TxEN command (CR0) is ignored.

5.6 AUTOMATIC SYN/DLE STRIPPING SUBMODE

In synchronous mode with CR7 and CR6 equal to 01, the EPCI is placed in the automatic SYN/DLE stripping mode. The exact action taken depends on the setting of the MR16 and MR17 bits.

1. In the nontransparent single SYN mode (MR17 and MR16 equal 10), characters in the data stream matching SYN1 are not transferred to the receive data holding register (RHR).

2. In the nontransparent double SYN mode (MR17 and MR16 equal 00), characters in the data stream matching SYN1 or SYN2 (if immediately preceded by SNY1) are not transferred to the RHR.

3. In transparent mode (MR16 equals one), characters in the data stream matching DLE or SYN1 (if immediately preceded by DLE) are not transferred to RHR. However, only the first DLE of a DLE-DLE pair is stripped.

Note that the automatic stripping mode does not affect the setting of the DLE detect and SYN detect status bits (SR3 and SR5).

5.7 DIAGNOSTIC SUBMODES

Two diagnostic sub-modes (local loopback and remote loopback) can also be configured. These submodes are described below.

5.7.1 Local Loopback Mode

—In local loopback mode (CR7 and CR6 equal 10), the following loops are connected internally :

1. The transmitter output is connected to the receiver input.
2. The $\overline{\text{DTR}}$ output is connected to $\overline{\text{DCD}}$ input and $\overline{\text{RTS}}$ output is connected to $\overline{\text{CTS}}$ input.
3. The receiver is clocked by the transmit clock.
4. The $\overline{\text{DTR}}$, $\overline{\text{RTS}}$, and TxD outputs are held high.
5. The $\overline{\text{CTS}}$, $\overline{\text{DCD}}$, $\overline{\text{DSR}}$, and $\overline{\text{RxD}}$ inputs are ignored.

Additional requirements to operate in the local loopback mode are that CR0 (TxEN), CR1 (DRT), and CR5 (RTS) must be set to one. The CR2 (RxEN) bit is ignored by the EPCI.

5.7.2 Remote Loopback Submode

—The second diagnostic mode is the remote loopback mode (CR6 and CR7 equal 11). In this mode :

1. Data assembled by the receiver are automatically placed in the transmit holding register and retransmitted by the transmitter on the TxD output.
2. The transmitter is clocked by the receive clock.
3. No data are sent to the local CPU, but the error status conditions (PE, OE, FE) are set.
4. The $\overline{\text{RxRDY}}$, $\overline{\text{TxRDY}}$, and $\overline{\text{TxEMT/DSCHG}}$ outputs are held high.
5. The CR1 (TxEN) bit is ignored.
6. All other signals operate normally.

6. INTERFACE REQUIREMENTS

6.1 TMP68000 MPU-TO-EPCI INTERFACE REQUIREMENTS

The circuit shown in Figure 6.1 interfaces the EPCI to the TMP68000 MPU. The 8-bit data bus of the EPCI is connected to the low order eight bits of the MPU data bus (D0~D7). Because of this, the EPCI's registers are addressed on odd byte boundaries and so address line A1 of the MPU is connected to the A0 address line of the EPCI. Similarly, A2 of the MPU is connected to A1 of the EPCI. The R/$\overline{W}$ pin on the TMP68000 is inverted and connected to the $\overline{R}$/W pin of the EPCI.

The $\overline{CE}$ signal must be generated for the EPCI and the $\overline{DTACK}$ signal must be supplied to the MPU. To allow for the data setup time on a read of the EPCI, $\overline{CE}$ must be delayed one-half clock cycle and $\overline{DTACK}$ generated on the next rising edge of the system clock. This causes the processor to insert one wait state in the bus cycle.

In addition to this, $\overline{CE}$ must not be reasserted until the chip enable period t_{CE} has expired. Since some instructions on the TMP68000 can cause access to consecutive addresses on consecutive bus cycles, e.g., MOVEP, an INHIBIT signal must be generated to hold off an access during this period.

A state machine consisting of a SN74LS161 binary counter and a SN74LS74 D flip-flop is configured as a digital "one shot". The rising edge of $\overline{CE}$ starts the counter which times out after a given number of clock cycles. Since t_{CE} is 600ns, a minimum of five clock cycles at 8MHz (625ns) is required. The timing for two consecutive read bus cycles is shown in Figure6.2. The INHIBIT signal prevents $\overline{CE}$ from being generated and $\overline{DTACK}$ from being asserted, causing the processor to generate wait states until INHIBIT is negated.

6.2 8-bit MPU-TO-EPCI INTERFACE REQUIREMENTS

8-bit microprocessors can be easily interfaced to the EPCI as shown in Figure 6.3.

6.3 TYPICAL APPLICATIONS

Some typical applications using the EPCI are shown in Figures 6.4~6.7.

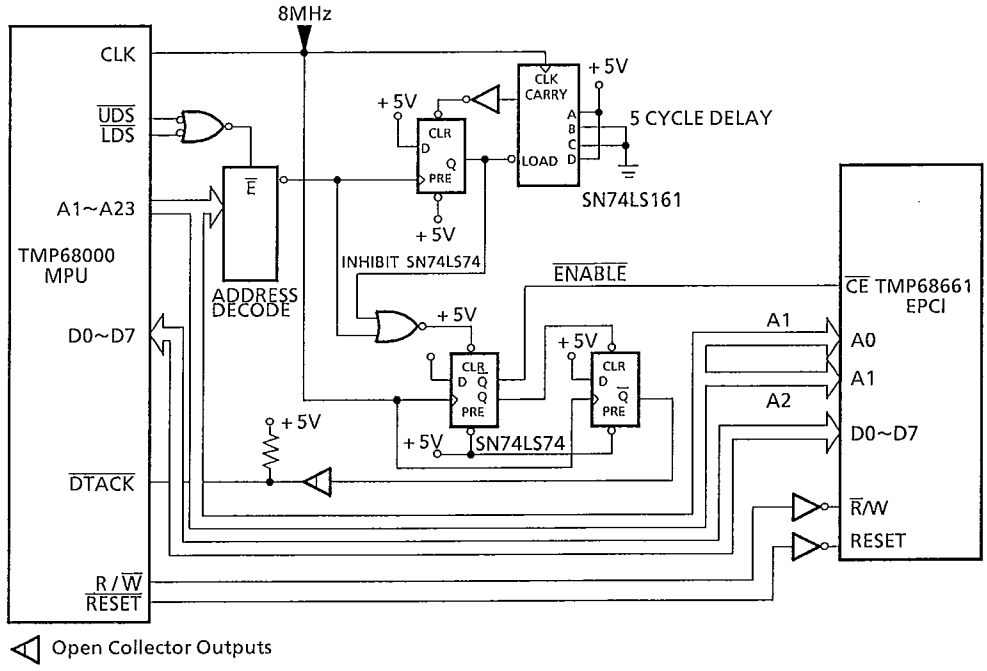
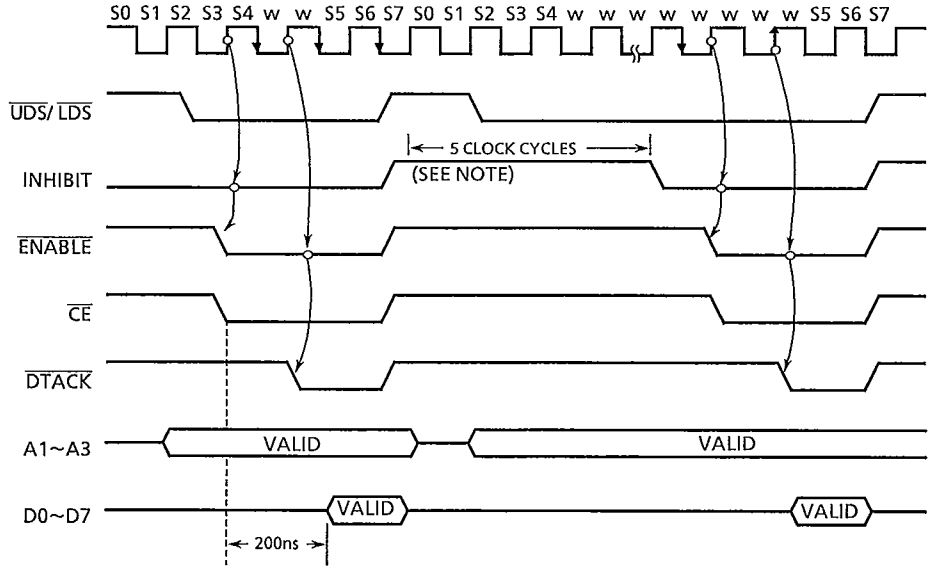


Figure 6.1 Example of TMP68000-to-EPCI Interface Circuit



Note : Insertion of inhibit period delays next read cycler for five clock cycles

Figure 6.2 TMP68000-to-EPCI Read Bus Cycle Timing

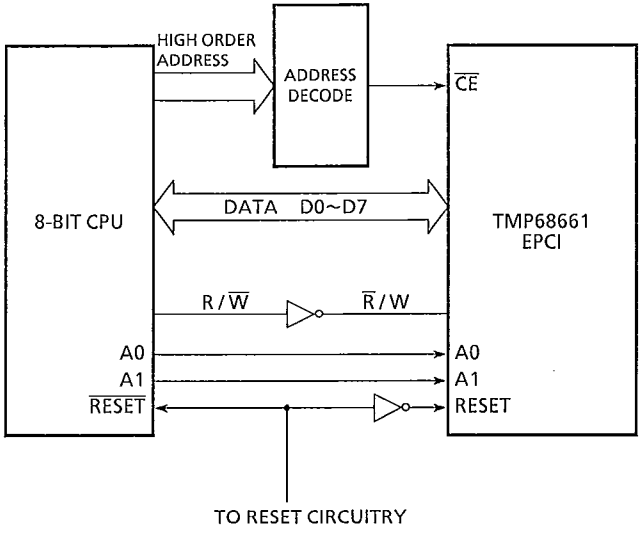


Figure 6.3 Interface Connections to 8-BIT CPU

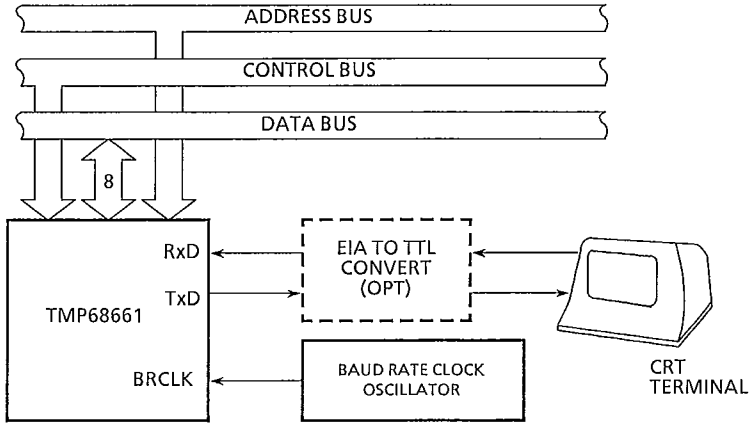


Figure 6.4 Asynchronous Interface to CRT Terminal

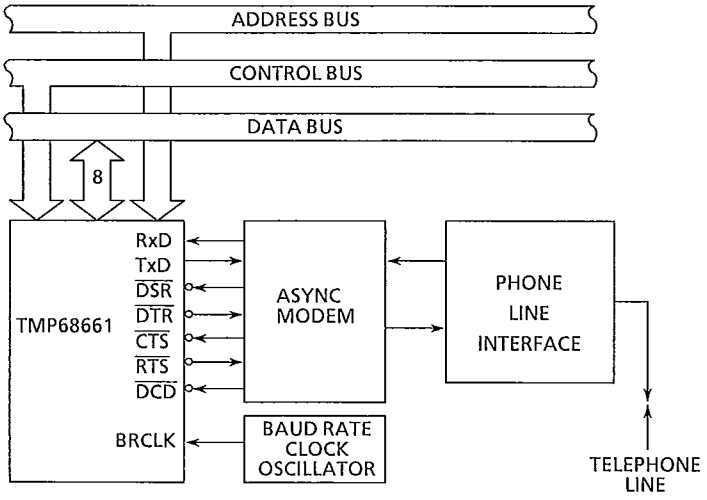


Figure 6.5 Asynchronous Interface to Telephone Lines

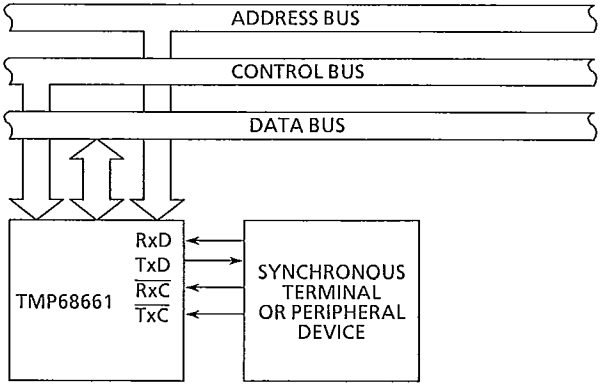


Figure 6.6 Synchronous Interface to Terminal or Peripheral Device

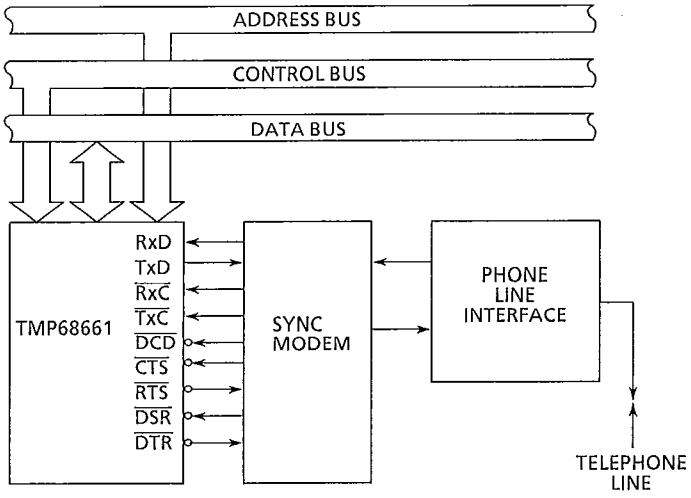


Figure 6.7 Synchronous Interface to Telephone Lines

7. ELECTRICAL SPECIFICATIONS

7.1 MAXIMUM RATINGS

Ratings	Symbol	Value	Unit
Operating Ambient Temperature Range	T_a	0 to + 70	°C
Storage Temperature Range	T_{stg}	− 55 to + 150	°C
All Input Voltages	V_{in}	− 0.3 to + 7.0	V

The device contains circuitry to protect the inputs against damage due to high static voltages or electric fields ; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range GND ≦ (V_{in} or V_{out}) ≦ V_{CC}.

7.2 DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 5%, GND = 0V, Ta = 0~70°C)

Characteristics	Symbol	Min	Max	Unit
Input High Voltage	V_{IH}	2.0	V_{CC}	V
Input Low Voltage	V_{IL}	− 0.3	0.8	V
Output High Voltage (I_{OH} = − 400μA) (see Note)	V_{OH}	2.4	−	V
Output Low Voltage (I_{OL} = 2.2mA)	V_{OL}	−	0.4	V
Input Leakage Current (V_{in} = 0 to 5.5V)	I_{IL}	−	10	μA
Output Leakage Current, 3-State (V_{out} = 0 to 5.25V) Data Bus Low Data Bus High	 I_{LL} I_{LH}	 − −	 10 10	μA
Power Supply Current	I_{CC}	−	150	mA
Power Dissipation	P_D	−	800	mW
Capacitance (Ta = 25°C, Vcc = 0V) Input (V_{in} = V_{out} = 0V) Output (f_c = 1MHz) Input/Output (Unmeasured Pins Tied to Ground)	 C_{in} C_{out} $C_{I/O}$	 − − −	 20 20 20	pF

Note : $\overline{\text{TxRDY}}$, $\overline{\text{RxRDY}}$, and $\overline{\text{TxEMT/DSCHG}}$ outputs are open drain.

7.3 AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 5%, GND = 0V, Ta = 0~70°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Pulse Width, Reset	t_{RES}	1000	–	–	ns
Pulse Width, Chip Enable	t_{CE}	250	–	–	ns
Address Setup Time	t_{AS}	10	–	–	ns
Address Hold Time	t_{AH}	10	–	–	ns
$\overline{R}$ / W Control Setup Time	t_{CS}	10	–	–	ns
$\overline{R}$ / W Control Hold Time	t_{CH}	10	–	–	ns
Data Setup time for Write	t_{DS}	150	–	–	ns
Data Hold Time for Write	t_{DH}	0	–	–	ns
Receive Data Setupt Time	t_{RS}	300	–	–	ns
Receive Data Hold Time	t_{RH}	350	–	–	ns
Data Delay Time for Read (C_L = 150pF)	t_{DD}	–	–	200	ns
Data Bus Floating Time for Read (CL = 150pF)	t_{DF}	–	–	100	ns
$\overline{CE}$ to $\overline{CE}$ Delay Time	t_{CED}	600	–	–	ns
Input Clock Frequency, Baud-Rate Generator TMP68661A, B TMP68661C	f_{BRG}	 1.0 1.0	 4.1952 5.0688	 4.9202 5.0738	MHz
Input Clock Frequency, $\overline{TxC}$ or $\overline{RxC}$ (see Note 1)	$f_{R/T}$	dc	–	1.0	MHz
Clock Width, Baud Rate High (see Note 2) TMP68661A, B TMP68661C	t_{BRH}	 75 70	 – –	 – –	ns
Clock Width, Baud Rate Low (see Note 2) TMP68661A, B TMP68661C	t_{BRL}	 75 70	 – –	 – –	ns
Clock Width, $\overline{TxC}$ or $\overline{RxC}$ High	$t_{R/TH}$	480	–	–	ns
Clock Width, $\overline{TxC}$ or $\overline{RxC}$ Low (see Note 1)	$t_{R/TL}$	480	–	–	ns
TxD Delay from Falling Edge of TxC (CL = 150pF)	t_{TXD}	–	–	650	ns
Skew Between TxD Changing and Falling Edge of TxC Output (CL = 150pF) (see Note 3)	t_{TCS}	–	0	–	ns

Note 1 : In asynchronous local loopback mode, using teh X1 clock, the following parameters apply : $f_{R/T}$ = 0.83MHz maximum ; $t_{R/TL}$ = 700ns minimum.

2 : Under test conditions of 5.0688MHz f_{BRG} (TMP68661C) and 4.9152MHz f_{BRG} (TMP68661A, B), f_{BRH} and t_{BRL} are measured at V_{III} and V_{IL} respectively.

3 : Parameter applies when internal transmitter clock is used.

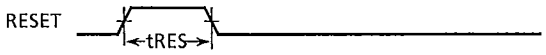


Figure 7.1 RESET Timing Diagram

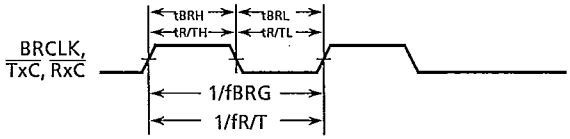


Figure 7.2 Clock Timing Diagram

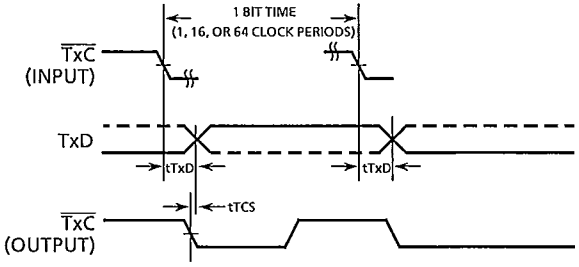


Figure 7.3 Transmit Timing Diagram

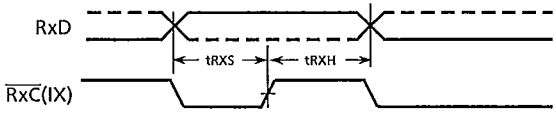


Figure 7.4 Receive Timing Diagram

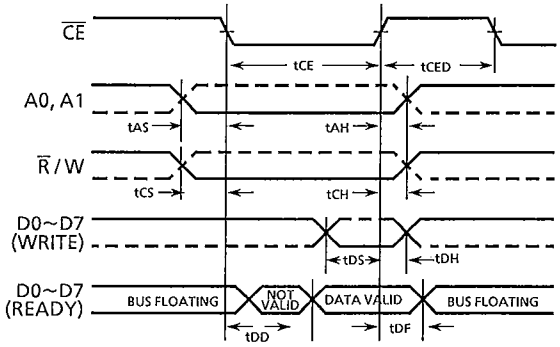
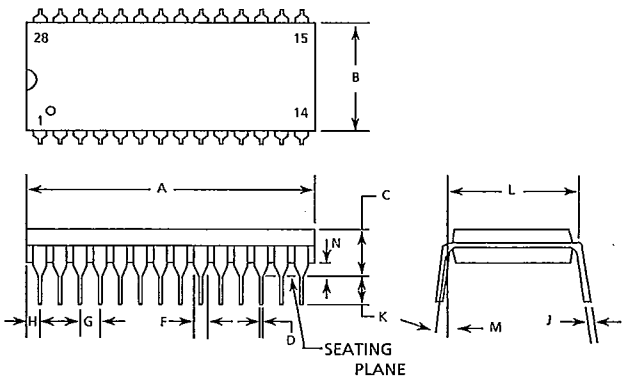


Figure 7.5 Read and Write Timing Diagram

8. MECHANICAL DATA

8.1 PACKAGE DIMENSIONS

PLASTIC PACKAGE



Unit : mm

Dim	Min	Max
A	36.45	37.21
B	13.72	14.22
C	3.94	5.08
D	0.36	0.56
F	1.02	1.52
G	2.54BSC	
H	1.65	2.16
J	0.20	0.38
K	2.92	3.43
L	15.24BSC	
M	0°	15°
N	0.51	1.02