PRELIMINARY DATA SHEET

NEC

BIPOLAR ANALOG INTEGRATED CIRCUIT
μPC2505

45 W AF POWER AMPLIFIER

The μPC2505, a power amplifier IC dedicated for BTL (Balanced Transformer Less), has been designed for car audio equipment. The μPC2505 integrates a stand-by switch circuit that can select amplifier operation mode and stand-by mode upon receipt of an external control signal, from a microcomputer, for instance.

The μPC2505 upgrades the μPC2500:

Less shock noise when the relative error of NF (Negative feedback) capacitor is large.

Less shutdown at overvoltage of input signal.

FEATURES

- Internal stand-by switch circuit; CMOS drive possible
- Can be used as OCL-BTL connection
- High output power: P_O = 45 W TYP. (at V_{CC} = 14.4 V, R_L = 2 Ω, THD = 10 %)
  P_O = 40 W TYP. (at V_{CC} = 13.2 V, R_L = 2 Ω, THD = 10 %)
- Low impedance load drive performance: Up to 2 Ω load
- Low distortion rate: THD = 0.03 % TYP. (at V_{CC} = 13.2 V, R_L = 2 Ω, P_O = 8 W, f = 1 kHz)
- High slew rate: 8.9 V/μs TYP. (at V_{CC} = 13.2 V, R_L = 2 Ω, V_{IN} = 0.5 V_{p-p})
- Small pop noise
- Low circuit current at stand-by: 10 μA or less (at V_{CC} = 13.2 V)
- Low output offset voltage: V_{offset} = 150 mV MAX.
- Following protection circuits are included:
  - Overvoltage, surge protection circuit
  - Thermal shut down protection circuit
  - ASO protection circuit (Output pin short circuit protection (V_{CC} to output pin, output pin to GND, output pin to output pin), Loudspeaker protection)
- High resistance to output pin short circuit

ORDERING INFORMATION

Part Number	Package	Quality Grade
μPC2505H	12-pin plastic power SIP (L)	Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

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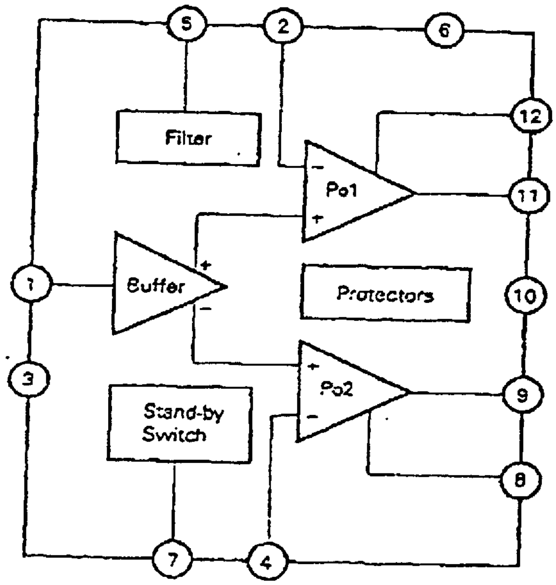
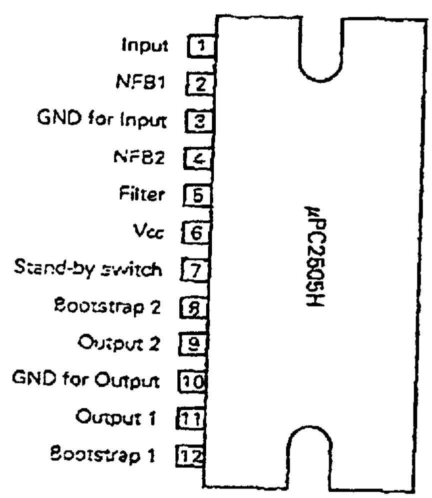
BLOCK DIAGRAM



PIN CONFIGURATION (Top View)



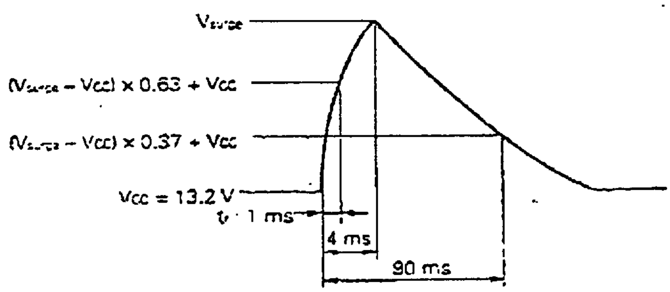
CONTENTS

1. ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (at T_a = 25 °C)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage (Surge)	$V_{CC(surge)}$		60 Note	V
Supply voltage (No signal)	V_{CC1}		25	V
Supply voltage (Operational)	V_{CC2}		18	V
Output current (Instantaneous)	I_O		8	A
Power dissipation	P_D		50	W
Operating Temperature	T_{opt}		−30 to +85	°C
Storage Temperature	T_{stg}		−40 to +150	°C

Note The surge pulse waveform is shown in the following figure.



Surge Pulse Waveform

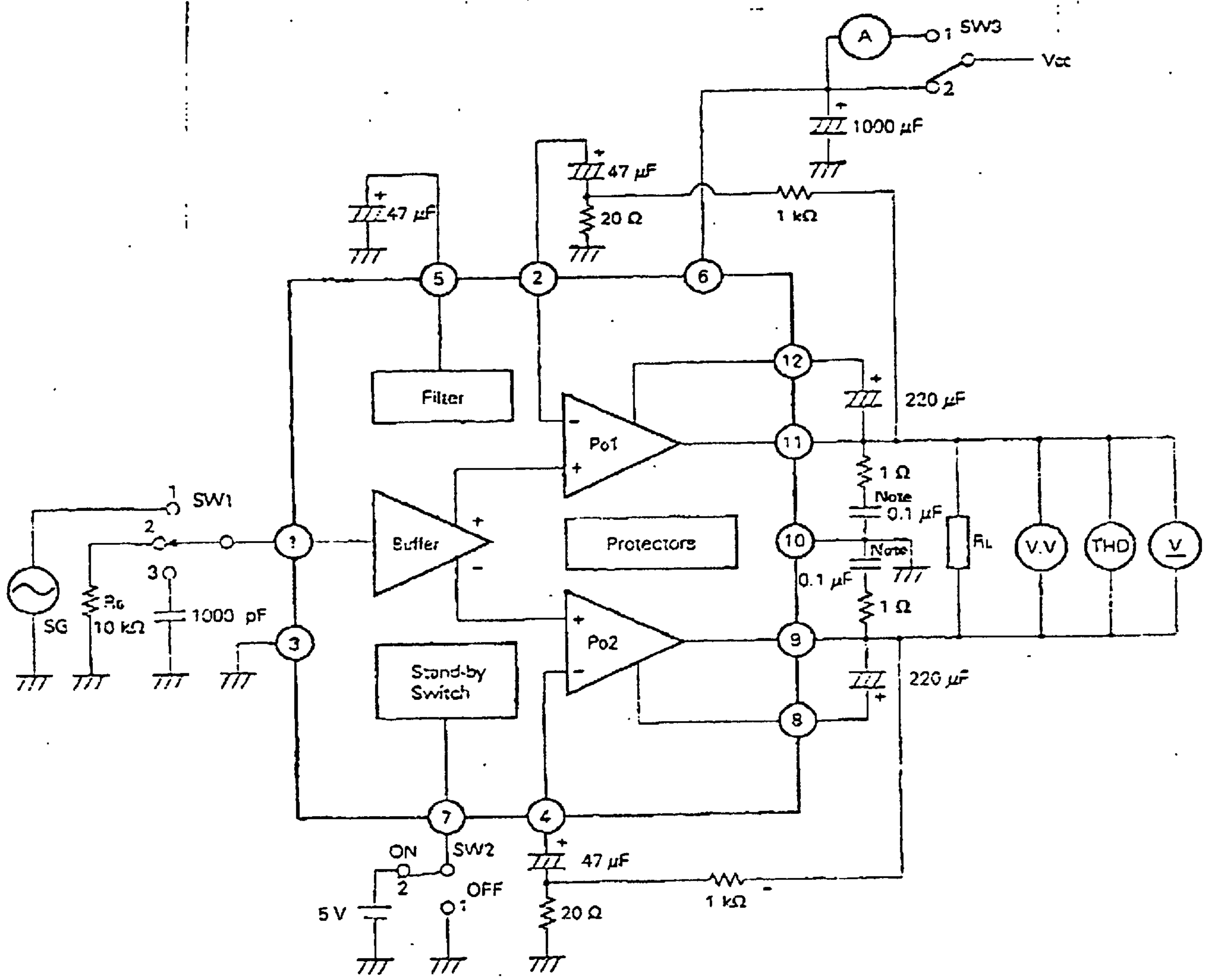
Recommended Operating Conditions (at T_a = 25 °C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		9	13.2	16	V
Load impedance	R_L		2	4	8	Ω
Stand-by switch (7) pin voltage (Operating)	V(#7)		3.5		Vcc	V
Stand-by switch (7) pin voltage (Stand-by)	V(#7)		0		1.5	V
Voltage gain	A_V		34	40		dB

Electrical Characteristics (T_a = 25 °C, V_{CC} = 13.2 V, R_L = 4 Ω, f = 1 kHz)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Circuit Current	I_{CC}	V_i = 0		150	250	mA
Output Offset Voltage	V_{offset}	V_i = 0	−150	0	+150	mV
Output Power	P_{O1}	R_L = 2 Ω, THD = 10 %	32	40		W
	P_{O2}	R_L = 2 Ω, THD = 10 %, V_{CC} = 14.4 V		45		W
	P_{O3}	R_L = 4 Ω, THD = 10 %	20	24		W
	P_{O4}	R_L = 2 Ω, THD = 1 %	25	33		W
	P_{O5}	R_L = 4 Ω, THD = 1 %	15	19		W
Voltage Gain	A_V	P_O = 2 W		40		dB
Total Harmonic Distortion	THD_1	R_L = 2 Ω, P_O = 8 W		0.03	0.12	%
	THD_2	R_L = 4 Ω, P_O = 4 W		0.03	0.12	%
Output Noise Level	V_n	R_G = 10 kΩ, BW = 20 Hz to 20 kHz		0.35	0.7	$mV_{r.m.s.}$
Supply Voltage Rejection Ratio	SVR	R_G = 0 Ω, f_{ripple} = 100 Hz, V_{ripple} = 1.0 V	50	60		dB
Input Resistance	R_i		20	30		kΩ
Roll-off Frequency	f_H	A_V = −3 dB from 1 kHz	100	250	400	kHz
	f_L	A_V = −3 dB from 1 kHz		5	10	Hz
Stand-by Current	$I_{CC(SB)}$	0 ≦ Voltage of pin 7 ≦ 1.5 V		0.05	10	μA
Overvoltage Protection Operating Voltage	$V_{CC(MAX)}$		18.5			V

ELECTRICAL CHARACTERISTICS MEASURING CIRCUIT



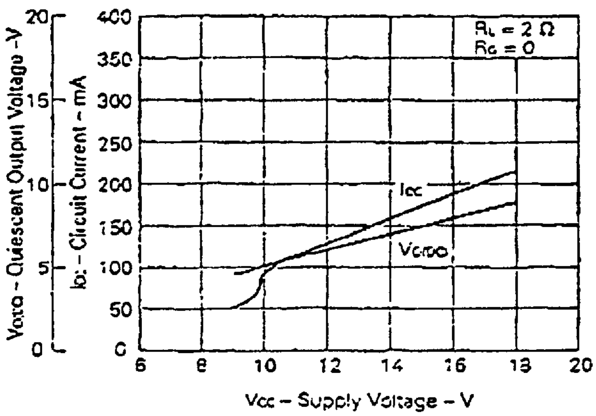
Note Mylar capacitor

SWITCH POSITION

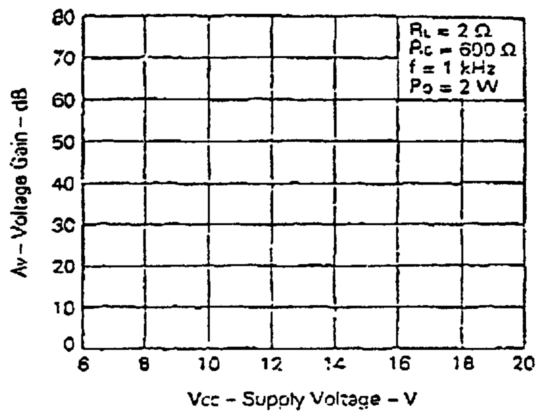
CHARACTERISTIC	SYMBOL	SW 1	SW 2	SW 3
Quiescent Current	Icc	2	2	1
Output Offset Voltage	V_{offset}	3	2	2
Voltage Gain	Av	1	2	2
Output Power	Po	1	2	2
Total Harmonic Distortion	THD	1	2	2
Output Noise Level	V_n	2	2	2
Stand-by Current	$I_{CC(SB)}$	2	1	1

2. CHARACTERISTIC CURVES (T_a = 25 °C)

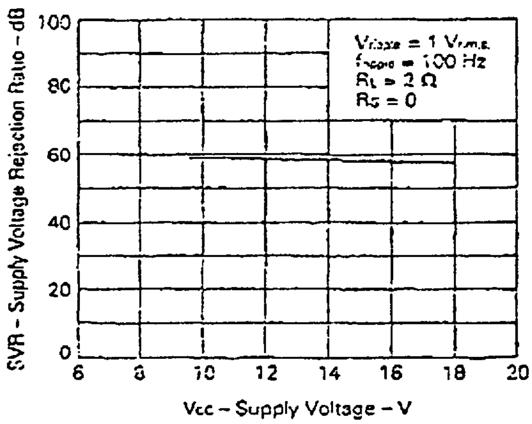
CIRCUIT CURRENT, QUIESCENT OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



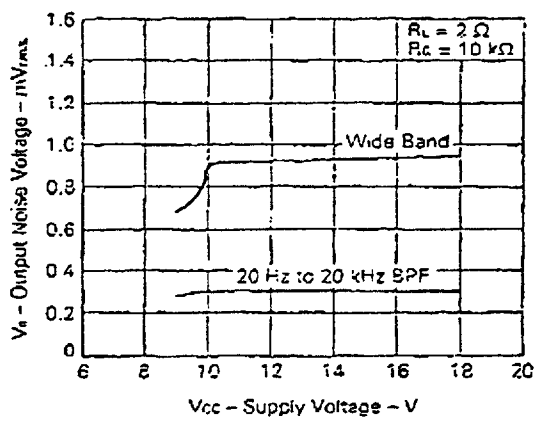
VOLTAGE GAIN vs. SUPPLY VOLTAGE



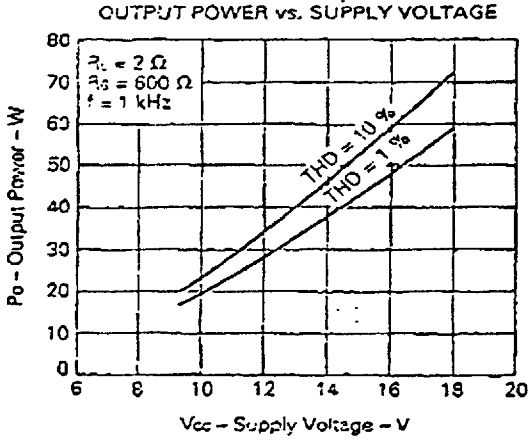
SUPPLY VOLTAGE REJECTION RATIO vs. SUPPLY VOLTAGE



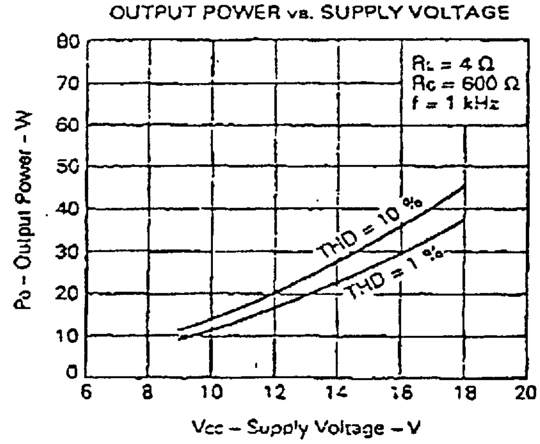
OUTPUT NOISE VOLTAGE vs. SUPPLY VOLTAGE



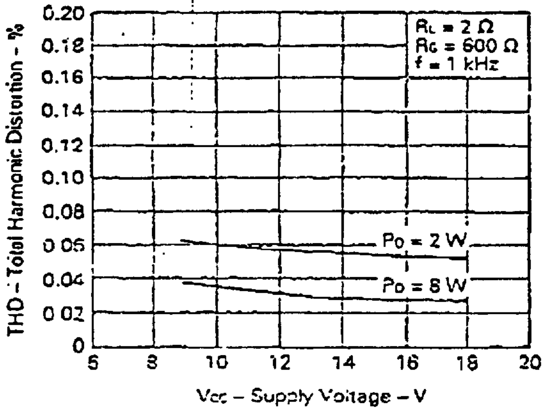
OUTPUT POWER vs. SUPPLY VOLTAGE



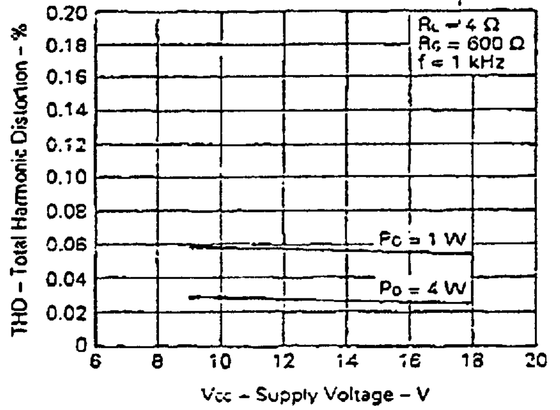
OUTPUT POWER vs. SUPPLY VOLTAGE



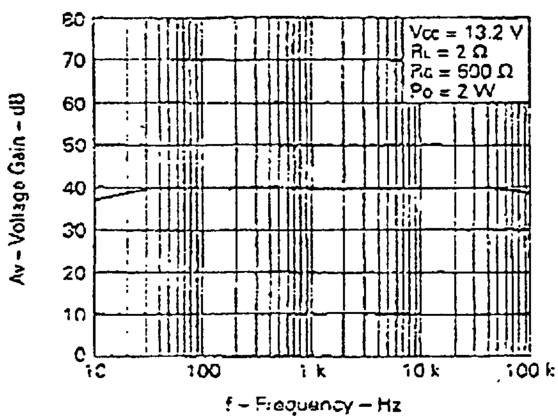
TOTAL HARMONIC DISTORTION vs. SUPPLY VOLTAGE



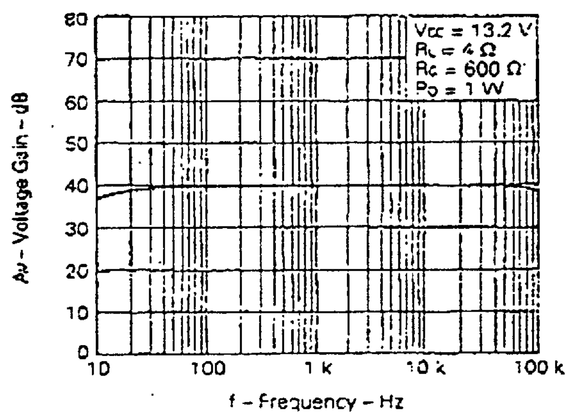
TOTAL HARMONIC DISTORTION vs. SUPPLY VOLTAGE



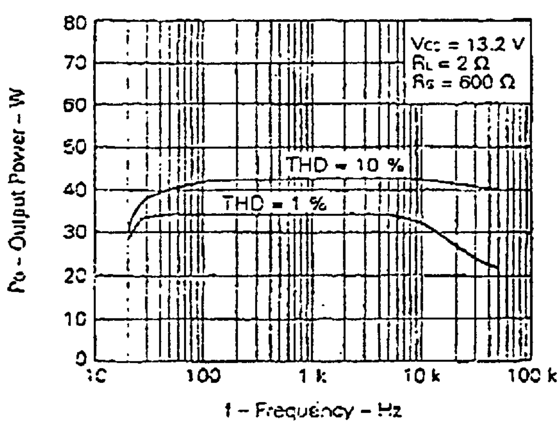
VOLTAGE GAIN vs. FREQUENCY



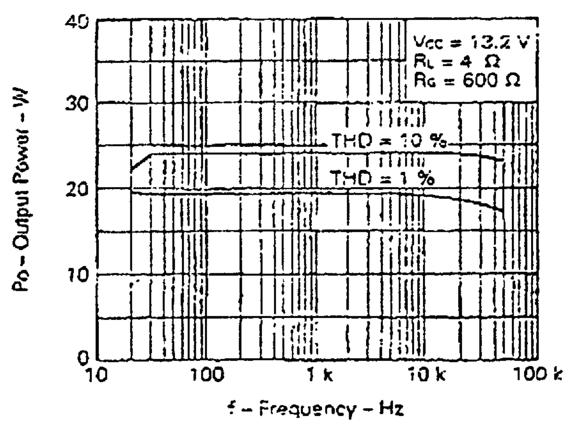
VOLTAGE GAIN vs. FREQUENCY



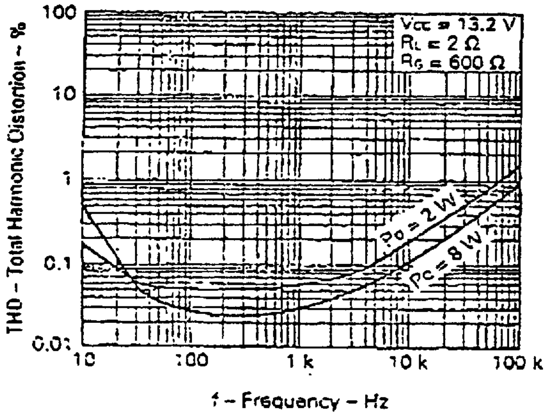
OUTPUT POWER vs. FREQUENCY



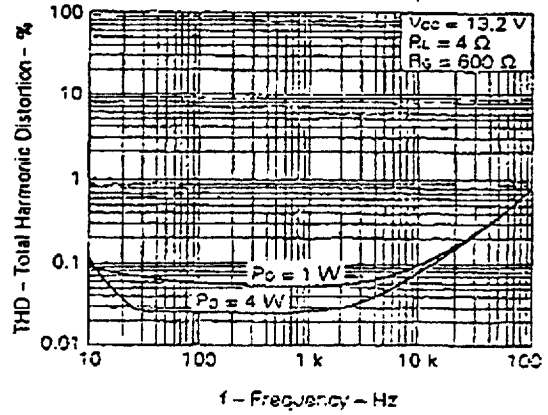
OUTPUT POWER vs. FREQUENCY



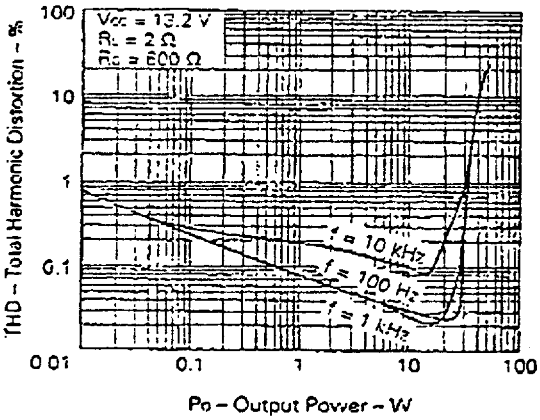
TOTAL HARMONIC DISTORTION vs. FREQUENCY



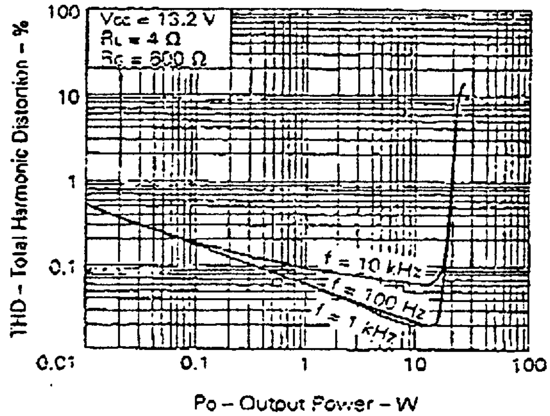
TOTAL HARMONIC DISTORTION vs. FREQUENCY



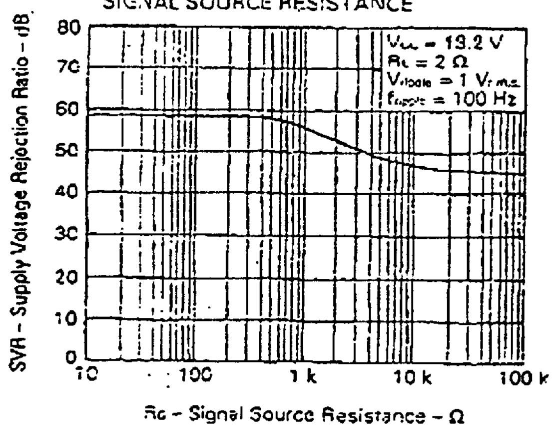
TOTAL HARMONIC DISTORTION vs. OUTPUT POWER



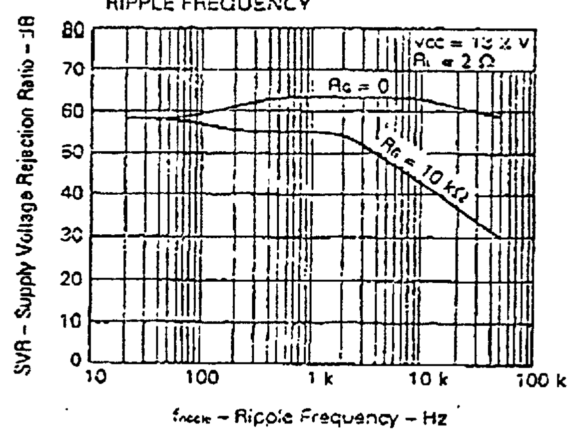
TOTAL HARMONIC DISTORTION vs. OUTPUT POWER



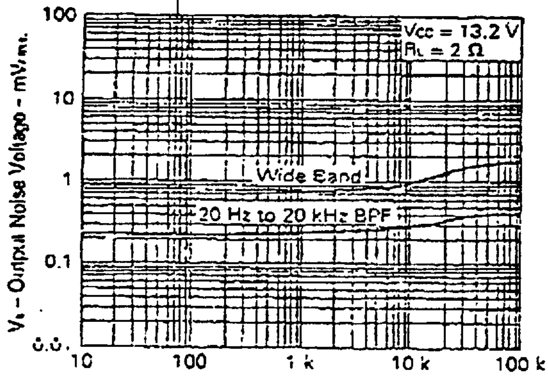
SUPPLY VOLTAGE REJECTION RATIO vs. SIGNAL SOURCE RESISTANCE



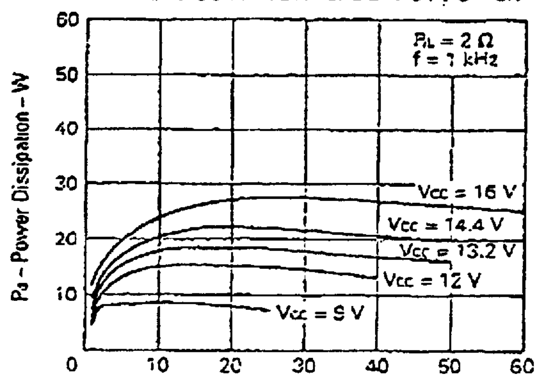
SUPPLY VOLTAGE REJECTION RATIO vs. RIPPLE FREQUENCY



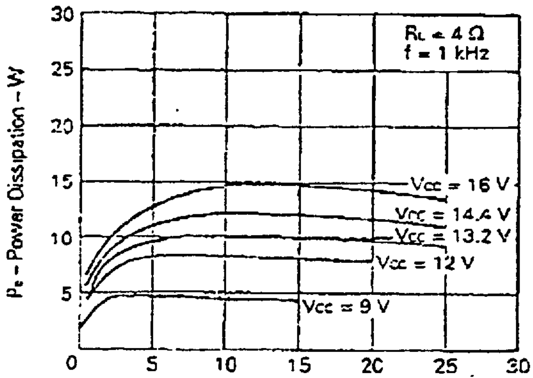
OUTPUT NOISE VOLTAGE vs. SIGNAL SOURCE RESISTANCE



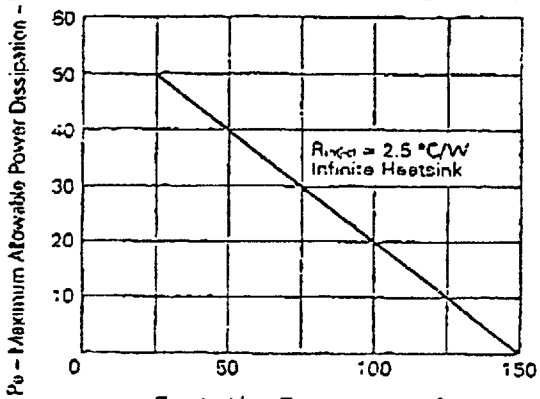
POWER DISSIPATION vs. OUTPUT POWER



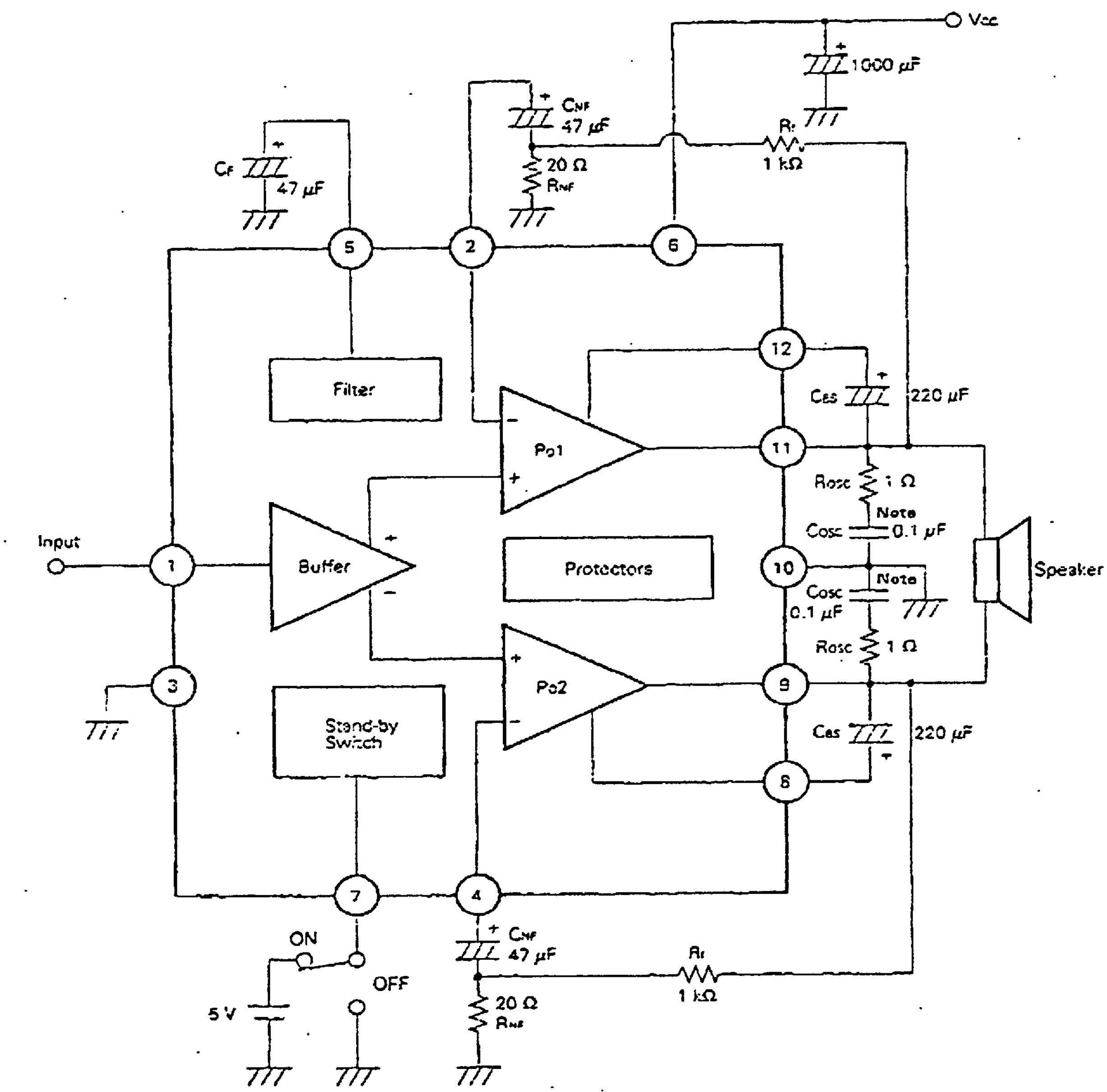
POWER DISSIPATION vs. OUTPUT POWER



MAXIMUM ALLOWABLE POWER DISSIPATION vs. AMBIENT TEMPERATURE



3. APPLICATION CIRCUIT



Note Mylar capacitor

CF : Filter capacitor
CNF : NF capacitor
CBS : Bootstrap capacitor
CROC : Capacitor for prevention of oscillation (Mylar capacitor)
ROSC : Resistor for prevention of oscillation
RF : External resistor
RNF : External resistor

4. RELATIONSHIP BETWEEN EXTERNAL PARTS AND ELECTRICAL CHARACTERISTICS

This chapter describes the effect of external parts, shown in the application circuit (see **3. APPLICATION CIRCUIT**), on the electrical characteristics of μPC2505.

The constant of each part is recommended to be set to the value shown in **3. APPLICATION CIRCUIT**. Use this as a reference when the value is changed.

4.1 Filter Capacitor (C_F)

4.1.1 Rise time

The rise time of the amplifier changes according to the capacitance of the C_F (filter capacitor). The larger this capacitance is, the longer the rise time becomes. Therefore, the rise time can be set by C_F.

See Table 4-1.

Table 4-1 Relationship between the capacitance of C_F and rise time

Capacitance of C_F (μF)	22	33	47	100	220
Rise time (s)	0.33	0.48	0.70	1.49	2.90

Caution Set the capacitance of C_F 22 μF or more.

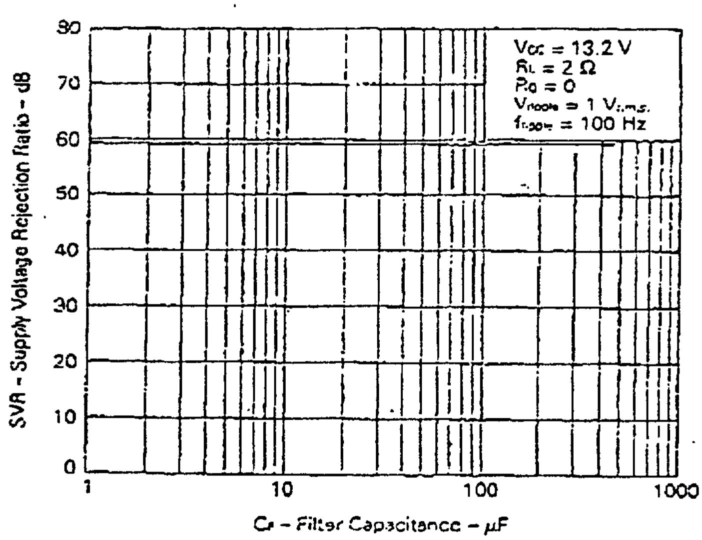
Remark The constant of the other external parts is recommended value.

4.1.2 Ripple rejection ratio

Since the structure of the positive phase signal amplifier (Po1) is exactly the same as that of the negative phase signal amplifier (Po2) in the μPC2505, the ripple components appearing in the output of speaker reject each other. Consequently, the supply voltage rejection ratio does not worsen much even if the capacitance of C_F is lessened (see Fig. 4-1).

However, the ripple components appearing in output of the output 1 (pin 11) and the output 2 (pin 9) become larger.

Fig. 4-1 Relationship between C_F and Supply Voltage Rejection Ratio



4.1.3 Resistance to breaking

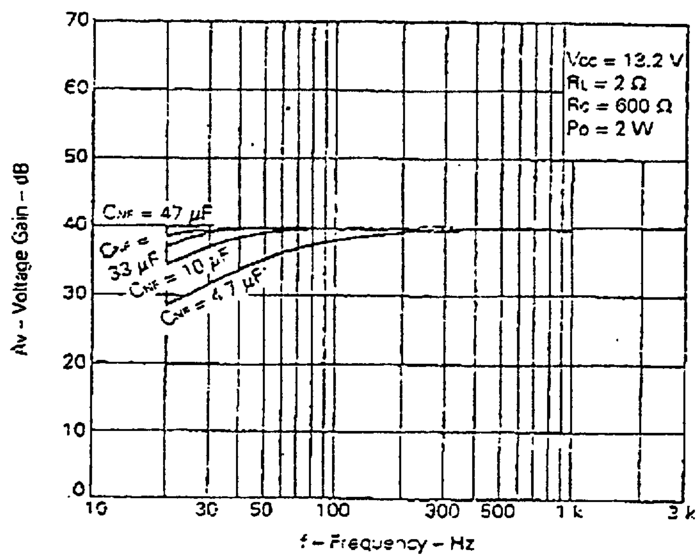
When this capacitance in made smaller, there is a risk that the resistance to breaking of the μPC2505 will lower. To prevent this, set the capacitance of C_F to 22 μF or more.

4.2 NF Capacitor (C_{NF})

4.2.1 Voltage gain

The low frequency characteristic changes when the capacitance of C_{NF} is changed (see Fig. 4-2).

Fig. 4-2 Voltage Gain vs. Frequency Characteristics



4.2.2 Rise time

When the capacitance of C_{NF} is changed, the rise time hardly changes. Therefore, the lower cut-off frequency can be decided without considering the rise time.

See Table 4-2.

Table 4-2 Relationship between the capacitance of C_{NF} and rise time

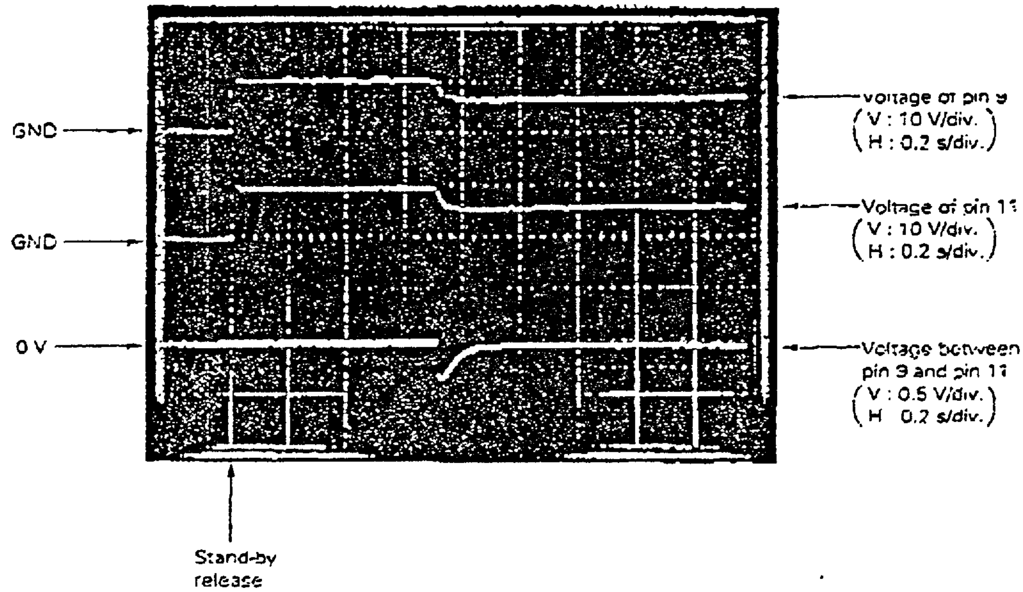
Capacitance of C_{NF} (μF)	22	33	47	100	220
Rise time (s)	0.70	0.70	0.70	0.70	0.70

Remark The constant of the other external parts is recommended value.

4.2.3 Peak value of shock noise

The rise time of μPC2505 is hardly influenced by C_{NF}. Therefore, the peak value of shock noise is controlled lower. When the relative error is 10 %, the peak value of shock noise is about quarter of μPC2500. Fig. 4-3 shows the waveform of shock noise when the relative error is 10 %.

Fig. 4-3 Waveform of Shock Noise (The Relative Error: 10 %)

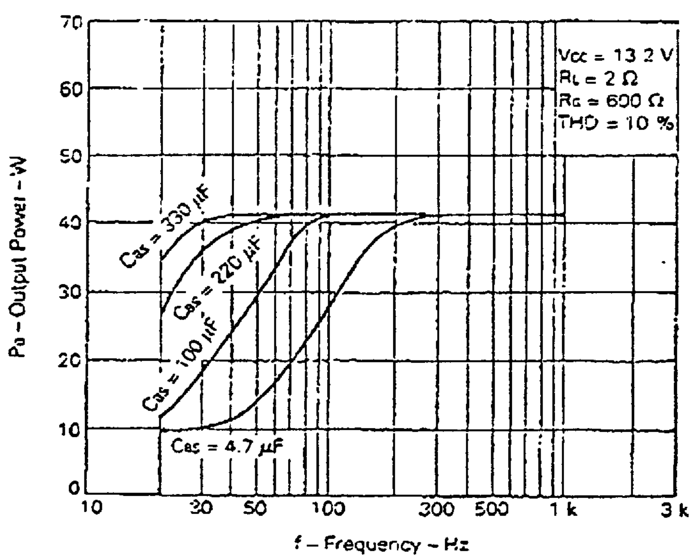


4.3 Bootstrap Capacitor (CBS)

4.3.1 Output power

When the capacitance of CBS is changed, the lower output power changes, See Fig. 4-4.

Fig. 4-4 Output Power vs. Frequency Characteristics



4.4 CR Circuit for Prevention of Oscillation (C_{osc}, R_{osc})

The CR circuit connected to output pins is used for prevention of oscillation. For the C_{osc}, use a capacitor having excellent temperature characteristic and frequency characteristic (recommended parts: mylar capacitor).

When the resistance and capacitance values of the circuits are changed, be sure to check that no oscillation is produced.

4.5 External Resistors (R_f, R_{NF})

4.5.1 Voltage gain

The closed loop voltage gain of the μPC2505 is determined depending on external resistors, R_f, R_{NF} and internal feedback resistor R_{f0}, and it can be obtained according to the following equation:

$$A_v = 20 \log \frac{R_{f0} // R_f}{R_{NF}} + 6 \text{ (dB)}$$

$R_{f0} \fallingdotseq 25\ k\Omega$

$R_{f0} // R_f$: Resistance value when R_{f0} and R_f are connected in parallel.

Caution Since the μPC2505 could start oscillating when the voltage gain is set too low, set the voltage gain to 34 dB or more.

5. PROTECTION CIRCUITS

The μPC2505 integrates various protection circuits to provide high resistance to breaking. This chapter outlines these protection circuits.

5.1 Overvoltage Protection Circuit and Surge Protection Circuit

The overvoltage circuit and surge protection circuit constitute a common circuit. When the supply voltage rises beyond 20 V TYP., it prevents the μPC2505 from being broken.

5.2 Thermal Shutdown Circuit

When the junction temperature of the μPC2505 reaches 175 °C TYP., this thermal shutdown circuit operates to reduce the current of the output bias constant current circuit, thereby curbing a further rise of temperature and preventing damage to the μPC2505. Since a latch function is not provided for the protecting operation of this circuit, the protection operation is automatically released when the junction temperature lowers to its normal temperature.

5.3 ASO Protection Circuit

The μPC2505 integrates this ASO protection circuit to provide high resistance to output pin short circuit (Vcc to output pin, output pin to GND, output pin to output pin).

When the ASO protection circuit is in its protective operation, output pins are all placed into the floating status. This prevents the speaker from breakdown when output pin short circuit and so on, occurs at the same time.

6. HEAT SINK DESIGNING

A heat sink for the μPC2505 must be designed according to the operating conditions.

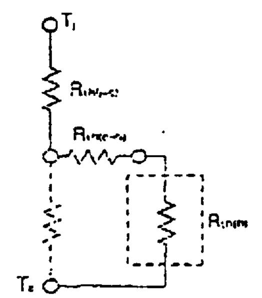
6.1 Outline of Heat Sink Designing

In general, the relationship among temperature change ΔT, thermal resistance R_{th}, and power consumption P_d is expressed as following equation:

$$\Delta T\ (^\circ C) = R_{th}\ (^\circ C/W) \times P_d\ (W)$$

For the heat sink of the μPC2505, the relationship between the thermal resistances and temperature is shown as below:

Fig. 6-1 Relationship of R_{th}, T_j and T_a



T_j	: Junction temperature
T_a	: Ambient temperature
$R_{th(j-c)}$	: Thermal resistance between junction and case
$R_{th(c-h)}$	: Thermal resistance between case and heat sink
$R_{th(h)}$	: Thermal resistance between heat sink and air
$R_{th(j-a)}$	: Thermal resistance between junction and ambience

$$R_{th(j-a)} = R_{th(j-c)} + R_{th(c-h)} + R_{th(h)}$$

That is, where the power consumption within the μPC2505 is taken as P_d, the junction temperature T_j of the μPC2505 can be represented by the following equation:

$$\begin{aligned} T_j &= T_a + R_{th(j-a)} \times P_d \\ &= T_a + (R_{th(j-c)} + R_{th(c-h)} + R_{th(h)}) \times P_d \end{aligned}$$

To keep the junction temperature less than the maximum allowable value $T_{j(MAX.)}$ when the μPC2505 is operated under the condition of the maximum ambient temperature of $T_{a(MAX.)}$ and maximum power consumption of $P_{d(MAX.)}$, the heat sink must meet the following equation:

$$R_{th(h)} < \frac{T_{j(MAX.)} - T_{a(MAX.)}}{P_{d(MAX.)}} - (R_{th(j-c)} + R_{th(c-h)})\ (^\circ C/W) \quad \cdots\cdots (1)$$

6.2 Heat Sink Designing of μPC2505

Fig. 6–2 shows the relationship between the power dissipation P_D of the μPC2505 and ambient temperature T_a. Fig. 6–3 and 6–4 show the relationship between the internal power consumption P_d and output power P_o.

From Fig. 6–2, the thermal resistance between the junction and heat sink of μPC2505 is given by "$R_{th(j-h)} = R_{th(j-c)} + R_{th(c-h)} = 2.5$ (°C/W)".

On the other hand, the absolute maximum rating $T_{j(MAX.)}$ of the junction temperature of μPC2505 is 150 °C. Therefore, equation (1) above becomes as shown below:

$$R_{th(h)} < \frac{150 - T_{a(MAX.)}}{P_{d(MAX.)}} - 2.5 \text{ (°C/W)} \quad \cdots\cdots (2)$$

Designing Procedure of Heat Sink

① Set the operating conditions.

(a) Load impedance : R_L
(b) Supply voltage : V_{CC}
(c) Maximum ambient temperature : $T_{a(MAX.)}$

② Obtain the maximum power consumption $P_{d(MAX.)}$ under conditions of (a) and (b) from Fig. 6–3 and 6–4.

③ Incorporate $T_{a(MAX.)}$ and $P_{d(MAX.)}$ obtained from steps ① and ② above into equation (2) to obtain the required thermal resistance of the heat sink.

Caution Although the thermal resistance of the heat sink can be obtained according to the method described above, it is recommended to use a heat sink somewhat larger than the calculated value for greater reliability. Also, be sure to use silicon grease when the heat sink is mounted to the μPC2505.

Fig. 6-2 Pᴅ vs. Tₐ Characteristic

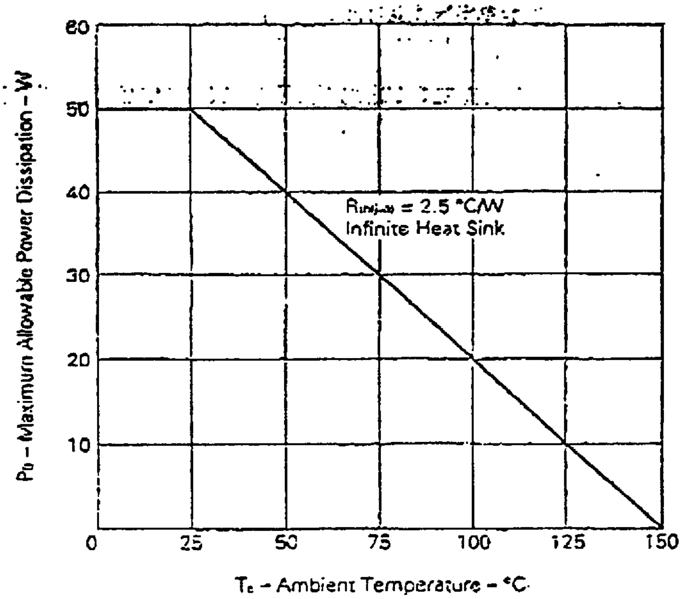


Fig. 6-3 Pd vs. Po Characteristic (RL = 2 Ω)

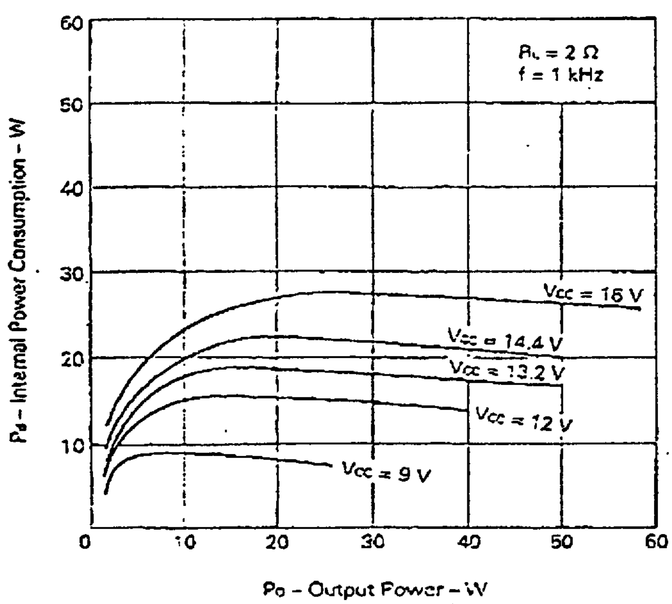
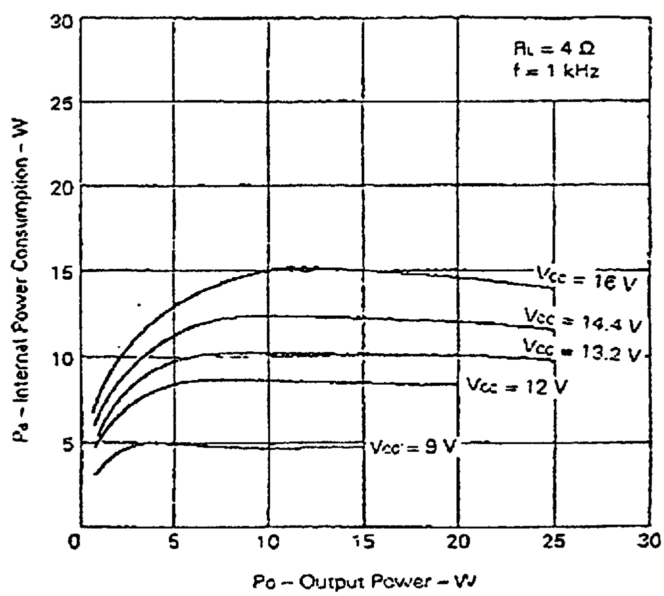


Fig. 6-4 Pd vs. Po Characteristic (RL = 4 Ω)



7. ATTENTION ON APPLICATION

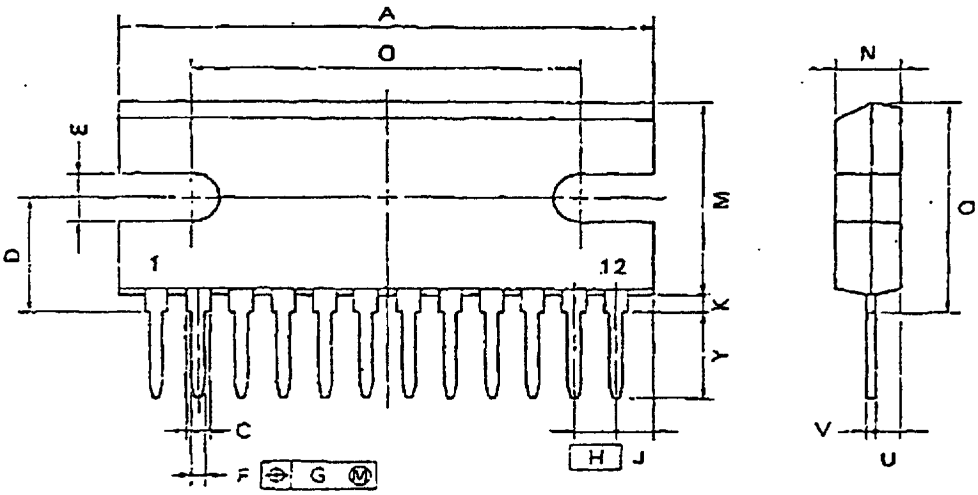
When attaching the μPC2505 on the heat sink, note following points.

- Be sure to use the silicon grease.
- Keep the fastening torque for the screw in the range of 5 to 8 kg·cm.
- Flatness of attached area of heat sink should be kept within ±0.1 mm.

When the μPC2505 is unstable due to the high impedance of signal source, connect a capacitor (about 1000 pF) between pin 1 and pin 3.

8. PACKAGE DRAWING

12 PIN PLASTIC POWER SIP (L)



NOTE
Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

P12HP-254B2

ITEM	MILLIMETERS	INCHES
A	33.02 MAX	1.3 MAX.
C	1.2 MIN.	0.047 MIN.
D	$8.2^{\pm 0.3}$	$0.323^{\pm 0.012}$
E	$3.8^{\pm 0.1}$	$0.142^{+0.004}_{-0.005}$
F	$0.8^{\pm 0.1}$	$0.031^{+0.004}_{-0.005}$
G	0.25	0.01
H	2.54	0.1
J	2.54 MAX.	0.1 MAX.
K	1.0 MIN.	0.039 MIN.
M	13.8 MAX.	0.544 MAX
N	$4.8^{\pm 0.2}$	$0.189^{\pm 0.008}$
O	$24.0^{\pm 0.1}$	$0.945^{+0.004}_{-0.005}$
Q	15.0 MAX.	0.591 MAX
U	2.8 MAX.	0.111 MAX.
V	$0.35^{\pm 0.1}$	$0.014^{+0.004}_{-0.005}$
Y	$6.6^{\pm 0.7}$	$0.256^{\pm 0.028}$

9. RECOMMENDED SOLDERING CONDITIONS

The following conditions (see table below) must be met when soldering this product.

For more details, refer to our document "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).

Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

Type of Through Hole Device

μPC2505H : 12 pin plastic power SIP (L)

Soldering Process	Soldering Conditions
Wave Soldering (For leads only)	Solder temperature: 260 °C or lower. Flow time: 10 seconds or less.
Partial Heating Method	Pin temperature: 260 °C or lower. Time: 10 seconds or less.

Caution Do not jet molten solder on the surface of package.