1.8V Auto-Zero In-Amp w/ Shutdown

Preliminary Technical Data AD8553

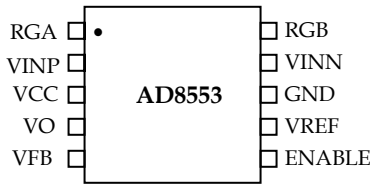
FEATURES

Low Offset Voltage: 25 µV max
Low Input Offset Drift: 0.1 µV/°C max
High CMRR: 120 dB min @ G=100
Low Noise: 0.7 µV p-p from 0.01Hz-10Hz
Wide Gain Range: 1 to 10,000
Single Supply Operation: +1.8V to +5.5V
Rail-to-Rail Output
Shutdown capability

APPLICATIONS

Strain Gages
Weigh Scales
Pressure Sensors
Laser Diode Control Loops
Portable Medical Instruments
Thermocouple Amplifiers

10-Lead MSOP
(RMZ-10)



GENERAL DESCRIPTION

The AD8553 is a precision instrumentation amplifier featuring low noise, rail-to-rail output and a power-saving shutdown mode. The AD8553 also features low offset and drift coupled with high common mode rejection. In shutdown mode, the total supply current is reduced to less than 4 µA. Operation is fully specified from +1.8V to +5.5V.

With low offset voltage of 25µV, offset voltage drift of 0.1µV/°C and voltage noise of only 0.7µV p-p (0.01Hz to 10 Hz), the AD8553 is ideal for applications where error sources cannot be tolerated. Precision instrumentation, position and pressure sensors, medical instrumentation, and strain gauge amplifiers benefit from the low noise, low input bias current, and high common mode rejection. The small footprint and low cost are ideal for high volume applications.

The small package and low power consumption allow maximum channel density or minimum board size for space-critical equipment and portable systems.

The AD8553 is specified over the industrial temperature range from -40°C to +85°C. The AD8553 is available in the lead-free 10-lead MSOP.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 **World Wide Web Site: http://www.analog.com**
Fax: 617/326-8703

ELECTRICAL SPECIFICATIONS

(V_S = 5V, V_{CM} = 2.5V, V_O = V_{REF} = V_{CC}/2, R_L = 10kΩ to GND, T_A=25°C unless specified, G=1000 (R_1 = 4kΩ, R_2 = 2MΩ), G=100 (R_1 = 3.92kΩ, R_2 = 196kΩ), G=10 (R_1 = 20kΩ, R_2 = 100kΩ), G=1 (R_1 = 200kΩ,R_2 = 100kΩ))

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Input Offset Voltage	Vos	G = 1000			25	µV
		G = 100			25	µV
		G = 10			50	µV
		G = 1			350	µV
vs. Temperature	$\Delta V_{os}/\Delta T$	G = 1000, -40°C ≤ T_A ≤ +85°C		0.01	0.1	µV/°C
		G = 100, -40°C ≤ T_A ≤ +85°C		0.01	0.1	µV/°C
		G = 10, -40°C ≤ T_A ≤ +85°C		0.1	0.3	µV/°C
		G = 1, -40°C ≤ T_A ≤ +85°C		0.7	3	µV/°C
Input Bias Current	I_B			0.3	1	nA
		-40°C ≤ T_A ≤ +85°C			2	nA
Input Bias Current @ V_{REF}				0.02	1	nA
Input Operating Impedance						
Differential				75 || 2		MΩ || pF
Common-Mode				100 || 2		MΩ || pF
Input Voltage Range			0		3.35	V
Common-Mode Rejection Ratio	CMRR	G = 100, V_{CM} = 0V to 3.35V	120	140		dB
		-40°C ≤ T_A ≤ +85°C	105	140		dB
		G=10, V_{CM} = 0V to 3.35V	100	120		dB
Gain Error		G = 100, V_{CM} = 12.125 mV, V_O = 0.075V to 4.925V			0.25	%
		G = 10, V_{CM} = 121.25mV, V_O = 0.075V to 4.925V			0.5	%
Gain tempco		-40°C ≤ T_A ≤ +85°C			50	ppm/°C
Non-Linearity		G = 100, V_{CM} = 12.125mV, V_O = 0.075V to 4.925V			0.006	% FS
		G=10, V_{CM} = 121.25mV, V_O = 0.075V to 4.925V			0.035	% FS
V_{REF} Range			0.8		4.2	V
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}		4.925			V
Output Voltage Low	V_{OL}				0.075	V
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	G=100, Vs = 1.8V to 5.5V, V_{CM} = 0V	100	120		dB
		G=10, Vs = 1.8V to 5.5V, V_{CM} = 0V	90	106		dB
Supply Current	I_{SY}	I_O = 0, V_{IN} = 0V		1.1	1.3	mA
		-40°C ≤ T_A ≤ +85°C			1.5	mA
Supply Current Shutdown Mode	I_{SD}			2	4	µA
ENABLE (pin) INPUTS						
Logic High Voltage		VINH	2.4			V
Logic Low Voltage		VINL			0.8	V

NOISE PERFORMANCE						
Voltage Noise	$e_{n\ p-p}$	f = 0.01 Hz to 10 Hz		0.7		μV_{p-p}
Voltage Noise Density	e_n	G = 100, f = 1 kHz		35		$nV/\sqrt{Hz}$
		G = 10, f = 1kHz		150		$nV/\sqrt{Hz}$
Internal Clock Frequency				40		kHz
Signal Bandwidth		G = 1 to 1000		1*		kHz
				(*500	Hz for x-grade samples)	

ELECTRICAL SPECIFICATIONS

(V_S = 1.8V, V_{CM} = 0.1V, V_O = V_{REF} = V_{CC}/2, R_L = 10kΩ to GND, T_A=+25°C unless specified, G=1000 (R_1 =4kΩ, R_2 = 2MΩ), G=100 (R_1 = 3.92kΩ, R_2 = 196kΩ), G=10 (R_1 =20kΩ, R_2 = 100kΩ), G=1 (R_1 =200kΩ, R_2 = 100kΩ))

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Input Offset Voltage	V_{os}	G = 1000			30	µV
		G = 100			30	µV
		G = 10			60	µV
		G = 1			500	µV
vs. Temperature	$\Delta V_{os}/\Delta T$	G = 1000, -40°C ≤ T_A ≤ +85°C		0.1	0.5	µV/°C
		G = 100, -40°C ≤ T_A ≤ +85°C		0.1	0.5	µV/°C
		G = 10 , -40°C ≤ T_A ≤ +85°C			3	µV/°C
		G = 1, -40°C ≤ T_A ≤ +85°C			10	µV/°C
Input Bias Current	I_B			0.3	1	nA
		-40°C ≤ T_A ≤ +85°C			2	nA
Input Bias Current @ V_{REF}				0.02	1	nA
Input Operating Impedance						
Differential				75 || 2		MΩ || pF
Common-Mode				100 || 2		MΩ || pF
Input Voltage Range			0		0.15	V
Common-Mode Rejection Ratio	CMRR	G=100, V_{CM} = 0V to 0.15V	100	110		dB
		-40°C ≤ T_A ≤ +85°C	86			dB
		G=10, V_{CM} = 0V to 0.15V	86	95		dB
Gain Error		G = 100, V_{CM}=4.125 mV, V_O = 0.075V to 1.65V			0.35	%
		G = 10, V_{CM} = 41.25mV, V_O = 0.075V to 1.65V			0.5	%
Gain tempco		-40°C ≤ T_A ≤ +85°C			50	ppm/°C
Non-Linearity		G= 100, V_{CM} = 4.125mV, V_O = 0.075V to 1.65V		0.015		% FS
		G=10, V_{CM} = 41.25mV, V_O = 0.075V to 1.65V		0.015		% FS
V_{REF} Range			0.8		1.0	V
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10kΩ to GND	1.65			V
Output Voltage Low	V_{OL}	R_L = 10kΩ to GND			0.075	V
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	G = 100, V_S = 1.8V to 5.5V, V_{CM} = 0V	100	120		dB
Supply Current	I_{SY}	I_O = 0, V_{IN} = 0V		0.9	1.2	mA
		-40°C ≤ T_A ≤ +85°C			1.4	mA
Supply Current Shutdown Mode	I_{SD}			2	4	uA

ENABLE (pin) INPUTS						
Logic High Voltage	V_{INH}		1.4			V
Logic Low Voltage	V_{INL}				0.5	V
NOISE PERFORMANCE						
Voltage Noise	$e_{n\ p-p}$	f = 0.01 Hz to 10 Hz		1		μV_{p-p}
Voltage Noise Density	e_n	G= 100, f = 1 kHz		45		nV/√Hz
		G=10, f = 1kHz		180		nV/√Hz
Internal Clock Frequency				40		kHz
Signal Bandwidth		G=1 to 1000		1*		kHz
				(*500 Hz for x-grade samples)		

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... +6V
Input Voltage ..... +Vsupply
Differential Input Voltage[1] ..... ±Vsupply
Output Short-Circuit Duration to Gnd ..... Indefinite
Storage Temperature Range
RM Package ..... -65°C to +150°C
Operating Temperature Range
AD8553 ..... -40°C to +85°C
Junction Temperature Range
RM Package ..... -65°C to +150°C
Lead Temperature Range (Soldering, 10 sec) ..... +300°C

Package Type	θ_{JA}[2]	θ_{JC}	Units
10-Lead MSOP (RMZ)	TBD	TBD	°C/W

NOTES

[1] Differential input voltage is limited to ±5.0 volts or the supply voltage, whichever is less.

[2] θ_{JA} is specified for the worst case conditions, i.e., θ_{JA} is specified for device in socket for P-DIP packages; θ_{JA} is specified for device soldered in circuit board for SOIC and TSSOP packages.

ORDERING GUIDE

Model	Temperature Range	Package Description	Suffix
AD8553ARMZ-R2	-40°C to +85°C	10-Lead MSOP	RM-10
AD8553ARMZ-REEL	-40°C to +85°C	10-lead MSOP	RM-10

APPLICATIONS

Typical Configuration
Figures 1 and 2 show a typical AD8553 circuit configuration for an A/D converter application.

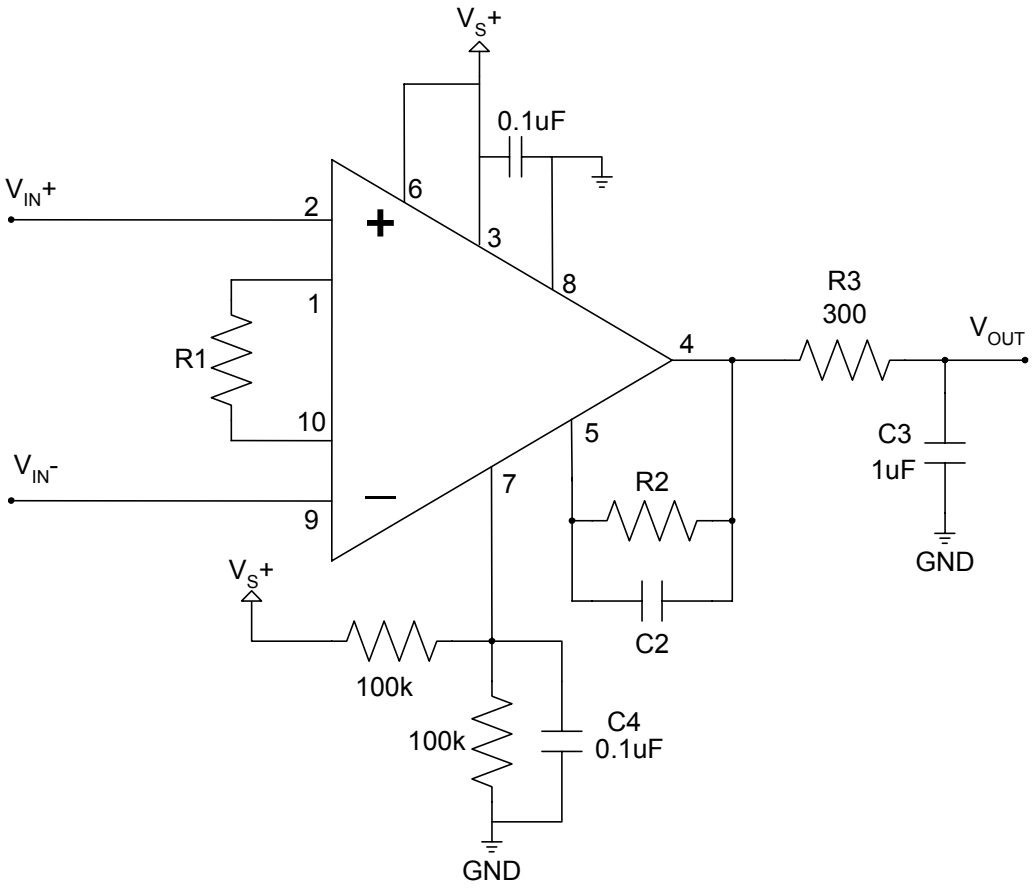


Figure 1. Single-supply connection diagram

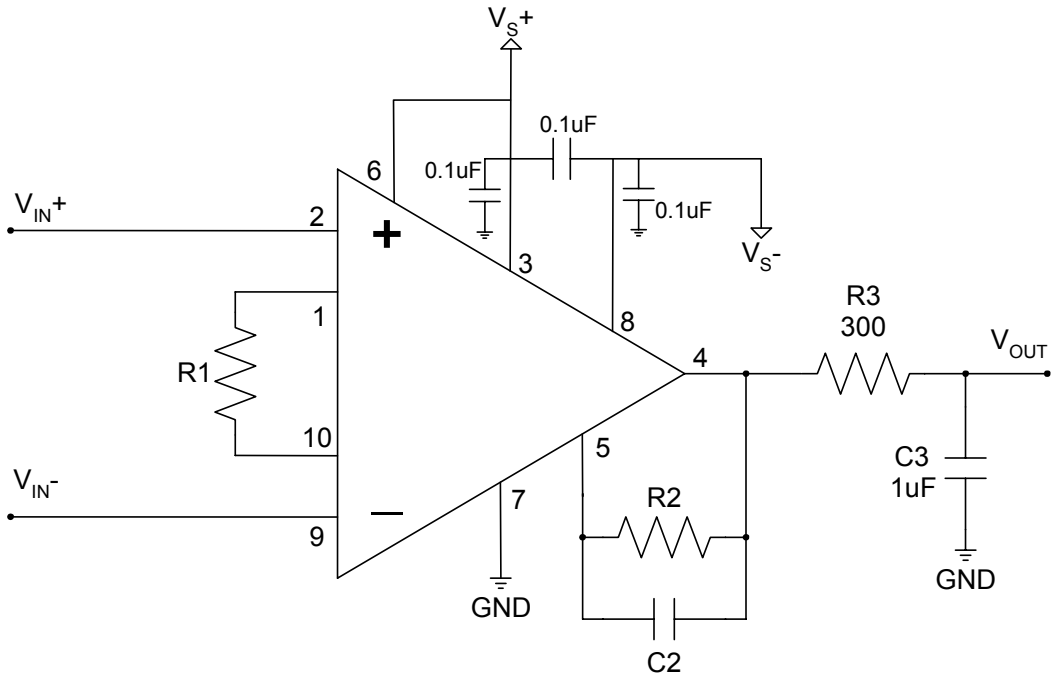


Figure 2. Dual-supply connection diagram

Gain Selection
The gain of the AD8553 is set according to the following equation:

$$G = 2*(R2/R1)$$

For proper operation:
(1) $R1 \geq 3.92k\Omega$
(2) $R1 \geq V_{in} / 13uA$.

Gain accuracy depends on the matching of the two external resistors. Any mismatch in resistor values results in a gain error. However, due to the current-mode operation of the AD8553, CMRR is not degraded because of resistor mismatch.

Care should be taken when selecting and positioning the gain setting resistors. The resistors should be made of the same material and package style. Surface mount resistors are recommended. They should be positioned as close together as possible to minimize TC errors and feedback voltage errors.

If resistor trimming is required to set a precise gain, trim resistor R2 only. Parasitic capacitance to pins 1 and 10 (resistor R1 connections) must be minimized.

Reference Connection
Unlike traditional three-opamp instrumentation amplifiers, parasitic resistance in series with the Vref pin (pin 7) does not degrade CMRR performance. This allows the AD8553 to attain its extremely high CMRR performance without the use of an external buffer amplifier driving the Vref pin. When using a single supply, the reference voltage can be set with a simple resistor voltage divider between the supply and ground (Figure 1). Capacitor C4 is recommended to filter supply noise. For optimal performance in single-supply applications, Vref should be set with a low-noise

precision voltage reference (for example, from the ADC). In dual-supply applications, Vref can simply be connected to ground.

Output Filtering

Filter capacitor C2 is required to limit the amount of switching noise present at the output. The recommended bandwidth of the filter created by C2 and R2 is 1.5 kHz (AD8553 x-grade samples are 500 Hz). The user should first select R1 and R2 based on the desired gain, then select C2 based on the following formula:

$$C2 = 1/(1500*2*\pi*R2)$$

Another single-pole R-C filter on the output is recommended. A filter frequency of 1.5kHz is recommended (AD8553 x-grade samples are 500 Hz). This filter can also serve as an anti-aliasing filter if the AD8553 is used to drive an A/D converter.

Maximizing Performance with a Proper Layout

To achieve the maximum performance of the AD8553, care should be taken in the circuit board layout. The PC board surface must remain clean and free of moisture to avoid leakage currents between adjacent traces. Surface coating of the circuit board will reduce surface moisture and provide a humidity barrier, reducing parasitic resistance on the board.

Care must be taken to minimize parasitic capacitance on pins 1 and 10 (resistor R1 connections). Traces from the IC to R1 should be kept symmetric and as short as possible. Excessive capacitance on these pins results in a gain error. This effect is most prominent at low gains (G < 10).

Power Supply Bypassing

A stable DC voltage should be used to power the AD8553. Noise on the supply pins may adversely affect performance. Bypass capacitors should be used to decouple the amplifier.

For dual-supply operation, a 0.1 µF surface-mount capacitor should be connected from each supply pin to ground. Additionally, another 0.1 µF surface-mount capacitor should be connected between the supply lines to maintain DC precision. For single-supply operation, one 0.1 µF surface-mount capacitor should be connected between the supply line and ground. All bypass capacitors should be positioned as close to the IC as possible.

A 10 µF tantalum capacitor may be used further away from the part for additional bypassing. In most cases, it may be shared by other precision ICs on the circuit board.

Load Drive

Figures 1 and 2 show a typical AD8553 circuit configuration for an A/D converter application. In this case, R3 will react with the converter input resistance and typically cause a small gain error. This gain error is due to the voltage divider that occurs due to R3 and the converter input resistance, or RL.

In some applications, the user may require a low impedance output drive from the AD8553. In this case, it is recommended that the user use the circuit shown in Figure 3. This circuit incorporates the second filter pole into the feedback of the output amplifier. This results in a low impedance output to drive the load, R_L. If the required current, I_L, for the load is significant, the user should consider the limitation on the output swing due to R3. In this case, the voltage at pin 4 is limited to the specified output swing, but the voltage at Vout is further limited by the voltage drop across R3, I_L*R3.

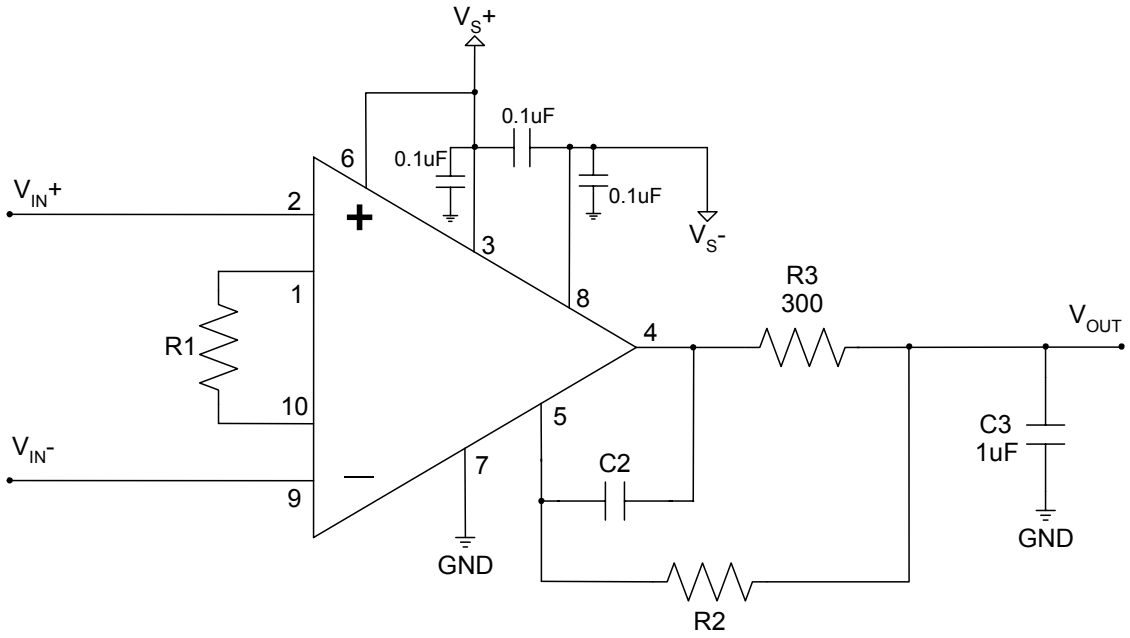


Figure 3. AD8553 configuration for low impedance output drive