# PROCESS CP210

## Small Signal Transistors

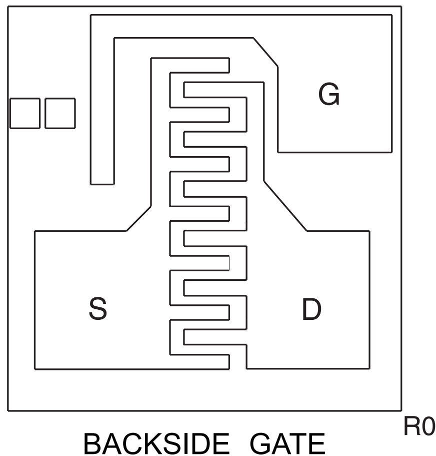
### N - Channel Silicon Amplifer J FET Chip

**Central**™
**Semiconductor Corp.**

**PROCESS DETAILS**

| Process | EPITAXIAL PLANAR |
|---|---|
| Die Size | 15 x 15 MILS |
| Die Thickness | 8.0 MILS |
| Drain Bonding Pad Area | 3.2 X 4.0 MILS |
| Source Bonding Pad Area | 3.2 X 4.0 MILS |
| Gate Bonding Pad Area | 3.2 X 4.0 MILS |
| Top Side Metalization | Al - 30,000Å |
| Back Side Metalization | Au - 6,000Å |

**GEOMETRY**




**GROSS DIE PER 4 INCH WAFER**
53,730

**PRINCIPAL DEVICE TYPES**
2N4416A
CMPF4416A

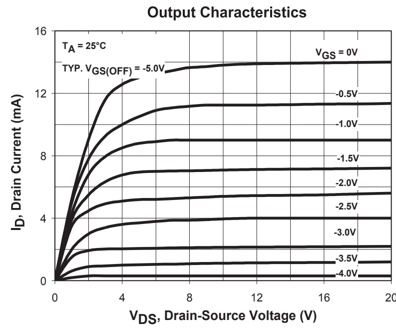
145 Adams Avenue
Hauppauge, NY 11788 USA
Tel: (631) 435-1110
Fax: (631) 435-1824
www.centralsemi.com

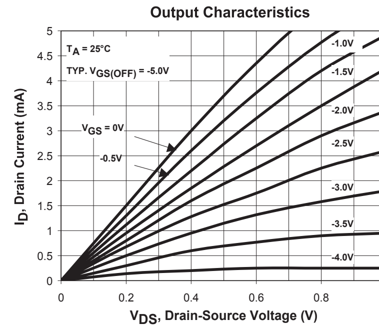
R3 (9 -September 2003)

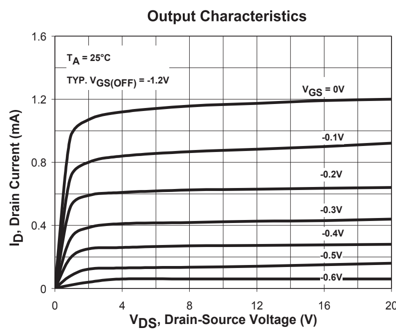
# Central™ Semiconductor Corp.

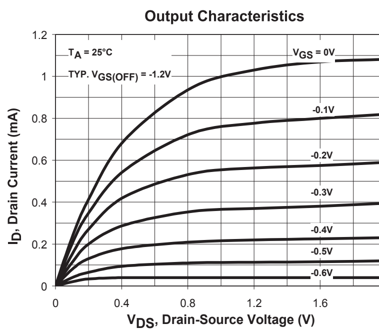
# *PROCESS* CP210

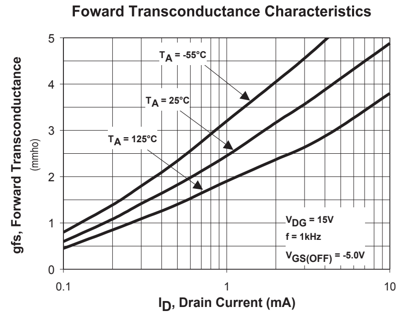
## Typical Electrical Characteristics

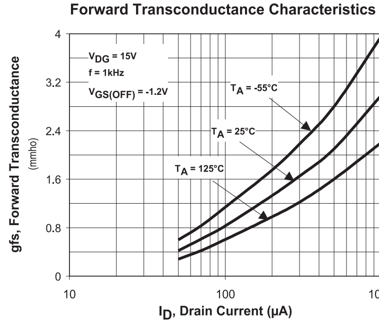
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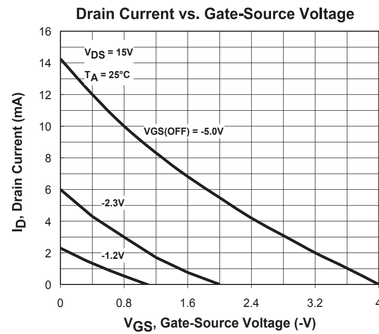


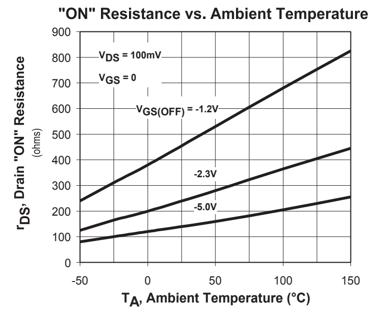


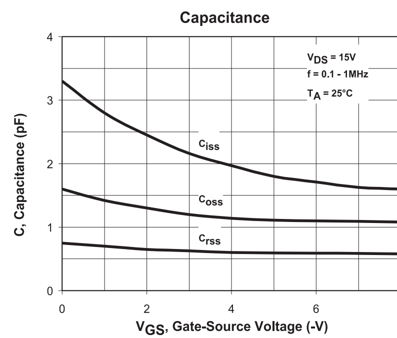


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