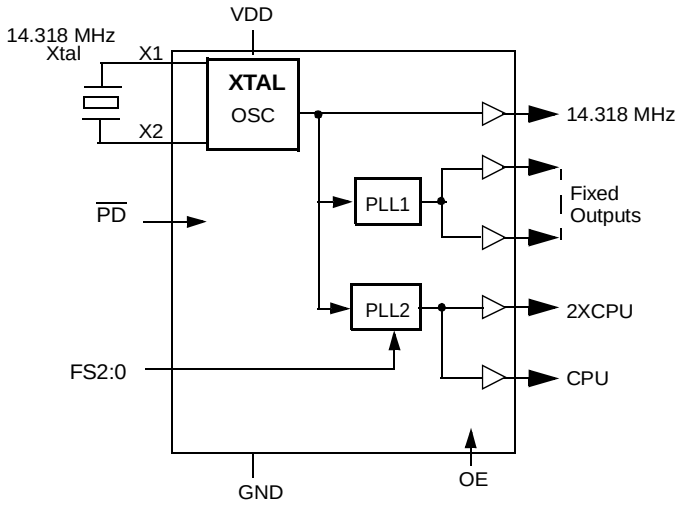
W48C54A/55A

Frequency Synthesizers

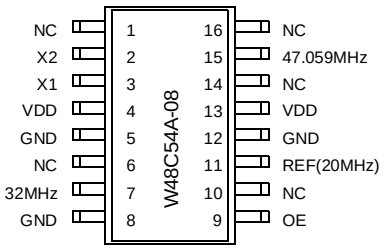
Features

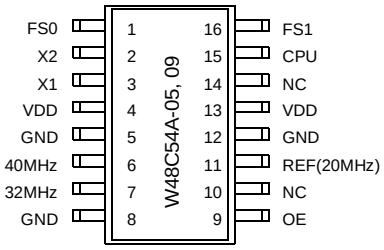
- **Proprietary crystal oscillator circuitry provides low REFOUT jitter, excellent duty cycle**
- **Power-on delay feature ensures full V_{DD} is reached prior to output activation**
- **3.3V and 5V operation supported including the VRE (Voltage Regulated Extended) specification for Pentium® processor**
- **Pin and function compatible with AV9154/AV9155**
- **Integral PLL loop filter components ensures stable PLL operation in noisy system environment**
- **Smooth frequency transition of CPU and 2XCPU outputs**
- **Compatible with Intel X86 and other high-performance processors**
- **Up to eight outputs for CPU and peripherals**
- **Supports Green PC and notebook designs**
- **Custom options available with metal layer change**
- **High-performance, low-power CMOS**
- **Available in 16- (150-mil) and 20-pin SOIC package (300-mil)**

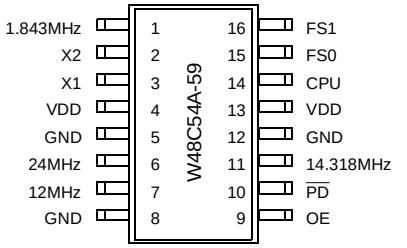
Block Diagram

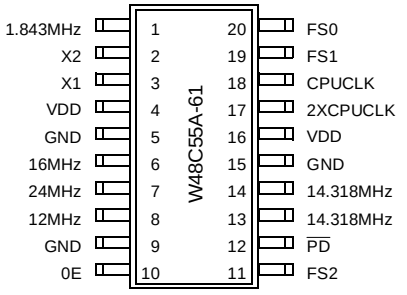


Pin Configurations









Pin Definitions

Pin Name	Pin Type	Pin # -05, -09	Pin # -08	Pin # -59	Pin # -61	Pin Description
1.843MHz	O	N/A	N/A	1	1	Fixed 1.843-MHz output for serial I/O clock application
12MHz	O	N/A	N/A	7	8	Fixed 12-MHz output for keyboard clock application
16MHz	O	N/A	N/A	N/A	6	Fixed 16-MHz output for APIC or bus clock application
REF	O	11	11	11	13, 14	Fixed Reference output.
24MHz	O	N/A	N/A	6	7	Fixed 24-MHz output for floppy drive or super I/O application
32MHz	O	7	7	N/A	N/A	Fixed 32-MHz output for ISA or PCI bus clock application
40MHz	O	6	N/A	N/A	N/A	Fixed 40-MHz output for SCSI clock application
47.059MHz	O	N/A	15	N/A	N/A	Fixed 47.059-MHz output
2XCPU	O	N/A	N/A	N/A	17	2X Clock Output (refer to Frequency Selection table)
CPU	O	15	N/A	14	18	Clock Output (refer to Frequency Selection table)
NC		10, 14	1, 6, 10, 14, 16	N/A	N/A	No Connect
OE	I	9	9	9	10	Output Enable, puts all outputs in high-impedance state when LOW
$\overline{PD}$	I	N/A	N/A	10	12	Power Down input, puts device in power-down mode when LOW
FS0	I	1	N/A	15	20	Frequency Selection input, LSB
FS1	I	16	N/A	16	19	Frequency Selection input
FS2	I	N/A	N/A	N/A	11	Frequency Selection input
VDD	P	4, 13	4, 13	4, 13	4, 16	Power supply connection
GND	G	5, 8, 12	5, 8, 12	5, 8, 12	5, 9, 15	Ground connection
X1	I	3	3	3	3	Crystal connection or external clock frequency input
X2	O	2	2	2	2	Crystal connection, leave unconnected when driving X1 with external clock

Overview

The W48C54A and W48C55A are general-purpose clock generator ICs. Some of the standard device options described in this document are designed for PC motherboard and embedded applications. Backward compatible with the W48C54 and W48C55, these dual-PLL clock devices incorporate an improved crystal oscillator as well as other refinements. On-chip loop filter components ensure stable operation even with the noise typical of a digital system. Device functionality, including input/output options and frequency selection is determined by a single metal mask that allows quick-turn customization capability. Both 3.3- and 5-volt operation are supported.

The improved crystal oscillator of the W48C54A and W48C55A most notably provides improved duty cycle at the reference output(s). With this new design, duty cycle is not affected by varying operating conditions such as with the addition of external crystal load capacitors. Clock jitter from the 14.318-MHz output(s) is also improved, as is the crystal oscillation frequency accuracy.

Like the W48C54 and W48C55, the W48C54A and W48C55A have a unique power-on delay circuit. This feature allows compatibility with certain microprocessor devices that cannot withstand clock input toggling until full supply voltage is reached. Upon application of power to the V_{DD} pins, the W48C54A/55A output clocks are delayed (held LOW) for approximately 15 ms, after which they assume normal operation.

Functional Description

The Functional Block Diagram shows the reference clock source can be a crystal connected across the X1 and X2 input pins, alternatively input clock connected to the X1 input pin. In the latter case, the X2 pin is left open. With either source as reference, both the W48C54A and W48C55A generate all necessary clocks at their respective frequencies to drive the specified clocks. To provide the broadest possible range of frequencies typically required for CPU mother-board designs, the target frequencies can be selected via up to four select inputs. Consult the appropriate tables for the clock selection range. In addition, the W48C54A/55A can provide rebuffered reference clock outputs.

Both the W48C54A and W48C55A offer smooth transitions when changing CPU/2XCPU output frequency. This feature can best be used by power management systems where it is frequently necessary to slow down the clock to conserve power. By controlling the rate of frequency transition, both devices are designed to be compatible with Intel® cycle-to-cycle processor timing specifications.

Power down capability is available in selected versions of the W48C54A and W48C55A. When $\overline{PD}$ is active (LOW), the device is placed in a standby mode during which power dissipation is at its minimum; all clock outputs are forced LOW. Partial power is also an available option, wherein selected outputs are disabled or enabled according to a logic input.

Table 1. Frequency Selection for W48C54A

		-05	-09	-59
FS1	**FS0**	**CPU (MHz)**	**CPU (MHz)**	**CPU (MHz)**
0	0	47.000	54.000	50.113
0	1	47.000	18.800	40.568
1	0	27.000	27.000	66.817
1	1	36.000	36.000	33.409
Input/REF		20	20	14.318

Table 2. Frequency Selection for W48C55A

			-61	
FS2	**FS1**	**FS0**	**2XCPU (MHz)**	**CPU (MHz)**
0	0	0	8	4
0	0	1	16	8
0	1	0	32	16
0	1	1	40	20
1	0	0	50	25
1	0	1	66.66	33.33
1	1	0	80	40
1	1	1	100[1]	50[1]

Note:
1. Not guaranteed when V_{DD} < 4.5V.

Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

Parameter	Description	Rating	Unit
V_{DD}	V_{DD} referenced to GND	7.0	V
T_{STG}	Storage Temperature	–40 to +150	°C
T_A	Operating Temperature	0 to +70	°C
V_{IN}	V on I/O ref to GND	GND–5.0 to V_{DD}+5.0	V
P_D	Power Dissipation	0.5	W

Electrical Characteristics

5.0V DC Characteristics ($0°C < T_A < 70°C$, $V_{DD} = 5.0V \pm 10\%$)

Parameter	Description	Test Condition	Min	Typ	Max	Unit
V_{IL}	Input Low Voltage	V_{DD} = 5.0V			0.8	V
V_{IH}	Input High Voltage	V_{DD} = 5.0V	2.0			V
I_{IL}	Input Low Current[2]	V_{IN} = 0V			–100	µA
I_{IH}	Input High Current	$V_{IN} = V_{DD}$			10	µA
V_{OL}	Output Low Voltage	I_{OL} = 4 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = –1 mA, V_{DD}=5V	V_{DD}–0.4			V
V_{OH}	Output High Voltage	I_{OH} = –4 mA, V_{DD}=5V	V_{DD}–0.8			V
I_{DD}	Supply Current[3]	No load		25	40	mA
F_D	Output Frequency Change[4]	Over supply and temperature		0.002	0.01	%
I_{SC}	Short Circuit Current	Each output clock	25	40		mA
I_{DDSTBY}	Supply Current, Power Down[5]			300		µA
C_{IN}	Input Capacitance	Except pins X1, X2			10	pF
C_L	Load Capacitance	Pins X1 and X2		20		pF
R_P	Pull-up Resistor Value	Except X1, X2		250		kΩ

Notes:
2. Includes pull-up resistor.
3. No output load capacitance, CPU or 2XCPU running at 50 MHz. Power supply current can change with different mask configuration.
4. Consideration of reference crystal shift only.
5. With full chip power-down pin LOW.

5.0V AC Characteristics ($0°C < T_A < 70°C$, $V_{DD} = 5.0V \pm 10\%$)

Parameter	Description	Conditions	Min	Typ	Max	Unit
T_{ICR}	Input Clock Rise Time				20	ns
T_{ICF}	Input Clock Fall Time				20	ns
T_R	Output Rise Time, 0.8 to 2.0V	25-pF load		1	2	ns
T_R	Rise Time, 20% to 80% V_{DD}	25-pF load		2	4	ns
T_F	Output Fall Time, 2.0 to 0.8V	25-pF load		1	2	ns
T_F	Fall Time, 80% to 20% V_{DD}	25-pF load		2	4	ns
D_T	Duty Cycle, All Outputs	25-pF load	40/60	50/50	60/40	%
T_{JAB}	Jitter, Absolute	16–100 MHz clocks			700	ps
F_I	Input Frequency			14.318		MHz
T_{SK}	Clock Skew between CPU and 2XCPU outputs				1.0	ns
T_{FT}	Frequency Transition Time	From 8–100 MHz		40	50	ms

3.3V DC Characteristics ($0°C < T_A < 70°C$, $V_{DD} = 3.3V \pm 10\%$)

Parameter	Description	Test Condition	Min	Typ	Max	Unit
V_{IL}	Input Low Voltage	$V_{DD} = 3.3V$			$0.15*V_{DD}$	V
V_{IH}	Input High Voltage	$V_{DD} = 3.3V$	$0.7*V_{DD}$			V
I_{IL}	Input Low Current[2]	$V_{IN} = 0V$			–100	µA
I_{IH}	Input High Current	$V_{IN} = V_{DD}$			10	µA
V_{OL}	Output Low Voltage	$I_{OL} = 4$ mA			0.4	V
V_{OH}	Output High Voltage	$I_{OH} = –4$ mA, V_{DD}=3.3V	2.4			V
I_{DD}	Supply Current[3]	No load		20	35	mA
F_D	Output Frequency Change[4]	Over supply and temperature		0.002	0.01	%
I_{SC}	Short Circuit Current	Each output clock	25	40		mA
C_{IN}	Input Capacitance	Except pins X1, X2			10	pF
C_L	Load Capacitance	Pins X1 and X2		20		pF
R_P	Pull-up Resistor Value	Except X1, X2		250		kΩ

3.3V AC Characteristics ($0°C < T_A < 70°C$, $V_{DD} = 3.3V \pm 10\%$)

Parameter	Description	Conditions	Min	Typ	Max	Unit
T_{ICR}	Input Clock Rise Time				20	ns
T_{ICF}	Input Clock Fall Time				20	ns
T_R	Rise Time, 20% to 80% V_{DD}	15-pF load		2	4	ns
T_F	Fall Time, 80% to 20% V_{DD}	15-pF load		2	4	ns
D_T	Duty Cycle, All Outputs	15-pF load	40/60	50/50	60/40	%
T_{JAB}	Jitter, Absolute	16–80 MHz clocks			700	ps
F_I	Input Frequency			14.318		MHz
T_{SK}	Clock Skew between CPU and 2XCPU outputs				1.0	ns
T_{FT}	Frequency Transition Time	From 8–100 MHz		40	50	ms

Recommended Board Layout: W48C54A/55A

For optimum performance in system applications, the power supply decoupling scheme shown in *Figure 1* should be used. All GND pins are connected to the ground plane.

V_{DD} decoupling is important to both reduce phase jitter and EMI radiation. The 0.1-µF decoupling capacitors should be placed as close to the V_{DD} pins as possible, otherwise the increased trace inductance will negate its decoupling capability. the 10-µF decoupling capacitor shown should be a tantalum type. For further EMI protection, the V_{DD} connection can be made via a ferrite bead, as shown.

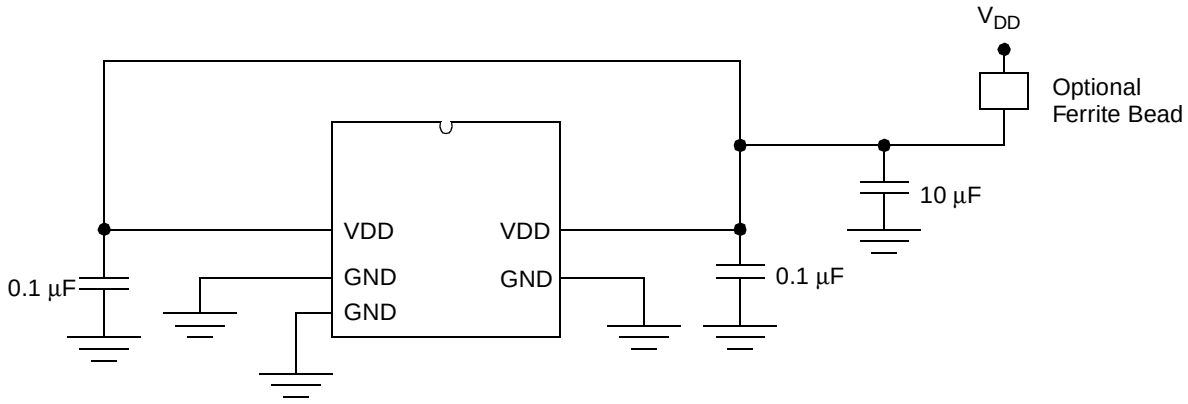


Figure 1. Recommended Circuit Configuration

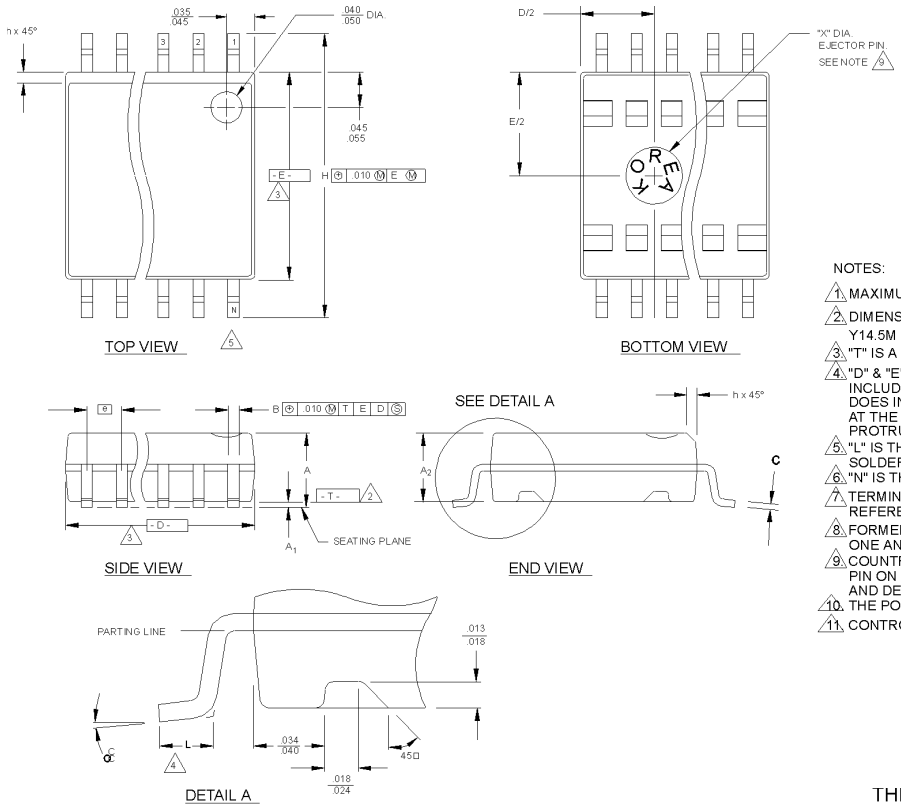
Ordering Information

Ordering Code	Freq. Mask Code	Package Name	Package Type
W48C54A	05, 08, 09, 59	G	16-pin Plastic SOIC (150-mil)
W48C55A	61	G	20-pin Plastic SOIC (300-mil)

Document #: 38-00803

Package Diagrams

20-Pin Small Outline Integrated Circuit (SOIC, 300-mil)



NOTES:

1. MAXIMUM DIE THICKNESS ALLOWABLE IS .025.
2. DIMENSIONING & TOLERANCES PER ANSI. Y14.5M - 1982.
3. "T" IS A REFERENCE DATUM.
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DOES INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE MOLD PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. "N" IS THE NUMBER OF TERMINAL POSITIONS.
7. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
8. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .003 INCHES AT SEATING PLANE.
9. COUNTRY OF ORIGIN LOCATION AND EJECTOR PIN ON PACKAGE BOTTOM IS OPTIONAL AND DEPEND ON ASSEMBLY LOCATION.
10. THE POCKETS ON THE BOTTOM ARE OPTIONAL.
11. CONTROLLING DIMENSION: INCHES.

THIS TABLE IN INCHES

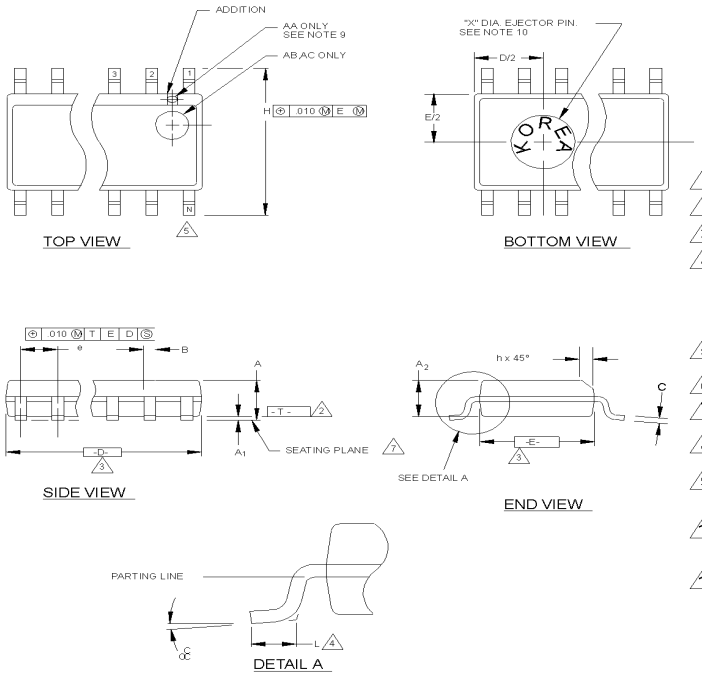
SYMBOL	COMMON DIMENSIONS			NOTE	NOTE VARIATIONS	3 D			5 N
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
A	.097	.101	.104		AA	.402	.407	.412	16
A_1	.0050	.009	.0115		AB	.451	.456	.461	18
A_2	.090	.092	.094		AC	.500	.505	.510	20
B	.014	.016	.019		AD	.602	.607	.612	24
C	.0091	.010	.0125		AE	.701	.706	.711	28
D	SEE VARIATIONS			3					
E	.292	.296	.299						
e	.050 BSC								
H	.400	.406	.410						
h	.010	.013	.016						
L	.024	.032	.040						
N	SEE VARIATIONS			5					
α	0°	5°	8°						
X	.085	.093	.100						

THIS TABLE IN MILLIMETERS

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE VARIATIONS	3 D			5 N
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
A	2.46	2.56	2.64		AA	10.21	10.34	10.46	16
A_1	0.127	0.22	0.29		AB	11.46	11.58	11.71	18
A_2	2.29	2.34	2.39		AC	12.70	12.83	12.95	20
B	0.35	0.41	0.48		AD	15.29	15.42	15.54	24
C	0.23	0.25	0.32		AE	17.81	17.93	18.06	28
D	SEE VARIATIONS			3					
E	7.42	7.52	7.59						
e	1.27 BSC								
H	10.16	10.31	10.41						
h	0.25	0.33	0.41						
L	0.61	0.81	1.02						
N	SEE VARIATIONS			5					
α	0°	5°	8°						
X	2.16	2.36	2.54						

Package Diagrams (continued)

16-Pin Small Outline Integrated Circuit (SOIC, 150-mil)



NOTES:

1. MAXIMUM DIE THICKNESS ALLOWABLE IS .015.
2. DIMENSIONING & TOLERANCES PER ANSI.Y14.5M - 1982.
3. "T" IS A REFERENCE DATUM.
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DOES INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE MOLD PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. "N" IS THE NUMBER OF TERMINAL POSITIONS.
7. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
8. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .003 INCHES AT SEATING PLANE.
9. THE APPEARANCE OF PIN #1 I.D ON THE 8 LD IS OPTIONAL, ROUND TYPE ON SINGLE LEADFRAME AND RECTANGULAR TYPE ON MATRIX LEADFRAME.
10. COUNTRY OF ORIGIN LOCATION AND EJECTOR PIN ON PACKAGE BOTTOM IS OPTIONAL AND DEPEND ON ASSEMBLY LOCATION.
11. CONTROLLING DIMENSION: INCHES.

THIS TABLE IN INCHES

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE	3			5
					VARI-	D			N
	MIN.	NOM.	MAX.		ATIONS	MIN.	NOM.	MAX.	
A	.061	.064	.068		AA	.189	.194	.196	8
A_1	.004	.006	.0098		AB	.337	.342	.344	14
A_2	.055	.058	.061		AC	.386	.391	.393	16
B	.0138	.016	.0192						
C	.0075	.008	.0098						
D	SEE VARIATIONS			3					
E	.150	.155	.157						
e	.050 BSC								
H	.230	.236	.244						
h	.010	.013	.016						
L	.016	.025	.035						
N	SEE VARIATIONS			5					
α	0°	5°	8°						
X	.085	.093	.100						

THIS TABLE IN MILLIMETERS

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE	3			5
					VARI-	D			N
	MIN.	NOM.	MAX.		ATIONS	MIN.	NOM.	MAX.	
A	1.55	1.63	1.73		AA	4.80	4.93	4.98	8
A_1	0.127	0.15	0.25		AB	8.58	8.69	8.74	14
A_2	1.40	1.47	1.55		AC	9.80	9.93	9.98	16
B	0.35	0.41	0.49						
C	0.19	0.20	0.25						
D	SEE VARIATIONS			3					
E	3.81	3.94	3.99						
e	1.27 BSC								
H	5.84	5.99	6.20						
h	0.25	0.33	0.41						
L	0.41	0.64	0.89						
N	SEE VARIATIONS			5					
α	0°	5°	8°						
X	2.16	2.36	2.54						