## GENERAL DESCRIPTION

N -channel enhancement mode logic level field-effect power transistor in a plastic envelope available in TO220AB and SOT404 . Using 'trench' technology which features very low on-state resistance. It is intended for use in automotive and general purpose switching applications.

QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | UNIT |
| :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {DS }}$ | Drain-source voltage | 100 | V |
| $\mathrm{I}_{\mathrm{D}}$ | Drain current (DC) | 23 | A |
| $\mathrm{P}_{\text {tot }}$ | Total power dissipation | 99 | W |
| $\mathrm{T}_{\mathrm{j}}$ | Junction temperature | 175 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}$ | Drain-source on-state resistance $\quad \mathrm{V}_{\mathrm{GS}}=5 \mathrm{~V}$ | 75 | $\mathrm{m} \Omega$ |
|  | $\mathrm{V}_{\mathrm{GS}}=10 \mathrm{~V}$ | 55 | $\mathrm{m} \Omega$ |

## PINNING

TO220AB \& SOT404

| PIN | DESCRIPTION |
| :---: | :--- |
| 1 | gate |
| 2 | drain |
| 3 | source |
| tab $/ \mathrm{mb}$ | drain |

PIN CONFIGURATION


SYMBOL


## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
| :--- | :--- | :--- | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{DS}}$ | Drain-source voltage | - | - | 100 | V |
| $\mathrm{~V}_{\mathrm{DGR}}$ | Drain-gate voltage | $\mathrm{R}_{\mathrm{GS}}=20 \mathrm{k} \Omega$ | - | 100 | V |
| $\pm \mathrm{V}_{\mathrm{GS}}$ | Gate-source voltage | - | - | 15 | V |
| $\mathrm{I}_{\mathrm{D}}$ | Drain current (DC) | $\mathrm{T}_{\mathrm{mb}}=25{ }^{\circ} \mathrm{C}$ | - | 23 | A |
| $\mathrm{I}_{\mathrm{D}}$ | Drain current (DC) | $\mathrm{T}_{\mathrm{mb}}=100{ }^{\circ} \mathrm{C}$ | - | 16 | A |
| $\mathrm{I}_{\mathrm{DM}}$ | Drain current (pulse peak value) | $\mathrm{T}_{\mathrm{mb}}=25{ }^{\circ} \mathrm{C}$ | - | 91 | A |
| $\mathrm{P}_{\text {tot }}$ | Total power dissipation | $\mathrm{T}_{\mathrm{mb}}=25{ }^{\circ} \mathrm{C}$ | - | 98 | W |
| $\mathrm{~T}_{\text {stg }}, \mathrm{T}_{\mathrm{j}}$ | Storage \& operating temperature | - | -55 | 175 | ${ }^{\circ} \mathrm{C}$ |

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | TYP. | MAX. | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{R}_{\text {th } j \text {-mb }}$ | Thermal resistance junction to mounting base | - |  | 1.5 | K/W |
| $\mathrm{R}_{\text {th } j-\mathrm{a}}$ | Thermal resistance junction to ambient(TO220AB) | in free air | 60 | - | K/W |
| $\mathrm{R}_{\text {th } \mathrm{j}-\mathrm{a}}$ | Thermal resistance junction to ambient(SOT404) | Minimum footprint, FR4 board | 50 | - | K/W |

TrenchMOS ${ }^{\text {TM }}$ transistor

## STATIC CHARACTERISTICS

$\mathrm{T}_{\mathrm{j}}=25^{\circ} \mathrm{C}$ unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {(BR)DSs }}$ <br> $\mathrm{V}_{\mathrm{GS}(\mathrm{T})}$ | Drain-source breakdown voltage <br> Gate threshold voltage |  | 100 | - | - | V |
|  |  | $\mathrm{V}_{\mathrm{GS}}=0 \mathrm{~V} ; \mathrm{I}_{\mathrm{D}}=0.25 \mathrm{~mA} ; \mathrm{T}_{\mathrm{j}}=-55^{\circ} \mathrm{C}$ | 89 | - | - | V |
|  |  | $\begin{array}{ll}V_{D S}=V_{G S} ; \mathrm{I}_{\mathrm{D}}=1 \mathrm{~mA} & \\ & \mathrm{~T}_{\mathrm{j}}=175^{\circ} \mathrm{C} \\ & \mathrm{T}_{\mathrm{j}}=-55^{\circ} \mathrm{C}\end{array}$ | 1 | 1.5 | 2.0 | V |
|  |  |  | 0.5 | - | - | V |
|  |  |  | - | - | 2.3 | V |
| $\mathrm{I}_{\text {DSS }}$ | Zero gate voltage drain current | $\mathrm{V}_{\text {SS }}=100 \mathrm{~V} ; \mathrm{V}_{G S}=0 \mathrm{~V} ;$ | - | 0.05 | 10 | $\mu \mathrm{A}$ |
|  |  | , $\mathrm{T}_{\mathrm{j}}=175^{\circ} \mathrm{C}$ | - | - | 500 | $\mu \mathrm{A}$ |
| $\mathrm{I}_{\mathrm{GSS}}$ $\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}$ | Gate source leakage current Drain-source on-state resistance | $\mathrm{V}_{\mathrm{GS}}= \pm 10 \mathrm{~V} ; \mathrm{V}_{\mathrm{DS}}=0 \mathrm{~V}$ | - | 2 | 100 | nA |
|  |  | $\mathrm{V}_{\mathrm{GS}}=5 \mathrm{~V} ; \mathrm{I}_{\mathrm{D}}=10 \mathrm{~A}$ | - | 60 | 75 | $\mathrm{m} \Omega$ |
|  |  | $T_{j}=175^{\circ} \mathrm{C}$ | - | - | 188 | $\mathrm{m} \Omega$ |
|  |  | $\mathrm{V}_{\mathrm{GS}}=10 \mathrm{~V} ; \mathrm{I}_{\mathrm{D}}=10 \mathrm{~A}$ | - | 55 | 72 | $\mathrm{m} \Omega$ |
|  |  | $\mathrm{V}_{\mathrm{GS}}=4.5 \mathrm{~V} ; \mathrm{I}_{\mathrm{D}}=10 \mathrm{~A}$ | - | 61 | 84 | $\mathrm{m} \Omega$ |

## DYNAMIC CHARACTERISTICS

$\mathrm{T}_{\mathrm{mb}}=25^{\circ} \mathrm{C}$ unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & \mathrm{C}_{\text {iss }} \\ & \mathrm{C}_{\text {oss }} \\ & \mathrm{C}_{\text {rss }} \end{aligned}$ | Input capacitance Output capacitance Feedback capacitance | $\mathrm{V}_{\mathrm{GS}}=0 \mathrm{~V} ; \mathrm{V}_{\mathrm{DS}}=25 \mathrm{~V} ; \mathrm{f}=1 \mathrm{MHz}$ | - | $\begin{gathered} 1278 \\ 129 \\ 88 \end{gathered}$ | $\begin{gathered} \hline 1704 \\ 155 \\ 120 \end{gathered}$ | $\begin{aligned} & \mathrm{pF} \\ & \mathrm{pF} \\ & \mathrm{pF} \end{aligned}$ |
| $\begin{aligned} & \mathrm{t}_{\mathrm{don}} \\ & \mathrm{t}_{\mathrm{r}} \\ & \mathrm{t}_{\mathrm{doff}} \\ & \mathrm{t}_{\mathrm{f}} \end{aligned}$ | Turn-on delay time Turn-on rise time Turn-off delay time Turn-off fall time | $\begin{aligned} & \mathrm{V}_{\mathrm{DD}}=30 \mathrm{~V} ; \mathrm{R}_{\text {load }}=1.2 \Omega ; \\ & \mathrm{V}_{\mathrm{GS}}=5 \mathrm{~V} ; \mathrm{R}_{\mathrm{G}}=10 \Omega \end{aligned}$ | - | $\begin{gathered} 13 \\ 120 \\ 58 \\ 57 \end{gathered}$ | $\begin{gathered} 20 \\ 168 \\ 87 \\ 86 \end{gathered}$ | ns <br> ns <br> ns <br> ns |
| $\mathrm{L}_{\mathrm{d}}$ | Internal drain inductance | Measured from drain lead 6 mm from package to centre of die | - | 4.5 | - | nH |
| $\mathrm{L}_{\mathrm{d}}$ | Internal drain inductance | Measured from contact screw on tab to centre of die(TO220AB) | - | 3.5 | - | nH |
| $\mathrm{L}_{\mathrm{d}}$ | Internal drain inductance | Measured from upper edge of drain tab to centre of die(SOT404) | - | 2.5 | - | nH |
| $\mathrm{L}_{\mathrm{s}}$ | Internal source inductance | Measured from source lead to source bond pad | - | 7.5 | - | nH |

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS
$\mathrm{T}_{\mathrm{j}}=25^{\circ} \mathrm{C}$ unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
| :--- | :--- | :--- | :---: | :---: | :---: | :---: |
| $\mathrm{I}_{\mathrm{DR}}$ | Continuous reverse drain |  | - | - | 23 | A |
| $\mathrm{I}_{\mathrm{DRM}}$ | current | Pulsed reverse drain current |  |  |  |  |
| $\mathrm{V}_{\mathrm{SD}}$ | Diode forward voltage | $\mathrm{I}_{\mathrm{F}}=10 \mathrm{~A} ; \mathrm{V}_{\mathrm{GS}}=0 \mathrm{~V}$ | - | - | 92 | A |
|  |  | $\mathrm{I}_{\mathrm{F}}=23 \mathrm{~A} ; \mathrm{V}_{\mathrm{GS}}=0 \mathrm{~V}$ | - | 0.85 | 1.2 | V |
| $\mathrm{t}_{\mathrm{rr}}$ | Reverse recovery time | $\mathrm{I}_{\mathrm{F}}=23 \mathrm{~A} ;-\mathrm{dI} \mathrm{I}_{\mathrm{F}} / \mathrm{dt}=100 \mathrm{~A} / \mu \mathrm{s} ;$ | - | 63 | - | ns |
| $\mathrm{Q}_{\mathrm{rr}}$ | Reverse recovery charge | $\mathrm{V}_{\mathrm{GS}}=-10 \mathrm{~V} ; \mathrm{V}_{\mathrm{R}}=30 \mathrm{~V}$ | - | 0.22 | - | $\mu \mathrm{C}$ |

## AVALANCHE LIMITING VALUE

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
| :--- | :--- | :--- | :---: | :---: | :---: | :---: |
| $\mathrm{W}_{\mathrm{DSs}}{ }^{1}$ | Drain-source non-repetitive <br> unclamped inductive turn-off <br> energy | $\mathrm{I}_{\mathrm{D}}=14.2 \mathrm{~A} ; \mathrm{V}_{\mathrm{DD}} \leq 25 \mathrm{~V} ;$ <br> $\mathrm{V}_{\mathrm{GS}}=5 \mathrm{~V} ; \mathrm{R}_{\mathrm{GS}}=50 \Omega ; \mathrm{T}_{\mathrm{mb}}=25{ }^{\circ} \mathrm{C}$ | - | - | 100 | mJ |



Fig.1. Normalised power dissipation. $P D \%=100 \cdot P_{D} / P_{D 25^{\circ} \mathrm{C}}=f\left(T_{m b}\right)$


Fig.2. Normalised continuous drain current. $I D \%=100 \cdot I_{D} / I_{D 25^{\circ} \mathrm{C}}=f\left(T_{m b}\right)$; conditions: $V_{G S} \geq 5 \mathrm{~V}$


Fig.3. Safe operating area. $T_{m b}=25^{\circ} \mathrm{C}$ $I_{D} \& I_{D M}=f\left(V_{D S}\right) ; I_{D M}$ single pulse; parameter $t_{p}$


Fig.4. Transient thermal impedance.
$Z_{t h j-m b}=f(t) ;$ parameter $D=t_{p} / T$

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Fig.5. Typical output characteristics, $T_{j}=25^{\circ} \mathrm{C}$. $I_{D}=f\left(V_{D S}\right)$; parameter $V_{G S}$


Fig.6. Typical on-state resistance, $T_{j}=25^{\circ} \mathrm{C}$. $R_{D S(O N)}=f\left(V_{G S}\right)$; conditions: $I_{D}=25 \mathrm{~A}$;


Fig.7. Typical on-state resistance, $T_{j}=25^{\circ} \mathrm{C}$. $R_{D S(O N)}=f\left(V_{G S}\right)$; conditions: $I_{D}=25 \mathrm{~A}$;


Fig.8. Typical on-state resistance, $T_{j}=25{ }^{\circ} \mathrm{C}$.
$R_{D S(O N)}=f\left(V_{G S}\right)$; conditions: $I_{D}=25 \mathrm{~A}$;


Fig.9. Typical transfer characteristics. $I_{D}=f\left(V_{G S}\right)$; conditions: $V_{D S}=25 \mathrm{~V}$; parameter $T_{j}$


Fig.10. Typical transconductance, $T_{j}=25^{\circ} \mathrm{C}$. $g_{f s}=f\left(I_{D}\right)$; conditions: $V_{D S}=25 \mathrm{~V}$

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Fig.11. Normalised drain-source on-state resistance. $a=R_{D S(O N)} / R_{D S(O N) 25{ }^{\circ} \mathrm{C}}=f\left(T_{j}\right) ; I_{D}=25 A ; V_{G S}=5 \mathrm{~V}$


Fig.12. Gate threshold voltage.
$V_{G S(T O)}=f\left(T_{j}\right)$; conditions: $I_{D}=1 \mathrm{~mA} ; V_{D S}=V_{G S}$


Fig.13. Sub-threshold drain current.
$I_{D}=f\left(V_{G S}\right) ;$ conditions: $T_{j}=25^{\circ} \mathrm{C} ; V_{D S}=V_{G S}$


Fig.14. Typical capacitances, $C_{\text {iss }}, C_{\text {oss, }}, C_{\text {rss }}$. $C=f\left(V_{D S}\right)$; conditions: $V_{G S}=0 \mathrm{~V} ; f=1 \mathrm{MHz}$


Fig.15. Typical turn-on gate-charge characteristics. $V_{G S}=f\left(Q_{G}\right)$; conditions: $I_{D}=25$ A; parameter $V_{D S}$


Fig.16. Typical reverse diode current. $I_{F}=f\left(V_{S D S}\right)$; conditions: $V_{G S}=0 \mathrm{~V}$; parameter $T_{j}$


Fig.17. Normalised avalanche energy rating. $W_{D S s} \%=f\left(T_{m b}\right)$; conditions: $I_{D}=75 \mathrm{~A}$


Fig.18. Avalanche energy test circuit.

$$
W_{D S S}=0.5 \cdot L I_{D}^{2} \cdot B V_{D S S} /\left(B V_{D S S}-V_{D D}\right)
$$



Fig.19. Maximum permissible repetitive avalanche current $\left(I_{A V}\right)$ versus avalanche time $\left(t_{A V}\right)$ for unclamped inductive loads.


Fig.20. Switching test circuit.

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## MECHANICAL DATA



Fig.21. SOT78 (TO220AB); pin 2 connected to mounting base.

## Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Refer to mounting instructions for SOT78 (TO220) envelopes.
3. Epoxy meets UL94 V0 at 1/8".

## MECHANICAL DATA



Fig.22. SOT404 surface mounting package. Centre pin connected to mounting base.

## Notes

1. This product is supplied in anti-static packaging. The gate-source input must be protected against static discharge during transport or handling.
2. Refer to SMD Footprint Design and Soldering Guidelines, Data Handbook SC18.
3. Epoxy meets UL94 V0 at 1/8".

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## MOUNTING INSTRUCTIONS

## Dimensions in mm



Fig.23. SOT404 : soldering pattern for surface mounting.

## DEFINITIONS

| Data sheet status |  |
| :--- | :--- |
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| Limiting values | Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one <br> or more of the limiting values may cause permanent damage to the device. These are stress ratings only and <br> operation of the device at these or at any other conditions above those given in the Characteristics sections of <br> this specification is not implied. Exposure to limiting values for extended periods may affect device reliability. |
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## LIFE SUPPORT APPLICATIONS

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[^0]:    1 For maximum permissible repetitive avalanche current see fig.18.

