CAT35C202/CAT35C202I

2K-Bit SERIAL E²PROM

FEATURES

- High Speed Operation: 1MHz
- Low Power CMOS Technology
- Single 5V Supply
- 128 x 16 or 256 x 8 Selectable Serial Memory
- Self-Timed Write Cycle with Auto-Clear
- RDY/$\overline{\text{BUSY}}$ Pin for End-of-Write Detection
- Hardware and Software Write Protection
- Power-Up Inadvertent Write Protection
- 100,000 Program/Erase Cycles
- 100 Year Data Retention
- Optional High Endurance Device Available

DESCRIPTION

The CAT35C202 and CAT35C202I are 2K bit Serial E²PROM memory devices which can be configured as either 128 registers by 16 bits (ORG pin at V_{CC}) or 256 registers by 8 bits (ORG pin at GND). Each register can be written (or read) serially by using the DI (or DO) pin.

The CAT35C202/CAT35C202I is manufactured using Catalyst's advanced CMOS E²PROM floating gate technology. It is designed to endure 100,000 program/erase cycles and has a data retention of 100 years. The device is available in 8 pin DIP or SO packages.

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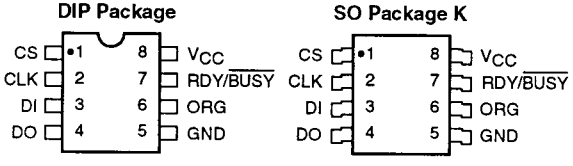
PIN CONFIGURATION



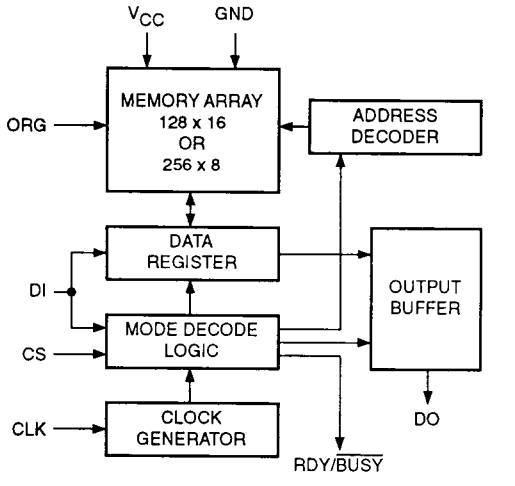
5060 FHD F01

PIN FUNCTIONS

Pin Name	Function
CS	Chip Select
CLK	Clock Input
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	+5V Power Supply
GND	Ground
RDY/$\overline{\text{BUSY}}$	Ready/Busy Status
ORG	Memory Organization

Note: When the ORG pin is connected to V_{CC}, the 128 x 16 organization is selected. When it is connected to ground, the 256 x 8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the 128 x 16 organization.

BLOCK DIAGRAM



5062 FHD F02

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ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... –55°C to +125°C

Storage Temperature ..... –65°C to +150°C

Voltage on Any Pin with Respect to Ground(1) ..... –2.0V to +V_{CC} + 2.0V

V_{CC} with Respect to Ground ..... –2.0V to +7.0V

Package Power Dissipation Capability (Ta = 25°C) 1.0W

Lead Soldering Temperature (10 secs) ..... 300°C

Output Short Circuit Current(2) 100mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N_{END}(3)	Endurance	100,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(3)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(3)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(3)(4)	Latch-up	100		mA	JEDEC Standard 17

D.C. OPERATING CHARACTERISTICS

CAT35C202 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
CAT35C202I T_A = –40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter		Limits Min.	Limits Typ.	Limits Max.	Units	Test Conditions
I_{CC1}	Power Supply Current (Operating)	Comm.			3	mA	DI = 0V, CLK = 5.0V V_{CC} = 5.0V, CS = 5.0V Output Open
		Ind.			4	mA	
I_{CC2}	Power Supply Current (Standby)				100	µA	DI = 0V, CLK = 0V V_{CC} = 5.0V, CS = 0V
I_{LI}	Input Leakage Current				2	µA	V_{IN} = 5.5V
I_{LO}	Output Leakage Current (Including ORG Pin)				10	µA	V_{OUT} = 0V to 5.5V, CS = 0
V_{IH}	High Level Input Voltage		2.0		V_{CC} +1	V	
V_{IL}	Low Level Input Voltage		–0.1		0.8	V	
V_{OH}	High Level Output Voltage		2.4			V	I_{OH} = –400µA
V_{OL}	Low Level Output Voltage				0.4	V	I_{OL} = 2.1 mA

Note:
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} + 2.0V for periods of less than 20ns.
(2) Output shorted for no more than one second. No more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.

INSTRUCTION SET

Instruction	Start Bit	Opcode	Address		Data		Comments
			256 x 8	128 x 16	256 x 8	128 x 16	
READ	1	1000	A7–A0	A6–A0			Read Address A_N–A_0
WRITE	1	X100	A7–A0	A6–A0	D7–D0	D15–D0	Write Address A_N–A_0
EWEN	1	0011	XXXXXXXX	XXXXXXX			Write Enable
EWDS	1	0000	XXXXXXXX	XXXXXXX			Write Disable
ERAL	1	0010	XXXXXXXX	XXXXXXX			Clear All Addresses
WRAL	1	0001	XXXXXXXX	XXXXXXX	D7–D0	D15–D0	Write All Addresses

A.C. CHARACTERISTICS

CAT35C202 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
CAT35C202I T_A = –40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
t_{CSS}	CS Setup Time	50			ns	
t_{CSH}	CS Hold Time	50			ns	
t_{DIS}	DI Setup Time	100			ns	C_L = 100pF
t_{DIH}	DI Hold Time	100			ns	V_{OL} = 0.8V, V_{OH} = 2.0V
t_{PD1}	Output Delay to 1			500	ns	V_{IL} = 0.45V, V_{IH} = 2.4V
t_{PD0}	Output Delay to 0			500	ns	
t_{HZ}(3)	Output Delay to High-Z			100	ns	C_L = 100pF
t_{EW}	Program/Erase Pulse Width			10	ms	
t_{CKH}	Minimum Clock High Time	250			ns	
t_{CKL}	Minimum Clock Low Time	250			ns	
t_{SV}	RDY/$\overline{\text{BUSY}}$ Delay to Status Valid			500	ns	C_L = 100pF
f_{CLK}	Maximum Clock Frequency	DC		1	MHz	

Note:
(3) This parameter is tested initially and after a design or process change that affects the parameter.

DEVICE OPERATION

The CAT35C202/CAT35C202I is a 2048 bit nonvolatile memory intended for use with industry standard microprocessors. The CAT35C202/CAT35C202I can be organized as either 128 registers by 16 bits, or as 256 registers by 8 bits. Six 12 bit instructions (13 bit instruction in 128 x 16 organization) control the reading, writing and erase operations of the device. The CAT35C202/CAT35C202I operates on a single 5V supply and will generate on chip, the high voltage required during any write operation. Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normally in a high impedance state except when reading data from the device. The ready/busy status can be determined after a write operation by polling the RDY/$\overline{\text{BUSY}}$ pin; a low level on this pin indicates that the write operation is not completed, while a high level indicates that the WRITE, ERAL or WRAL operation has been completed and the device is ready for the next instruction.

The format for all instructions sent to the CAT35C202/CAT35C202I is a logical "1" start bit, a 4 bit opcode, a 7 bit address (8 bit address when organized as 256 x 8), and for write operations a 16 bit data field (8 bit data field when organized as 256 x 8). At power-down, when V_{CC} falls below a threshold of approximately 3.5V, the data protection circuitry inhibits all erase and write instructions and a write disable (EWDS) is executed internally.

Figure 1. Synchronous Data Timing(5)

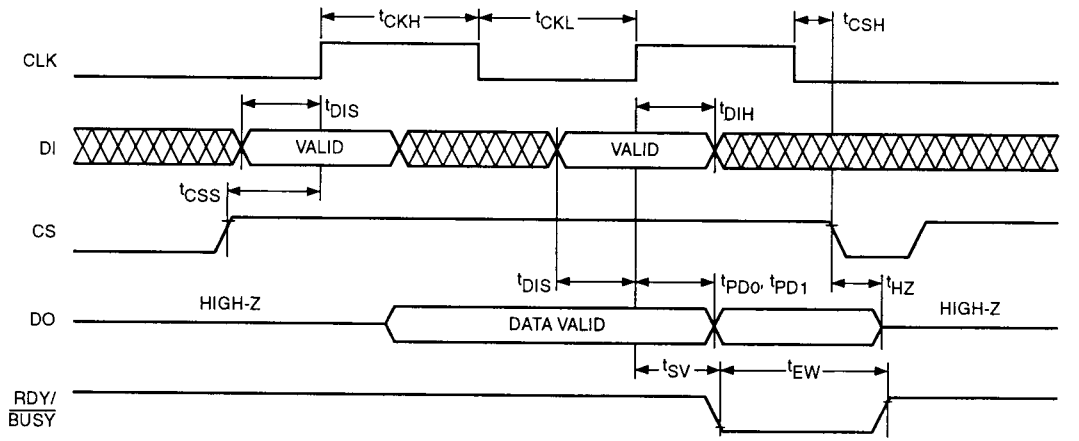
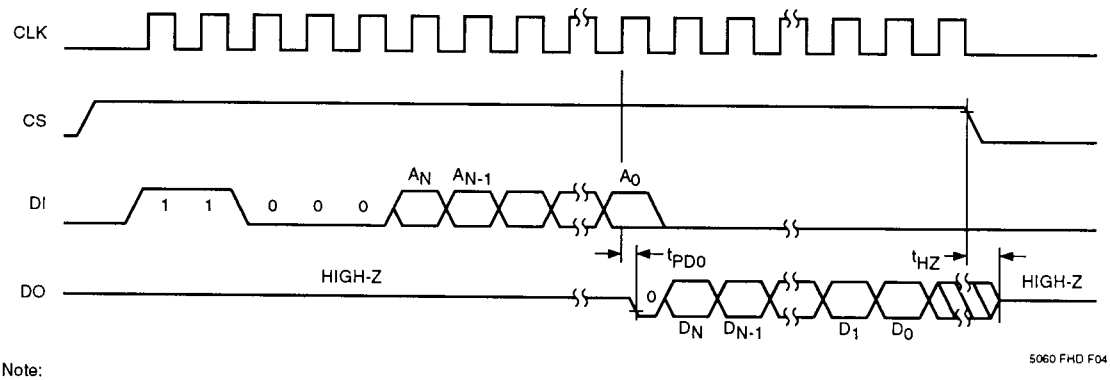


Figure 2. Read Instruction Timing(5)



Note:
(5) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A7 and DN = D7. When x16 organization is selected, AN = A6 and DN = D15.

Read

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the CAT35C202/CAT35C202I will come out of the high impedance state and, after sending an initial dummy zero bit (after a delay of t_{PDO} from the positive edge of the A_0 clock), will begin shifting out the data addressed. The output data bits will toggle on the rising edge of the clock and are stable after the specified time delay (t_{PDO} or t_{PD1}). DO returns to High-Z after a delay of t_{HZ} from the negative going edge of CS.

Erase/Write Enable and Disable

The CAT35C202/CAT35C202I powers up in the write disabled state. Any write after power-up or after a EWDS (write disable) instruction must first be preceded by the EWEN (write enable) instruction. Once the write instruction is enabled, it will remain enabled until power to the device is removed, or the EWEN instruction is sent. The EWEN instruction can be used to disable all CAT35C202/CAT35C202I write and clear instructions, and will prevent any accidental writing or clearing of the device. Data can be read normally from the device regardless of the write enable/disable status.

Write

After receiving a WRITE command, address and data, the RDY/$\overline{BUSY}$ pin goes low (after a delay of t_{SV} from the negative edge of the D_0 clock) indicating the self-clocking program/erase cycle is in progress. The program/erase pulse width (t_{EW}) is timed from the negative clock edge of the last data bit (D_0) and its completion is indicated by the RDY/$\overline{BUSY}$ pin returning to a high level. The clocking of the CLK pin is not necessary after the device has entered the self clocking mode. Since this device features Auto-Clear before write, it is NOT necessary to erase a memory location before the WRITE command is sent.

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Figure 3. Write Instruction Timing(5)

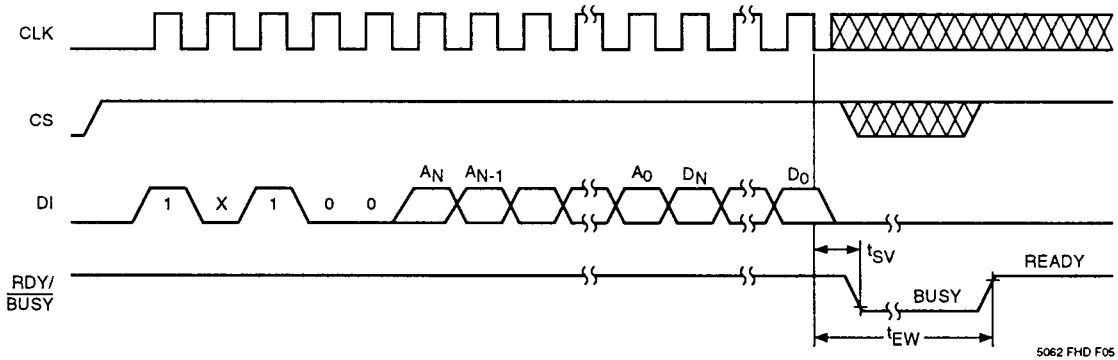
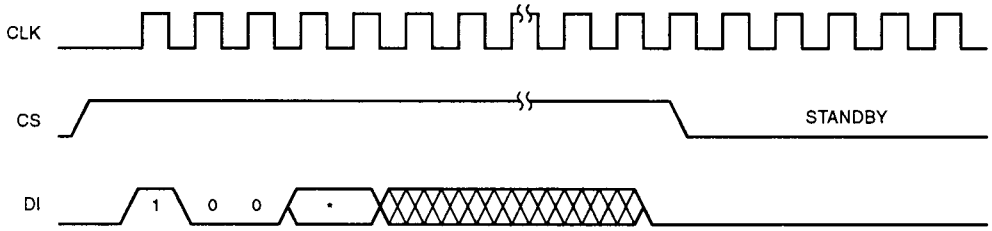


Figure 4. EWEN/EWDS Instruction Timing(5)



Note:
(5) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A7 and DN = D7. When x16 organization is selected, AN = A6 and DN = D15.

Erase All

After receiving an ERAL command and address the RDY/$\overline{BUSY}$ pin goes low (after a delay of t_{SV} from the negative edge of the D_0 clock) indicating the self-clocking program/erase cycle is in progress. The program/erase pulse width (t_{EW}) is timed from the negative clock edge of the last don't care bit and its completion is indicated by the RDY/$\overline{BUSY}$ pin returning to a high level. The clocking of the CLK pin is not necessary after the device has entered the self-clocking mode. Once cleared, the contents of all memory bits return to a logical "1" state.

Write All

Upon receiving a WRAL command, address and data, the RDY/$\overline{BUSY}$ pin goes low (after a delay of t_{SV} from the negative edge of the D_0 clock) indicating the self-clocking program/erase cycle is in progress. The program/erase pulse width (t_{EW}) is timed from the negative edge of the last data bit (D_0) and its completion is indicated by the RDY/$\overline{BUSY}$ pin returning to a high level. The clocking of the CLK pin is not necessary after the device has entered the self clocking mode. It IS necessary for all memory locations to be cleared before the WRAL command is executed.

Figure 5. ERAL Instruction Timing(5)

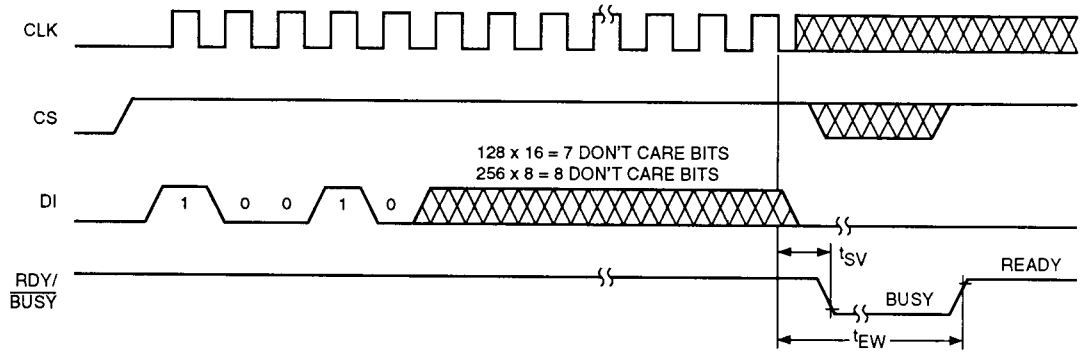
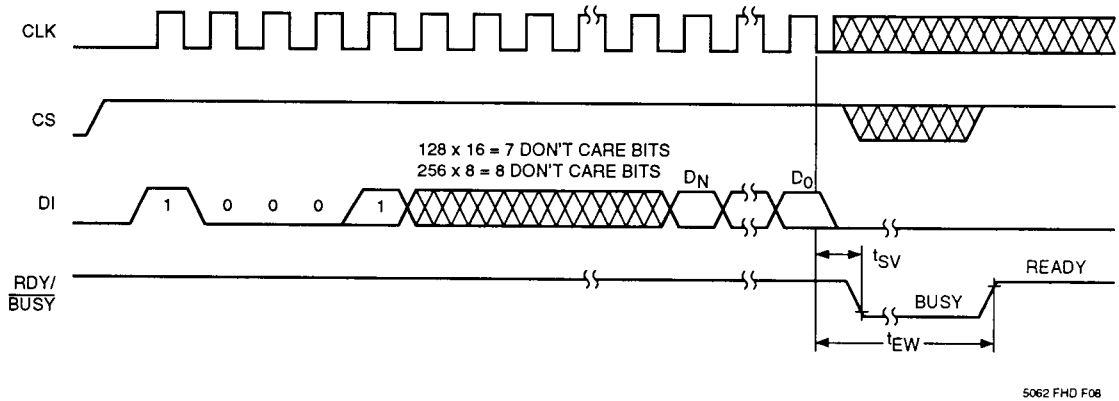


Figure 6. WRAL Instruction Timing(5)



Note:
(5) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A7 and DN = D7. When x16 organization is selected, AN = A6 and DN = D15.