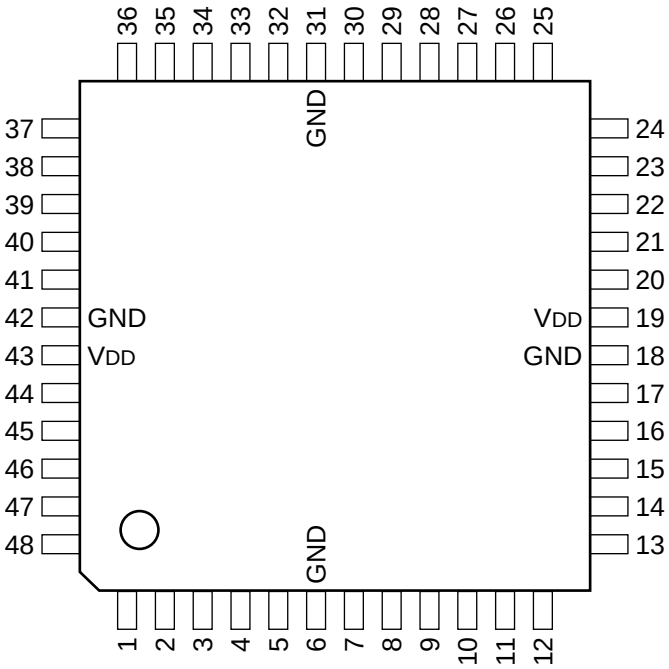
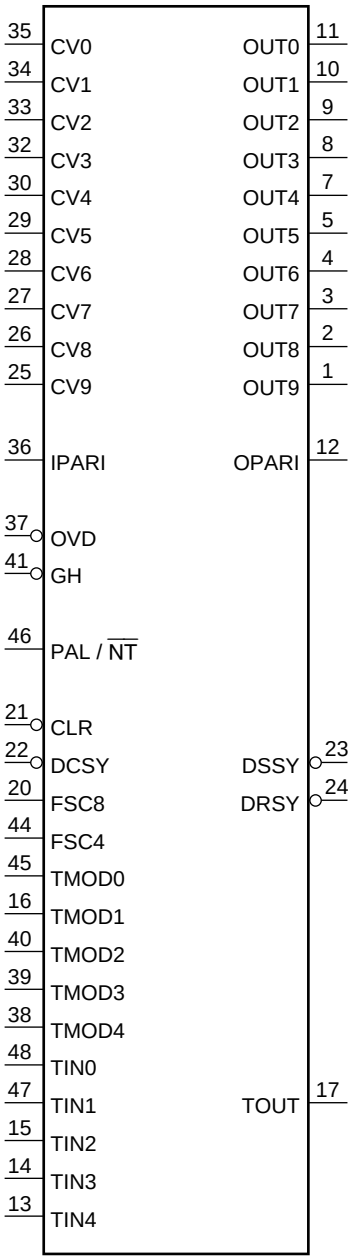
C-MOS 10-BIT PEDESTAL LEVEL REPLACEMENT OF COMPOSITE SIGNAL

—TOP VIEW—



PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	O	OUT9	13	I	TIN4	25	I	CV9	37	I	$\overline{\text{OVD}}$
2	O	OUT8	14	I	TIN3	26	I	CV8	38	I	TMOD4
3	O	OUT7	15	I	TIN2	27	I	CV7	39	I	TMOD3
4	O	OUT6	16	I	TMOD1	28	I	CV6	40	I	TMOD2
5	O	OUT5	17	O	TOUT	29	I	CV5	41	I	$\overline{\text{GH}}$
6	—	GND	18	—	GND	30	I	CV4	42	—	GND
7	O	OUT4	19	—	V_{DD}	31	—	GND	43	—	V_{DD}
8	O	OUT3	20	I	FSC8	32	I	CV3	44	I	FSC4
9	O	OUT2	21	I	$\overline{\text{CLR}}$	33	I	CV2	45	I	TMOD0
10	O	OUT1	22	I	$\overline{\text{DCSY}}$	34	I	CV1	46	I	PAL / $\overline{\text{NT}}$
11	O	OUT0	23	O	$\overline{\text{DSSY}}$	35	I	CV0	47	I	TIN1
12	O	OPARI	24	O	$\overline{\text{DRSY}}$	36	I	IPARI	48	I	TIN0



INPUT

$\overline{CLR}$	:	POWER ON RESET
CV0 - CV9	:	10-BIT COMPOSITE DATA
$\overline{DCSY}$	:	ANALOG SYNC
FSC4	:	4 fsc CLOCK
FSC8	:	8 fsc CLOCK
$\overline{GH}$	:	GH (GATED H) FROM CXD8819AQ
IPARI	:	PARITY OF INPUT DATA
$\overline{OVD}$	:	OUTPUT VD FROM CXD8819AQ
PAL / $\overline{NT}$	:	H : PAL, L : NTSC
TIN0 - TIN4	:	TEST PIN : OPEN
TMOD0 - TMOD4	:	TEST PIN : OPEN

OUTPUT

$\overline{DRSY}$	:	ANALOG DELAYED SYNC ($\overline{8\ fsc}$: 56-CLOCK)
$\overline{DSSY}$	:	ANALOG DELAYED SYNC (8 fsc : 56-CLOCK)
OPARI	:	PARITY OF OUTPUT DATA
OUT0 - OUT9	:	10-BIT COMPOSITE DATA
TOUT	:	TEST PIN

INPUT COMPOSITE VIDEO (From DIGITAL FILTER)