

**LC86P4564**

## One-time PROM built-in 8-bit Single Chip Microcontroller

### Preliminary

### Overview

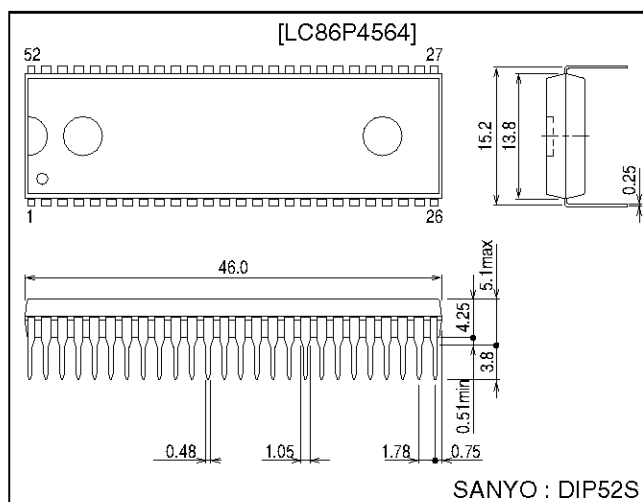
The LC86P4564 is a CMOS 8-bit single chip microcontroller with One-time PROM for the LC864500 series.

This microcontroller has the function and the pin assignment identical to those of the LC864500 series mask ROM version, and has the built-in 64K-byte PROM.

### Package Dimensions

unit : mm

#### 3128-DIP52S



### Features

- (1) Options switchable by PROM data

The option functions of the LC864500 series can be specified by the PROM data. The functions of the trial pieces can be evaluated using mass production board.

- (2) Internal PROM capacity : 65512 bytes (For program)  
8192 × 12 bits (For character)

- (3) Internal RAM capacity : 256 bytes

The LC86P4564 contains a 65512-byte PROM and a 256-byte RAM. Each size is the maximum capacity of the LC86P4564 mask-ROM series.

Mask ROM version	PROM capacity	RAM capacity
LC864532	32768 bytes	256 bytes
LC864528	28672 bytes	256 bytes
LC864524	24576 bytes	256 bytes
LC864520	20480 bytes	256 bytes
LC864516	16384 bytes	256 bytes
LC864512	12288 bytes	256 bytes
LC864508	8192 bytes	256 bytes

- (4) Operating supply voltage : 4.5 V to 5.5 V  
 (5) Instruction cycle time : 1.0 μs to 366 μs  
 (6) Operating temperature : -30°C to +70°C  
 (7) The pin and the package compatible with the LC864500 series mask ROM version  
 (8) Applicable mask ROM version : LC864532/LC864528/LC864524/LC864520/LC864516/LC864512/LC864508  
 (9) Factory shipment : DIP52S

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## LC86P4564

### Usage Notes

When using, take note of the followings.

(1) Differences between the LC86P4564 and the LC864500 series

Item	LC86P4564	LC864532/28/24/20/16/12/08
Operation after reset releasing	The option must be set internally within 3 ms after a high-level signal is applied to the reset terminal. In this period options are switched gradually, and after that, the program is executed from 00H of the program counter.	The program is executed from 00H of the program counter as soon as a high-level signal is applied to the reset terminal.
Operating supply voltage range (V <sub>DD</sub> )	4.5 V to 5.5 V	2.5 V to 6.0 V
Current drain under normal operation	Refer to 'electrical characteristics' on the semiconductor news.	

Port format of the LC86P4564 during the reset is identical to that of the LC864532/28/24/20/16/12/08.

The LC86P4564 uses 256-byte spaces addressed 0FF00H to 0FFFFH in the program memory to set options. In this way, all options of the LC864500 series cannot be executed.

Some of the LC864500 series options, which the LC86P4564 can support are as shown in the table below.

• LC86P4564 options

Option types	Pins, circuits	Contents of the option
Input/output specifications of input/output ports	Port 0	1. N-channel open-drain output 2. CMOS output *1
		1. Pull-up MOS transistor provided 2. Pull-up MOS transistor not provided *2
Pull-up MOS transistor of input port.	Port 1 *1	1. Input : Programmable pull-up MOS transistor Output : N-channel open drain 2. Input : Programmable pull-up MOS transistor Output : CMOS
	Port 7 *1	1. Pull-up MOS transistor not provided. 2. Pull-up MOS transistor provided.

\*1) Specified in bit units

\*2) When the "CMOS output" is selected as an output format, the pull-up MOS transistor will be provided, and when the "n-channel open-drain output" is selected, the pull-up MOS transistor will not be provided.

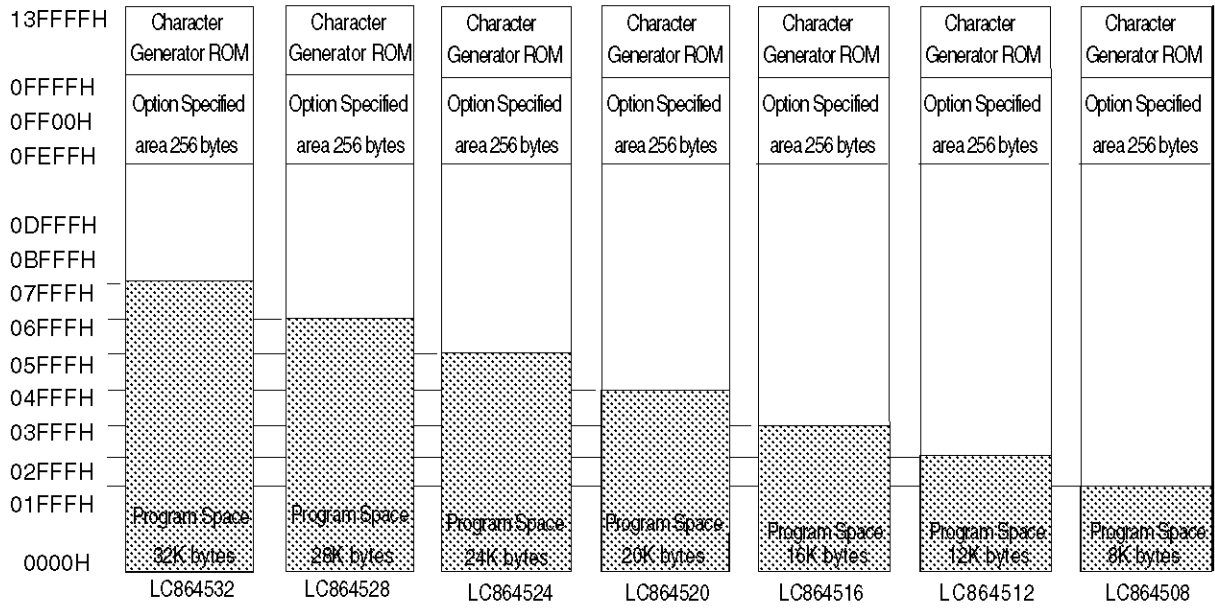
(2) Option setting program

The option data is written with the option specifying program "SU86K.EXE". The option data is linked to the program area by the linkage loader "L86K.EXE".

## LC86P4564

(3) ROM space

The LC86P4564 and LC864500 series use 256 bytes addressed on 0FF00H to 0FFFFH in the program memory as the option specified data area. The program memory capacity of the series is 65280 bytes addressed on 0000H to 0FEFFH. Note that the capacity of the LC86P4564 user-available PROM is 32768 bytes addressed on 0000H to 7FFFH, because the maximum ROM capacity of the LC864500 series ROM version is 32 K byte.



## How to Use

(1) Create a programming data for LC86P4564

Programming data for PROM of the LC86P4564 is required.

Debugged evaluation file (EVA file) must be converted to an INTEL-HEX formatted file (HEX file) with file converter program EVA2HEX.EXE. The HEX file is used as the programming data for the LC86P4564.

(2) How to program for the PROM

The LC86P4564 can be programmed by the general purpose EPROM programmer with an attachment ; W86EP4564D.

- Recommended EPROM programmers are as shown in the table below.

Manufacturer	EPROM programmer
Advantest	R4945, R4944
Andou	AF-9704
AVAL	PKW-1100, PKW-3000
Minato electronics	MODEL1890A

- The "27010 (Vp-p = 12.5 V) Intel high speed programming" mode requires to be used for writing. The storage area addressed "0 to 13FFFH" requires to be selected for address setting and the jumper (DASEC) must be set to 'OFF' at programming.

(3) How to use the data security function

"Data security" is the function to prevent the EPROM data from being read out.

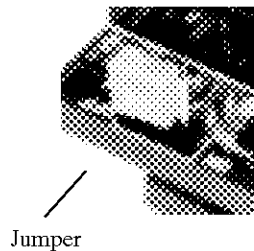
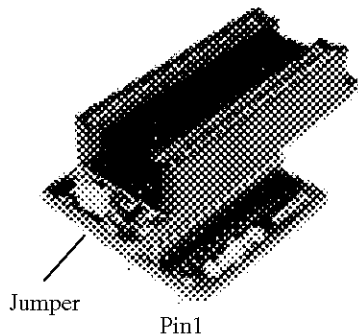
The following is the process in order to execute the data security.

1. Set the jumper of attachment 'ON'.
2. Program again. The EPROM programmer will display an error. The error indication means normal activity of the data security. It does not mean a trouble of the EPROM programmer or the LSI.

Notes

- Data security is not executed when the data of all address have 'FF' at sequence 2 above.
- Data security cannot be executed by programming the sequential operation "BLANK=>PROGRAM=>VERIFY" at sequence 2 above.
- Set the jumper 'OFF' after executing the data security.

Data security



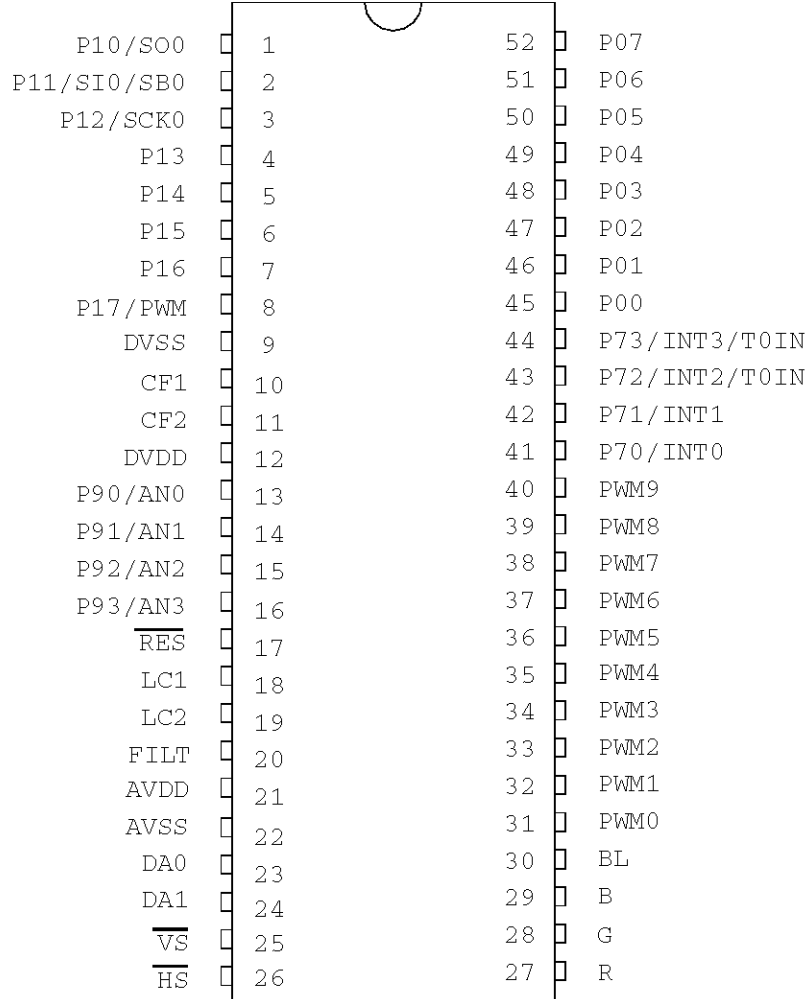
Data security OFF

W86EP4564D

# LC86P4564

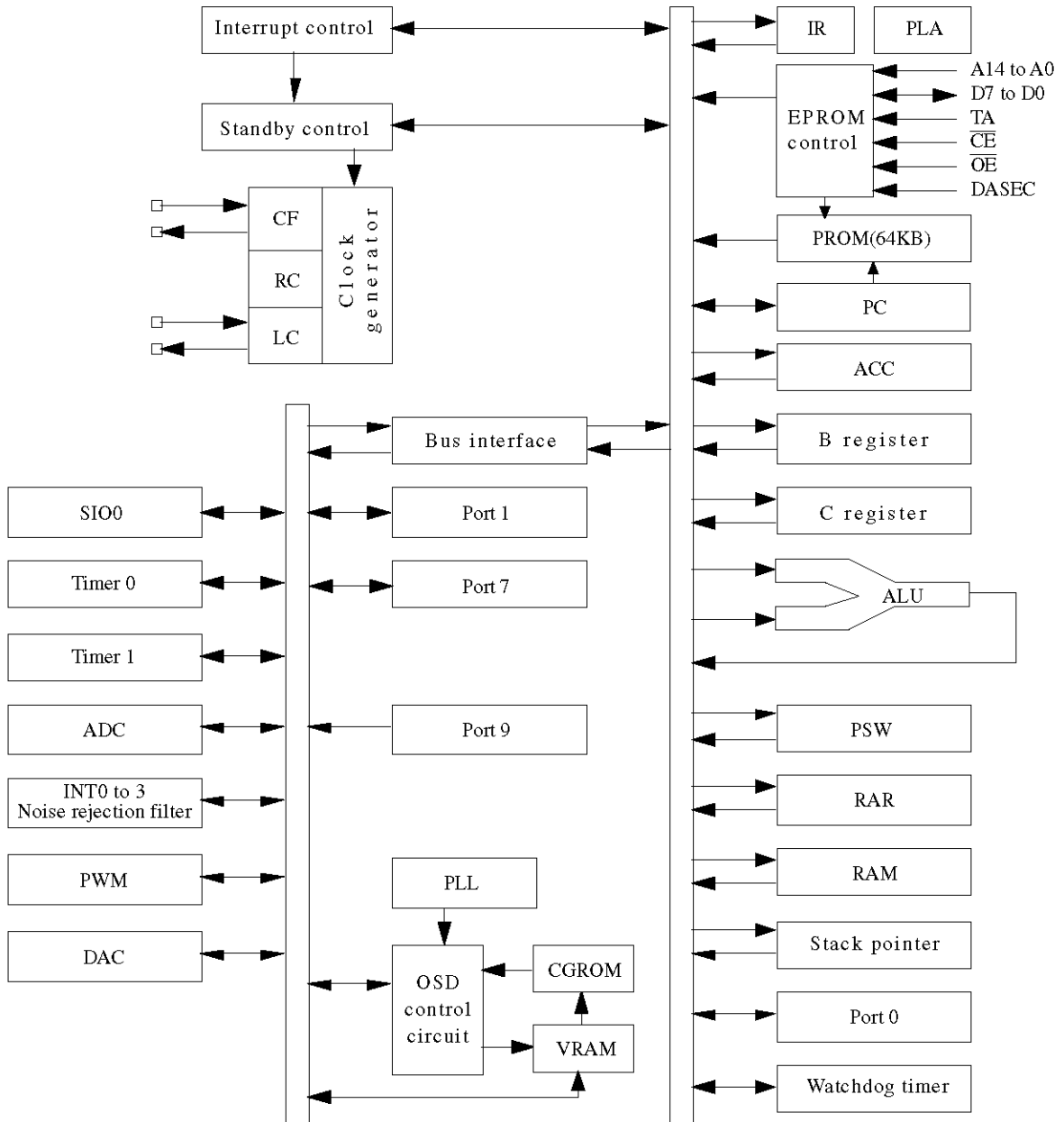
## Pin Assignment

### DIP52S



Top view

System Block Diagram



# LC86P4564

## Pin Description

Pin Description Table

Pin name	Pin No.	I/O	Function description	Option	PROM mode
DVSS	9	—	Negative power supply for digital circuit		
CF1	10	I	Input for ceramic oscillator		
CF2	11	O	Output for ceramic oscillator		
DVDD	12	—	Positive power supply for digital circuit		
$\overline{\text{RES}}$	17	I	Reset		
LC1	18	I	LC oscillation circuit input		
LC2	19	O	LC oscillation circuit output		
FILT	20	O	Filter for PLL		
AVDD	21	—	Positive power supply for analog circuit		
AVSS	22	—	Negative power supply for analog circuit		
DA0	23	I/O	DA0 output/General purpose I/O port		
DA1	24	I/O	DA1 output/General purpose I/O port		
$\overline{\text{VS}}$	25	I	Vertical synchronization signal input		
$\overline{\text{HS}}$	26	I	Horizontal synchronization signal input		
R	27	O	Red (R) output of RGB image output		A4 (*1)
G	28	O	Green (G) output of RGB image output		A5 (*1)
B	29	O	Blue (B) output of RGB image output		A6 (*1)
BL	30	O	Fast blanking control signal TV image signal or OSD image signal selecting		A7 (*1)
PWM0 to PWM9	31 to 40	O	PWM0 to PWM9 output 15V withstand		PWM 0 to PWM 8 : A8 to A16 (*1) PWM 9 : fixed to "L"
Port0 P00 to P07	45 to 52	I/O	8-bit Input/output port	Pull-up resistor provided/not provided	
			Input/output can be specified in nibble units HOLD release input Interrupt input		
Port1 P10 to P17	1 to 8	I/O	8-bit Input/output port	Output Format CMOS/Nch-OD	D0 to D7 (*2)
			Input/output can be specified in bit units.		
			Other functions		
			P10 SIO0 data output		
			P11 SIO0 data input /bus input/output		
			P12 SIO0 clock input/output		
			P17 Timer 1 (PWM) output		

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Terminal	No.	I/O	Function description	Option	PROM mode
Port7	41 P70 P71 to P73	I/O I	4-bit input port	Pull-up resistor provided/ not provided (in bit units)	P70 : VPP (*3) P71 : DASEC (*4) P72 : $\overline{OE}$ (*5) P73 : $\overline{CE}$ (*6)
			Other function		
			P70 INT0 input/HOLD release input/ n-ch transistor output for watchdog timer		
			P71 INT1 input/HOLD release input		
			P72 INT2 input/timer 0 event input		
			P73 INT3 input (noise rejection filter attached input/timer 0 event input		
	Interrupt receiver format vector address				
			Rise      Fall      Rise/Fall	H level    L level	Vector
			INT0    enable    enable    disable	enable    enable	03H
			INT1    enable    enable    disable	enable    enable	0BH
			INT2    enable    enable    enable	disable    disable	13H
			INT3    enable    enable    enable	disable    disable	1BH
Port9	13 to 16	I	4-bit input port		A0 to A3 (*1)
P90 to P93			Other function A/D converter input port (4 lines)		

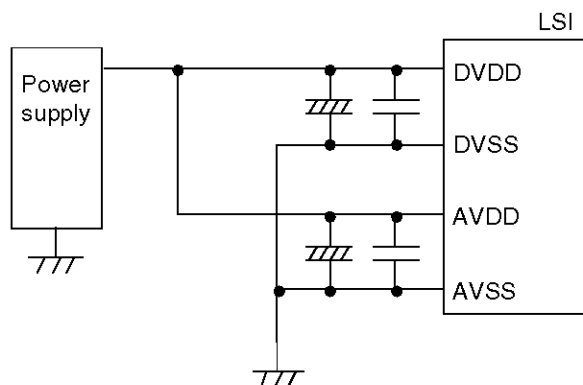
- \*1 An → Address input
- \*2 Data I/O
- \*3 Power for programming
- \*4 Memory select input/output for data security
- \*5 Output enable input
- \*6 Chip enable input

- All of port options except the pull-up resistor option of Port 0 can be specified in bit units.
- When the “CMOS output” is selected for port 0 as an output format, the pull-up resistor will be provided, and when the “n-channel open-drain output” is selected, the pull-up resistor will not be provided.
- Whichever the “CMOS” or the “n-channel open-drain” output format is selected, the programmable pull-up resistor will be provided.

- Port states during reset

Terminal	I/O	Pull-up resistor status at selecting pull-up option
Port 0	Input	Pull-up resistor OFF, ON after reset release
Port 1	Input	Programmable pull-up resistor OFF
Port 7	Input	Fixed pull-up resistor provided

- \* AVDD and AVSS are the power supply terminals for the analog operation block. DVDD and DVSS are the power supply terminals for the digital operation block. Connect as shown in the following figure to reduce the mutual noise influence.





## Specifications

### 1. Absolute Maximum Ratings at Ta = 25°C, VSS = 0 V

Parameter		Symbol	Pins	Conditions	Ratings			Unit		
					V <sub>DD</sub> [V]	min	typ		max	
Supply voltage		V <sub>DD</sub> max	DVDD, AVDD	DVDD = AVDD		-0.3		+7.0	V	
Input voltage		V <sub>I</sub> (1)	<ul style="list-style-type: none"> <li>• P71, 72, 73</li> <li>• Port 9</li> <li>• <math>\overline{RES}</math>, <math>\overline{HS}</math>, <math>\overline{VS}</math></li> </ul>			-0.3		V <sub>DD</sub> +0.3		
Output voltage		V <sub>O</sub> (1)	R, G, B, BL, FILT			-0.3		V <sub>DD</sub> +0.3		
		V <sub>O</sub> (2)	PWM0 to PWM9			-0.3		+15		
Input/output voltage		V <sub>IO</sub> (1)	Ports 0, 1, P70 DA0, 1			-0.3		V <sub>DD</sub> +0.3		
High-level output current	Peak output current	I <sub>OPH</sub> (1)	Ports 0, 1	<ul style="list-style-type: none"> <li>• Pull-up MOS transistor output</li> <li>• At each pin</li> </ul>		-2			mA	
		I <sub>OPH</sub> (2)	Ports 0, 1 DA0, 1	<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• At each pin</li> </ul>		-4				
		I <sub>OPH</sub> (3)	R, G, B, BL	<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• At each pin</li> </ul>		-5				
	Total output current	∑I <sub>OA</sub> H (1)	Port 1	The total of all pins			-10			
		∑I <sub>OA</sub> H (2)	Port 0	The total of all pins			-10			
		∑I <sub>OA</sub> H (3)	R, G, B, BL	The total of all pins			-15			
Low-level output current	Peak output current	I <sub>OPL</sub> (1)	Ports 0, 1 DA0, 1	At each pin				20		
		I <sub>OPL</sub> (2)	P70	At each pin				30		
		I <sub>OPL</sub> (3)	<ul style="list-style-type: none"> <li>• R, G, B, BL</li> <li>• PWM0 to PWM9</li> </ul>	At each pin				5		
	Total output current	∑I <sub>OAL</sub> (1)	Port 0	The total of all pins					40	
		∑I <sub>OAL</sub> (2)	Port 1, P70	The total of all pins					40	
		∑I <sub>OAL</sub> (3)	R, G, B, BL	The total of all pins					15	
		∑I <sub>OAL</sub> (4)	PWM0 to PWM9	The total of all pins					30	
Allowable power dissipation		Pd max	DIP52S	Ta = -30 to +70°C				430	mW	
Operating temperature range		Topr				-30		+70	°C	
Storage temperature range		Tstg				-55		+150		

The same level voltage must be applied to both DVSS and AVSS.  
The same level voltage must be applied to both DVDD and AVDD.

V<sub>SS</sub> = DVSS = AVSS  
V<sub>DD</sub> = DVDD = AVDD

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### 2. Allowable Operating Range at Ta = -30°C to +70°C, VSS = 0 V

Parameter	Symbol	Pins	Conditions	Ratings			Unit	
				V <sub>DD</sub> [V]	min	typ		max
Operating supply voltage range	V <sub>DD</sub>	DVDD, AVDD	0.98 μs ≤ tCYC tCYC ≤ 1.02 μs		4.5		5.5	V
Hold voltage	V <sub>HD</sub>	DVDD, AVDD	RAMs and the registers held at HOLD mode.		2.0		5.5	
High-level input voltage	V <sub>IH</sub> (1)	Port 0 (Schmitt)	Output disable	4.5 to 5.5	0.6V <sub>DD</sub>		V <sub>DD</sub>	
	V <sub>IH</sub> (2)	• Port 1 (Schmitt) • P72, 73 • HS, VS	Output disable	4.5 to 5.5	0.75V <sub>DD</sub>		V <sub>DD</sub>	
	V <sub>IH</sub> (3)	• P70 port input / interrupt • P71 • RES (Schmitt)	Output n-channel transistor OFF	4.5 to 5.5	0.75V <sub>DD</sub>		V <sub>DD</sub>	
	V <sub>IH</sub> (4)	P70 Watchdog timer input	Output n-channel transistor OFF	4.5 to 5.5	V <sub>DD</sub> -0.5		V <sub>DD</sub>	
	V <sub>IH</sub> (5)	Port 9 DA0, 1 port input		4.5 to 5.5	0.7 V <sub>DD</sub>		V <sub>DD</sub>	
Low-level input voltage	V <sub>IL</sub> (1)	Port 0 (Schmitt)	Output disable	4.5 to 5.5	V <sub>SS</sub>		0.2V <sub>DD</sub>	
	V <sub>IL</sub> (2)	• Port 1 (Schmitt) • P72, 73 • HS, VS • Port 9	Output disable	4.5 to 5.5	V <sub>SS</sub>		0.25V <sub>DD</sub>	
	V <sub>IL</sub> (3)	• P70 port input / interrupt • P71 • RES (Schmitt)	N-channel transistor OFF	4.5 to 5.5	V <sub>SS</sub>		0.25V <sub>DD</sub>	
	V <sub>IL</sub> (4)	P70 Watchdog timer input	N-channel transistor OFF	4.5 to 5.5	V <sub>SS</sub>		0.6V <sub>DD</sub>	
	V <sub>IL</sub> (5)	Port 9 DA0, 1 Port input		4.5 to 5.5	V <sub>SS</sub>		0.3V <sub>DD</sub>	
Operation cycle time	tCYC(1)		OSD function	4.5 to 5.5	0.98	1	1.02	μs
	tCYC(2)		No OSD function	4.5 to 5.5	0.98		30	

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Parameter	Symbol	Pin	Conditions	Ratings			Unit	
				V <sub>DD</sub> [V]	min	typ		max
Oscillation frequency range (Note 1)	FmCF	CF1, CF2	12 MHz (ceramic resonator oscillation) Refer to Figure 1	4.5 to 5.5	11.76	12	12.24	MHz
	FmLC	LC1, LC2	14.11 MHz (LC oscillation) Refer to Figure 2	4.5 to 5.5		14.11		
	FmRC		RC oscillation	4.5 to 5.5	0.4	0.8	2.0	
Oscillation stable time period (Note 2)	tmsCF	CF1, CF2	12 MHz (ceramic resonator oscillation) Refer to Figure 3	4.5 to 5.5		0.02	0.2	ms

(Note 1) Refer to Table 1 and Table 2 for the oscillation constant.

(Note 2) The oscillation stable time is a period necessary for the oscillation to be stable after the power first applied, the HOLD mode released and the main-clock oscillation stop instruction released.  
Refer to the Figure 3 for details.

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### 3. Electrical Characteristics at Ta = -30°C to +70°C, VSS = 0 V

Parameter	Symbol	Pins	Conditions	Ratings			Unit	
				V <sub>DD</sub> [V]	min	typ		max
Input high-level current	I <sub>IH</sub> (1)	<ul style="list-style-type: none"> <li>Port 1 DA0, 1</li> <li>Port 0 without pull-up MOS transistor</li> </ul>	<ul style="list-style-type: none"> <li>Output disable</li> <li>Pull-up MOS transistor OFF</li> <li>V<sub>IN</sub> = V<sub>DD</sub> (including the off-leakage current of the output transistor)</li> </ul>	4.5 to 5.5			1	μA
	I <sub>IH</sub> (2)	<ul style="list-style-type: none"> <li>Port 7 without pull-up MOS transistor</li> <li>Port 9</li> <li><math>\overline{\text{RES}}</math></li> <li>HS, VS</li> </ul>	V <sub>IN</sub> = V <sub>DD</sub>	4.5 to 5.5			1	
Input low-level current	I <sub>IL</sub> (1)	<ul style="list-style-type: none"> <li>Port 1 DA0, 1</li> <li>Port 0 without pull-up MOS transistor</li> </ul>	<ul style="list-style-type: none"> <li>Output disable</li> <li>Pull-up MOS transistor OFF</li> <li>V<sub>IN</sub> = V<sub>SS</sub> (including the off-leakage current of the output transistor)</li> </ul>	4.5 to 5.5	-1			
	I <sub>IL</sub> (2)	<ul style="list-style-type: none"> <li>Port 7 without pull-up MOS transistor</li> <li>Port 9</li> </ul>	V <sub>IN</sub> = V <sub>SS</sub>	4.5 to 5.5	-1			
	I <sub>IL</sub> (3)	<ul style="list-style-type: none"> <li><math>\overline{\text{RES}}</math></li> <li>HS, VS</li> </ul>	V <sub>IN</sub> = V <sub>SS</sub>	4.5 to 5.5	-1			
Output high-level voltage	V <sub>OH</sub> (1)	CMOS output of ports 0, 1 DA0, 1	I <sub>OH</sub> = -1.0 mA	4.5 to 5.5	V <sub>DD</sub> -1			V
	V <sub>OH</sub> (2)	R, G, B, BL	I <sub>OH</sub> = -0.1 mA	4.5 to 5.5	V <sub>DD</sub> -0.5			
Output low-level voltage	V <sub>OL</sub> (1)	Ports 0, 1	I <sub>OL</sub> = 10 mA	4.5 to 5.5			1.5	
	V <sub>OL</sub> (2)	Ports 0, 1 DA0, 1	<ul style="list-style-type: none"> <li>I<sub>OL</sub> = 1.6 mA</li> <li>The total current of the ports 0, 1 is not over 40 mA.</li> </ul>	4.5 to 5.5			0.4	
	V <sub>OL</sub> (3)	<ul style="list-style-type: none"> <li>R, G, B, BL</li> <li>PWM0 to PWM9</li> </ul>	<ul style="list-style-type: none"> <li>I<sub>OL</sub> = 3.0 mA</li> <li>The current of any pin is 3 mA or less.</li> </ul>	4.5 to 5.5			0.4	
	V <sub>OL</sub> (4)	P70	I <sub>OL</sub> = 1 mA	4.5 to 5.5			0.4	
Pull-up MOS transistor resistance	R <sub>pu</sub>	<ul style="list-style-type: none"> <li>Ports 0, 1</li> <li>Port 7</li> </ul>	V <sub>OH</sub> = 0.9 V <sub>DD</sub>	4.5 to 5.5	13	38	80	kΩ
Output off-leakage current	I <sub>OFF</sub>	PWM0 to PWM9	V <sub>OUT</sub> = 13.5 V	4.5 to 5.5			5	μA
Hysteresis voltage	V <sub>HIS</sub>	<ul style="list-style-type: none"> <li>Ports 0, 1</li> <li>Port 7</li> <li><math>\overline{\text{RES}}</math></li> <li>HS, VS</li> </ul>	Output disable	4.5 to 5.5		0.1V <sub>DD</sub>		V

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Parameter	Symbol	Pins	Conditions	Ratings			Unit	
				V <sub>DD</sub> [V]	min	typ		max
Pin capacitance	CP	All pins	<ul style="list-style-type: none"> <li>• f = 1 MHz</li> <li>• Unmeasured input pins are set to V<sub>SS</sub> level.</li> <li>• Ta = 25°C</li> </ul>	4.5 to 5.5		10		pF

### 4. Serial Input/Output Characteristics at Ta = -30°C to +70°C , V<sub>SS</sub> = 0 V

Parameter	Symbol	Pins	Conditions	Ratings			Unit					
				V <sub>DD</sub> [V]	min	typ		max				
Serial clock	Input clock	Cycle	tCKCY(1)	<ul style="list-style-type: none"> <li>• SCK0</li> <li>• SCLK0</li> </ul>	Refer to Figure 5	4.5 to 5.5	2			tCYC		
		Low-level pulse width	tCKL(1)					4.5 to 5.5	1			
		High-level pulse width	tCKH(1)					4.5 to 5.5	1			
	Output clock	Cycle	tCKCY(2)	<ul style="list-style-type: none"> <li>• SCK0</li> <li>• SCLK0</li> </ul>	<ul style="list-style-type: none"> <li>• Use a pull-up resistor (1 kΩ) when open-drain output</li> <li>• Refer to Figure 5</li> </ul>	4.5 to 5.5	2					
		Low-level pulse width	tCKL(2)					4.5 to 5.5			1/2tCKCY	
		High-level pulse width	tCKH(2)					4.5 to 5.5			1/2tCKCY	
Serial input	Data set-up time	tICK	SI0	<ul style="list-style-type: none"> <li>• Synchronized with the rising edge of SCK0.</li> <li>• Refer to Figure 5</li> </ul>	4.5 to 5.5	0.1			μs			
	Data hold time	tCKI					4.5 to 5.5	0.1				
Serial output	Output delay time (External serial clock)	tCKO(1)	SO0	<ul style="list-style-type: none"> <li>• Use a pull-up resistor (1kΩ) when open-drain output.</li> <li>• Synchronized with the falling edge of SCK0.</li> <li>• Refer to Figure 5</li> </ul>	4.5 to 5.5				μs			
	Output delay time (Internal serial clock)	tCKO(2)					4.5 to 5.5				7/12tCYC +0.2	

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### 5. Pulse Input Conditions at $T_a = -30^{\circ}\text{C}$ to $+70^{\circ}\text{C}$ , $V_{SS} = 0\text{ V}$

Parameter	Symbol	Pins	Conditions	Ratings			Unit	
				$V_{DD}$ [V]	min	typ		max
High/low level pulse width	tPIH(1) tPIL(1)	• INT0, INT1 • INT2/T0IN	• Interrupt factor flag settable. • Timer and counter 0 pulse-countable.	4.5 to 5.5	1		tCYC	
	tPIH(2) tPIL(2)	INT3/T0IN (The noise rejection filter time constant is 1/1)	• Interrupt factor flag settable. • Timer and counter 0 pulse-countable.	4.5 to 5.5	2			
	tPIH(3) tPIL(3)	INT3/T0IN (The noise rejection filter time constant is 1/16)	• Interrupt factor flag settable. • Timer and counter 0 pulse-countable.	4.5 to 5.5	32			
	tPIL(4)	$\overline{\text{RES}}$	Reset acceptable	4.5 to 5.5	200		$\mu\text{s}$	
	tPIH(5) tPIL(5)	$\overline{\text{HS}}$ , $\overline{\text{VS}}$	Display position can be controlled Each active edge of $\overline{\text{HS}}$ , $\overline{\text{VS}}$ must be set apart more than 1tCYC. Refer to Figure 7	4.5 to 5.5	10		tCYC	
Rise/fall time	tTHL tTLH	$\overline{\text{HS}}$	Refer to Figure 7	4.5 to 5.5		500	ns	
Horizontal pull-in range	FH	$\overline{\text{HS}}$	The monitor point in Figure 10 is $1/2 V_{DD}$ .	4.5 to 5.5	15.23	15.73	16.23	kHz

### 6. A/D Converter Characteristics at $T_a = -30^{\circ}\text{C}$ to $+70^{\circ}\text{C}$ , $V_{SS} = 0\text{ V}$

Parameter	Symbol	Pins	Conditions	Ratings			Unit	
				$V_{DD}$ [V]	min	typ		max
Resolution	N			4.5 to 5.5		4	bit	
Absolute precision	ET	(Note 3)		4.5 to 5.5		$\pm 1/4$	$\pm 1/2$	LSB
Conversion time	tCAD	After the $V_{ref}$ selected till the conversion completed.	1 bit conversion time = 2tCYC	4.5 to 5.5			1.96	$\mu\text{s}$
Reference current	$I_{REF}$		(Regulate the ladder resistor)	4.5 to 5.5		1.0	2.0	mA
Analog input voltage range	$V_{AIN}$	AN0 to AN3		4.5 to 5.5	$V_{SS}$		$V_{DD}$	V
Analog port input current	$I_{AINH}$		$V_{AIN} = V_{DD}$	4.5 to 5.5			1	$\mu\text{A}$
	$I_{AINL}$		$V_{AIN} = V_{SS}$	4.5 to 5.5	-1			

Note 3: Absolute precision excepts quantizing error ( $\pm 1/2\text{LSB}$ ).

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### 7. D/A Converter Characteristics at Ta = -30°C to +70°C, V<sub>SS</sub> = 0 V

Parameter	Symbol	Pins	Conditions	Ratings			Unit
				V <sub>DD</sub> [V]	min	typ	
Resolution	NDA			4.5 to 5.5		7	bit
Absolute precision	ETDA		7 bits mode (Note 4)	4.5 to 5.5		±2.0	LSB
Settling time	tSDA		(Note 5)	4.5 to 5.5		1.0	μs
Analog input voltage range	V <sub>AOUT</sub>	DA0 to DA1		4.5 to 5.5	V <sub>SS</sub>		V <sub>DD</sub> V
Output resistor	RODA		(Note 6)	4.5 to 5.5		8	kΩ

Note 4 : The ±1/2-LSB quantization error is not included. (No load.)

Note 5 : Settling time refers to the time from when the D/A conversion instruction is executed to when the analog voltage output corresponding to the digital voltage on the specific port is generated.

Note 6 : D/A data = 80H

### 8. Current Drain Characteristics at Ta = -30°C to +20°C, V<sub>SS</sub> = 0 V

Parameter	Symbol	Pins	Conditions	Ratings			Unit	
				V <sub>DD</sub> [V]	min	typ		max
Current drain during basic operation (Note 7)	I <sub>DDOP</sub> (1)	DVDD, AVDD	<ul style="list-style-type: none"> <li>• FmCF = 12 MHz when ceramic oscillation</li> <li>• FmLC = 14.11MHz when LC oscillation</li> <li>• System clock : 12 MHz</li> <li>• Internal RC when oscillation stops</li> </ul>	4.5 to 5.5		21	32	mA
Current drain in HALT mode (Note 7)	I <sub>DDHALT</sub> (1)	DVDD, AVDD	<ul style="list-style-type: none"> <li>• HALT mode</li> <li>• FmCF = 12 MHz when ceramic oscillation</li> <li>• FmLC = 0 Hz (when oscillation stops)</li> <li>• System clock : 12 MHz</li> <li>• Internal RC when oscillation stops.</li> </ul>	4.5 to 5.5		5	10	mA
	I <sub>DDHALT</sub> (2)	DVDD, AVDD	<ul style="list-style-type: none"> <li>• HALT mode</li> <li>• FmCF = 0 MHz (when oscillation stops)</li> <li>• FmLC = 0 Hz (when oscillation stops)</li> <li>• System clock : Internal RC</li> </ul>	4.5 to 5.5		400	800	μA
Current drain in HOLD mode (Note 7)	I <sub>DDHOLD</sub> (1)	DVDD, AVDD	<ul style="list-style-type: none"> <li>• HOLD mode</li> <li>• All oscillation stops.</li> </ul>	4.5 to 5.5		0.05	20	μA
	I <sub>DDHOLD</sub> (2)							

Note 7 : The current into the output transistors and the pull-up MOS transistors are ignored.

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Oscillation type	Manufacturer	Oscillator	C1	C2
12 MHz ceramic resonator oscillation	Murata	CSA12.0MTZ	33 pF	33 pF
		CST12.0MTW	on chip	
	Kyocera	KBR-12.0M	47 pF	47 pF

\* Both C1 and C2 must use an K rank ( $\pm 10\%$ ) and an SL characteristics.

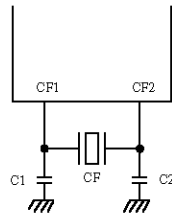
**Table 1 Ceramic Resonator Oscillation Guaranteed Constant (main-clock)**

Oscillation type	L	C3	C4
14.11 MHz LC oscillation	4.7 $\mu\text{H}$	33 pF	45 pF (Trimmer)
	4.7 $\mu\text{H} \pm 10\%$ (Variable)	33 pF	33 pF

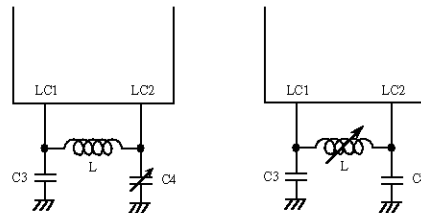
\* See Figures 11 and 12.

**Table 2 LC Oscillation Guaranteed Constant (OSD clock)**

- (Notes)
- Since the circuit pattern affects the oscillation frequency, place the oscillation-related parts as close to the oscillation pins as possible with the shortest possible pattern length.
  - If you use other oscillators herein, we provide no guarantee for the characteristics.
  - Adjust the voltage of monitor point in Figure 10 to  $1/2V_{\text{DD}} \pm 10\%$  by the LC oscillation constant 'L' or 'C' to lock the PLL circuit.



**Figure 1 Ceramic Oscillation**



**Figure 2 LC Oscillation**



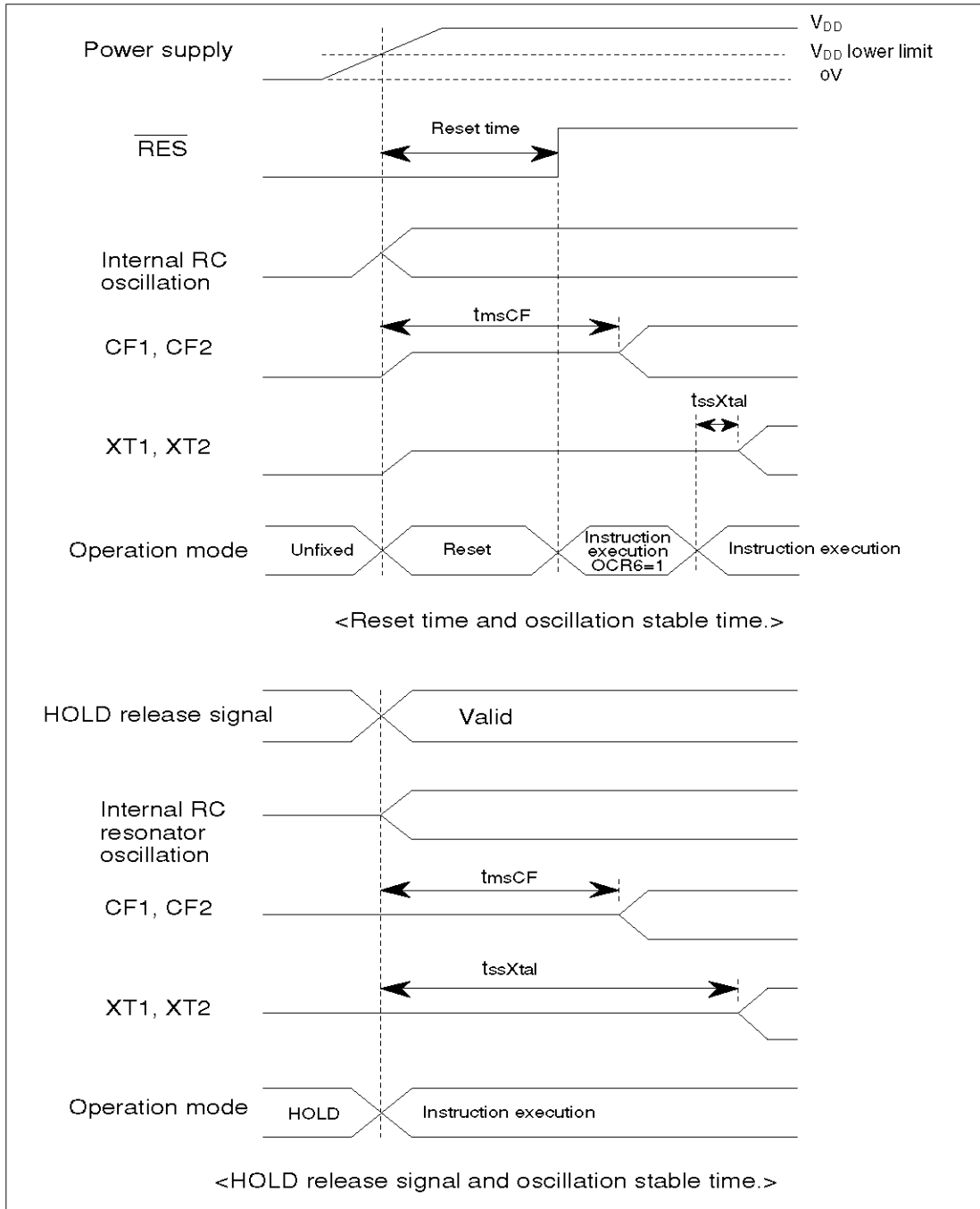


Figure 3 Oscillation Stable Time

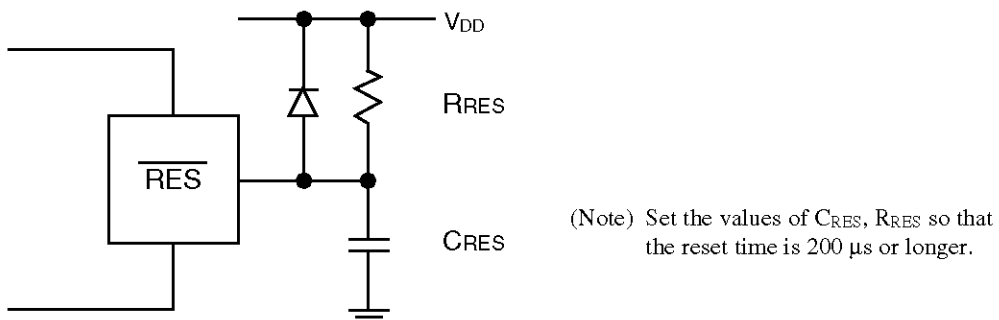
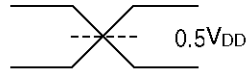


Figure 4 Reset Circuit

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< AC timing point >

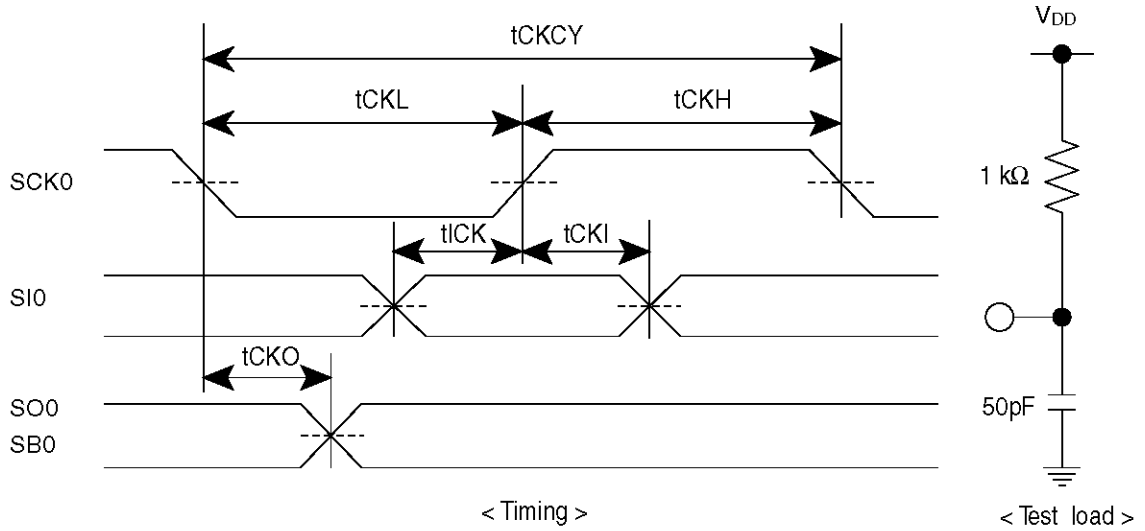


Figure 5 Serial Input/output Test Condition

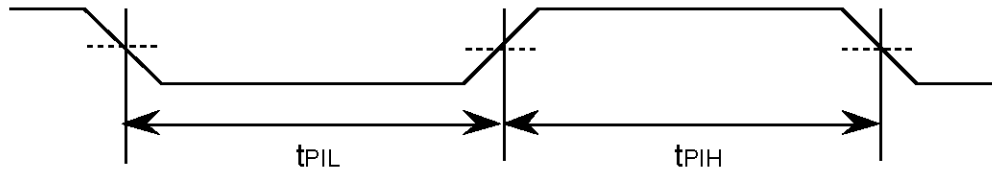


Figure 6 Pulse Input Timing Condition - 1

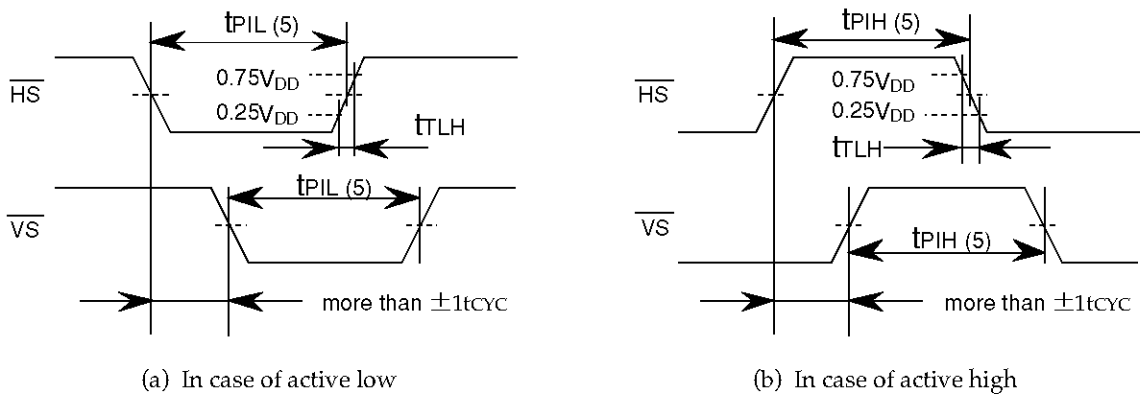


Figure 7 Pulse Input Timing Condition - 2

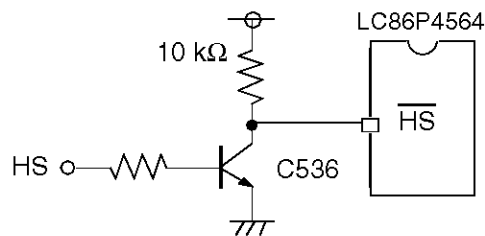


Figure 8 Recommended Interface Circuit

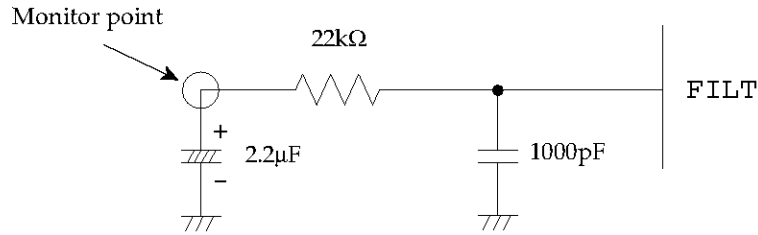


Figure 10 FILT Recommended Circuit

(Note) • Place the parts connected FILT terminal as close to the FILT as possible with the shortest pattern length on the board.

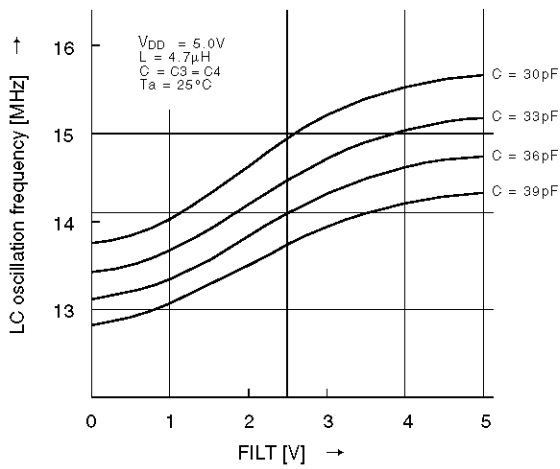


Figure 11 FILT-LC Oscillation Frequency(1)

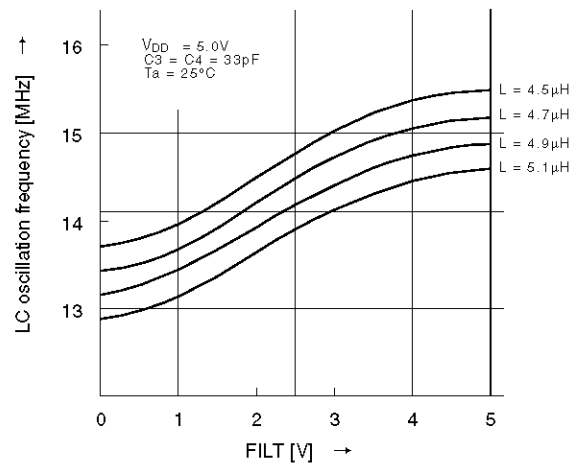


Figure 12 FILT-LC Oscillation Frequency(2)

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