MN35502

D/A Converter for Digital Audio Equipment

■ Overview

The MN35502 is a CMOS digital-to-analog converter designed especially for PCM digital audio equipment. It features a built-in digital filter with 16/20-bit input.

It uses pulse edge modulation (PEM) and JVC advanced noise shaping (VANS) to yield the high resolution and low distortion ratio equivalent to those of 20-bit systems covering the range between 0 and 20 kHz.

The chip incorporates an 8-fold oversampling digital filter that eliminates a low-pass filter after the D/A converter and thus greatly reduces the power consumption of the overall D/A conversion system.

Use of single-channel 4PEM output yields a D/A converter with a low distortion ratio and high signal-to-noise ratio.

The chip makes a major contribution to reducing the cost and size of CD players and other digital audio equipment.

■ Features

- Built-in 20-bit, 8-fold oversampling digital filter
  - 2-fold oversampling digital filters with 3-stage cascade configuration

    Bandwidth ripple: within ±0.0042 dB for 0 to 0.454 f_s

    Cutoff band attenuation

    1±0.454 f_s: min. 94.8dB

    2±0.454 f_s: min. 77.4dB

    4±0.454 f_s: min. 66.8dB

    Transition bandwidth

    0.469 f_s: – 0.12dB

    0.531 f_s: –38dB
  - Digital filter output: 24 bits

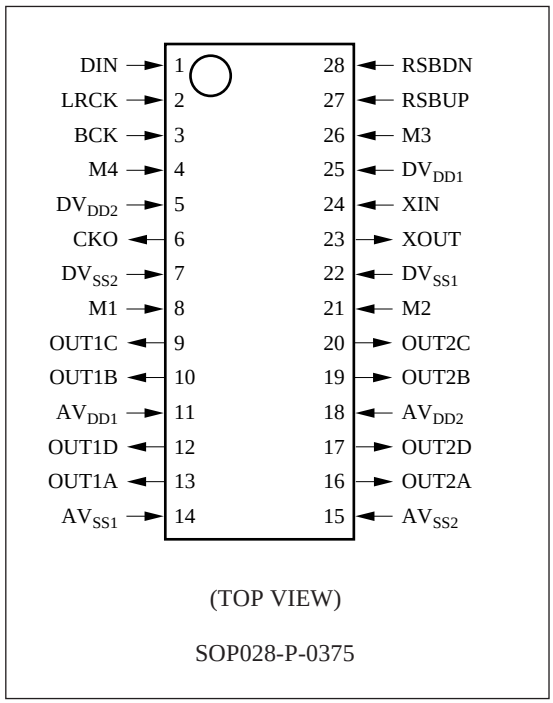
    (Output after data compression with primary noise shaper)
- Built-in digital de-emphasis

  f_S=44.1 kHz 0 to 18kHz max. deviation ±0.055dB

  18 to 20kHz max. deviation 0.115dB
- Built-in digital attenuation

  Up/down over 32 steps
- Support for double-speed operation (192 f_s clock)

■ Pin Assignment



(TOP VIEW)

SOP028-P-0375

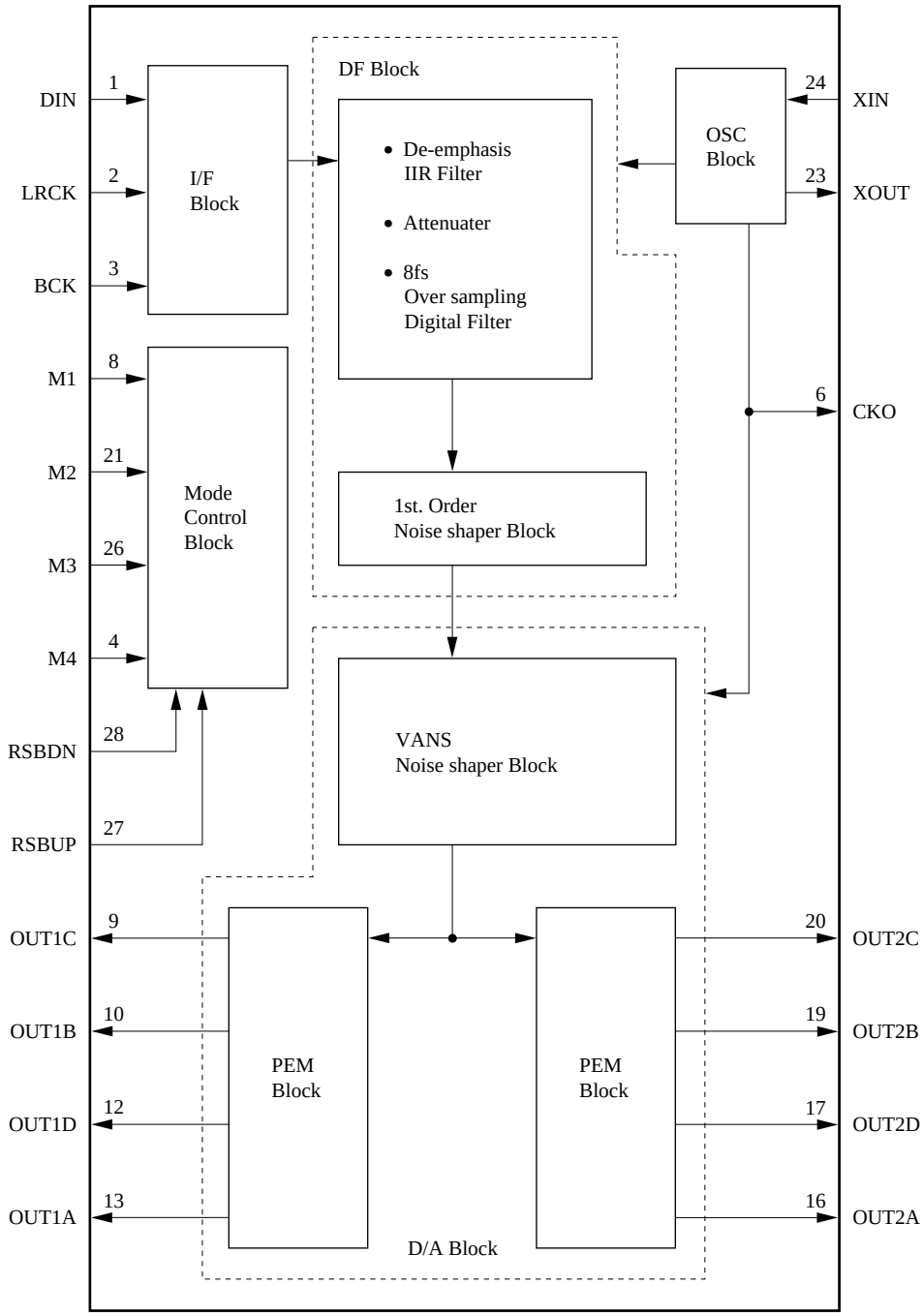
- 8PEM output configuration (4PEM output per channel)
- Support for low-voltage (3.3-volt) operation
- Choice of system clocks:

  192 f_s, 256 f_s, 384 f_s, 512 f_s, 576 f_s
- Choice of input data formats: left-packed, right-packed, I^2S bus (16 or 20 bits, alternating channel input, MSB first)

■ Applications

- CD players and other digital audio equipment

■ Block Diagram



■ Pin Descriptions

Pin No.	Pin Name	Function Description
1	DIN	Serial data pin (MSB first)
2	LRCK	LR synchronization signal input pin (f_s rate)
3	BCK	Data shift bit clock input pin
4	M4	Operating mode selection pin 4 (See Table 1.)
5	DV_{DD2}	Power supply pin 2 for digital circuits
6	CKO	Clock output pin
7	DV_{SS2}	Ground pin for digital circuits
8	M1	Operating mode selection pin 1, with pull-up resistor (See Table 1.)
9	OUT1C	PEM output pin 1C (Left channel with reversed phase)
10	OUT1B	PEM output pin 1B (Left channel with same phase)
11	AV_{DD1}	Power supply pin 1 for analog circuits
12	OUT1D	PEM output pin 1D (Left channel with reversed phase)
13	OUT1A	PEM output pin 1A (Left channel with same phase)
14	AV_{SS1}	Ground pin 1 for analog circuits
15	AV_{SS2}	Ground pin 2 for analog circuits
16	OUT2A	PEM output pin 2A (Right channel with same phase)
17	OUT2D	PEM output pin 2D (Right channel with reversed phase)
18	AV_{DD2}	Power supply pin 2 for analog circuits
19	OUT2B	PEM output pin 2B (Right channel with same phase)
20	OUT2C	PEM output pin 2C (Right channel with reversed phase)
21	M2	Operating mode selection pin 2, with pull-up resistor (See Table 1.)
22	DV_{SS1}	Ground pin 1 for digital circuits (Ground for oscillator circuit)
23	XOUT	Crystal oscillator pin
24	XIN	Crystal oscillator pin (external clock input pin) (Built-in feedback resistor)
25	DV_{DD1}	Power supply pin 1 for digital circuits
26	M3	Operating mode selection pin 3, with pull-up resistor (See Table 1.)
27	RSBUP	Reset pin/digital attenuation control pin (See Table 2.)
28	RSBDN	Reset pin/digital attenuation control pin (See Table 2.)

■ Operating Mode Descriptions

Table 1. MN35502 Operating Modes

Mode Selection Pins	Pin States and Operating Modes																	
M1	L										H							
M2	L				H						H				H			
M3	L		H		L		H				L		H		L		H	
M4	L	H	L	H	L	H	L		H		L	H	L	H	L	H	L	H
RSBUP	——						L	H	L	H	——							
Mode	0	1	2	3	4	5	60	61	70	71	8	9	A	B	C	D	E	F
Input data format	Right-packed									Test Mode	Right-packed	Left-packed	Right-packed	Left-packed	Right-packed	I^2S	Right-packed	I^2S
Input word length (bit)	16				20		16	20	16		16	20	16	20	16	20	16	20
Data when LRCK=H	Left channel										R	L	R	L	L	R	L	R
XIN clock frequency (f_s)	384		192		384		512				384		576		256		384	
CKO output frequency (f_s)	384		192		384		512				32	64	32	64				
Digital attenuation	Available						Not available				Available							
De-emphasis (f_s=44.1kHz)	—	O	—	O	—	O	—	—	O		——							
VANS oversampling (f_s)	64		32		64						64		96		64		96	
Theoretical signal-to-noise ratio (dB)	134		107		134		128				134		150		128		144	
Output level	$0.666 \times AV_{DD}$						$0.4995 \times AV_{DD}$				$0.666 \times AV_{DD}$				$0.4995 \times AV_{DD}$			

Notes

1: Modes 2 and 3 support f_s clock speeds up to 88.2 kHz.

2: Modes A, B, E, and F support f_s clock speeds up to 32 kHz; the others, up to 48 kHz.

■ Functional Descriptions

- Digital attenuation and reset

Table 2 shows how the inputs from the two pins RSBUP and RSBDN control digital attenuation.

Table 2. Attenuation Modes

Pin Name	Pin States and Operating Modes				
RSBUP	L	↑↓	L	↑	H
RSBDN	L	L	↑	H	↑
Mode	Reset	Mute	Normal	Attenuation control	
Volume	Mute (–∞)		0dB	UP	DOWN

Notes

1: The upward arrow indicates the rising edge change of the input signal; the paired arrows, the rising and falling edge changes.

2: Always reset the chip after applying the power, restarting the clock, or changing the clock speed. (Wait for the crystal oscillation to stabilize and then apply a reset signal at least eight LRCK clock cycles long.)

3: Digital attenuation is not available for modes with a master clock of 512 f_s (modes 60 to 70).

There are a total of 32 attenuation levels.

According to the attenuation control shown in Table-2, volume goes up or down in one step every input-signal rising-edge. Still, in the 0 dB state, up-pulse does not change the volume. Similary, in the muting state (–∞), down-pulse does not change the volume.

The change of the input signals is detected by inner clock of 32 f_s period, so always use a frequency of 16 f_s or less for changes in the RSBUP and RSBDN signals.

Do not simultaneously change the RSBUP and RSBDN signals unless setting up for a reset.

■ Conversion Characteristics

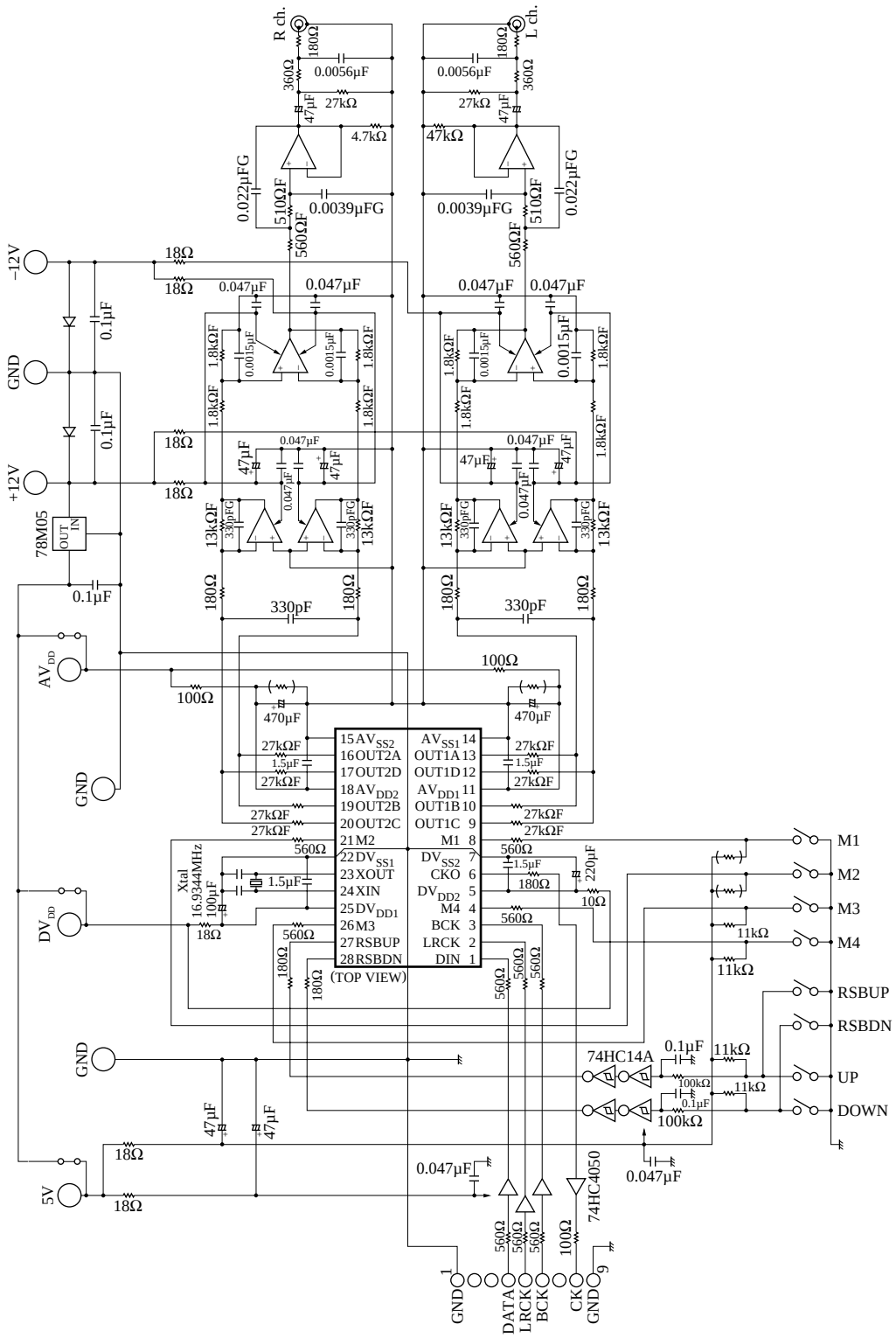
DV_{DD}=5.0V, DV_{SS}=0V, AV_{DD}=5.0V, AV_{SS}, f=16.9344MHz, Ta=25˚C

Analog Characteristics for 20-bit, 1 f_s input

Parameter	Symbol	Test Condition	min	typ	max	Unit
Signal-to-noise ratio	SN	EIAJ (kHz)		114		dB
Dynamic range	D.R.	EIAJ (kHz)		113		dB
Total harmonic distortion	THD+N	EIAJ (kHz)		0.0006	0.0010	%
Output level		1kHz F.S.		2.1		V_{rms}

The above analog characteristics are based on measurements with the sample application circuit using mode 4.

■ Application Circuit Example



■ Package Dimensions (Unit: mm)

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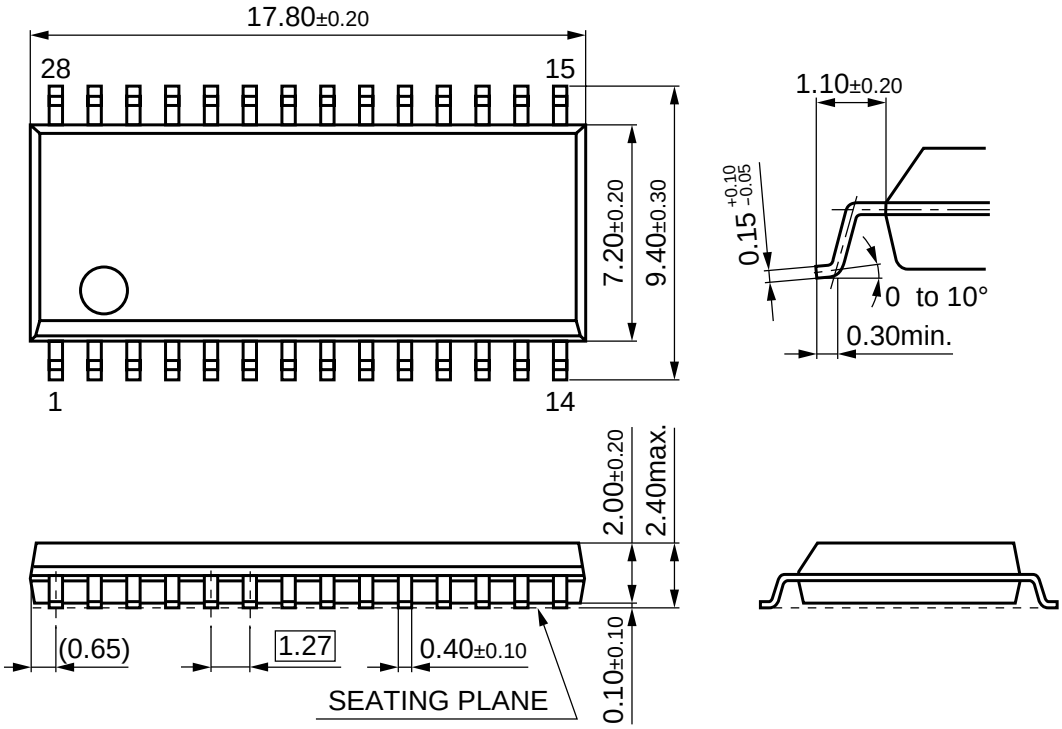

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