

4-bit cascadable shift register (3-State)

74F395

FEATURES

- 4-bit parallel load shift register
- Independent 3-State buffer outputs, Q0–Q3
- Separate Qs output for serial expansion
- Asynchronous Master Reset

DESCRIPTION

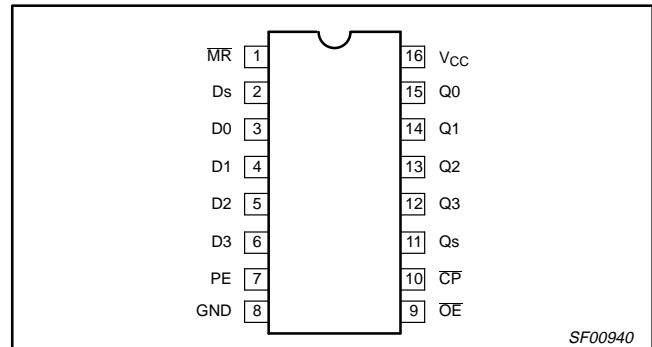
The 74F395 is a 4-bit Shift Register with serial and parallel synchronous operating modes and 3-State buffer outputs. The shifting and loading operations are controlled by the state of the Parallel Enable (PE) input. When PE is High, data is loaded from the Parallel Data inputs (D0–D3) into the register synchronous with the High-to-Low transition of the Clock input (CP). When PE is Low, the data at the Serial Data input (Ds) is loaded into the Q0 flip-flop, and the data in the register is shifted one bit to the right in the direction (Q0→Q1→Q2→Q3) synchronous with the negative clock transition. The PE and Data inputs are fully edge-triggered and must be stable one setup prior to the High-to-Low transition of the clock.

The Master Reset (\overline{MR}) is an asynchronous active-Low input. When Low, the \overline{MR} overrides the clock and all other inputs and clears the register.

The 3-state output buffers are designed to drive heavily loaded 3-State buses, or large capacitive loads.

The active-Low Output Enable (\overline{OE}) controls all four 3-State buffers independent of the register operation. The data in the register appears at the outputs when \overline{OE} is Low. The outputs are in High impedance "OFF" state, which means they will neither drive nor load the bus when \overline{OE} is High. The output from the last stage is brought out separately. This output (Qs) is tied to the Serial Data input (Ds) of the next register for serial expansion applications. The Qs output is not affected by the 3-State buffer operation.

PIN CONFIGURATION



TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F395	120MHz	32mA

ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE
	$V_{CC} = 5V \pm 10\%$, $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$
16-pin plastic DIP	N74F395N
16-pin plastic SO	N74F395D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 – D3	Data inputs	1.0/1.0	20 μ A/0.6mA
Ds	Serial data input	1.0/1.0	20 μ A/0.6mA
PE	Parallel Enable input	1.0/1.0	20 μ A/0.6mA
\overline{MR}	Master Reset input (active Low)	1.0/1.0	20 μ A/0.6mA
\overline{OE}	Output Enable input (active Low)	1.0/1.0	20 μ A/0.6mA
CP	Clock Pulse input (active falling edge)	1.0/1.0	20 μ A/0.6mA
Qs	Serial expansion output	50/33	1.0mA/20mA
Q0–Q3	Data outputs (3-State)	150/40	3.0mA/24mA

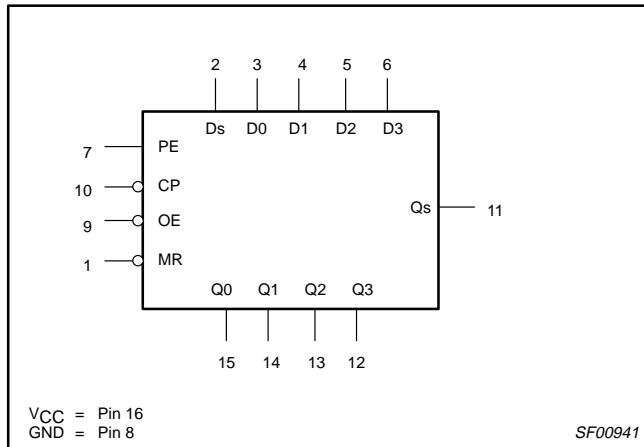
NOTE:

One (1.0) FAST unit load is defined as: 20 μ A in the High state and 0.6mA in the Low state.

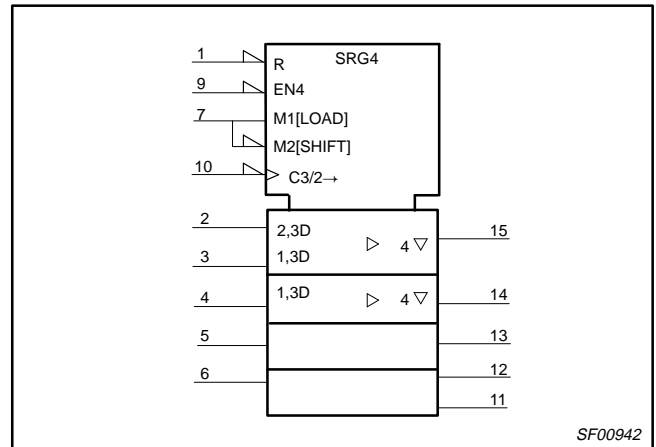
4-bit cascadable shift register (3-State)

74F395

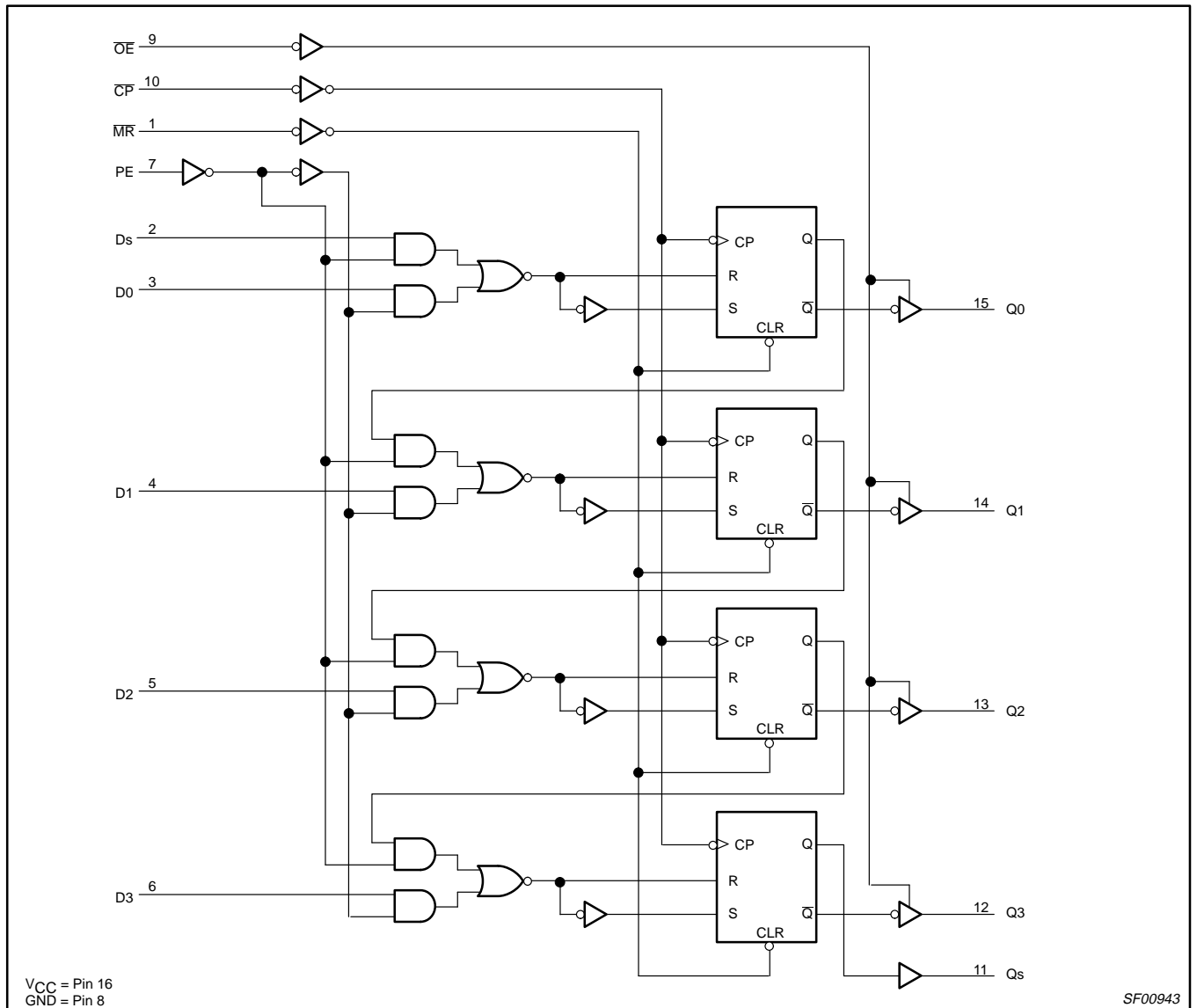
LOGIC SYMBOL



IEC/IEEE SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



4-bit cascadable shift register (3-State)

74F395

MODE SELECT–FUNCTION TABLE

INPUTS					OUTPUTS				REGISTER OPERATING MODES
MR	CP	PE	Ds	Dn	Q0	Q1	Q2	Q3	
L	X	X	X	X	L	L	L	L	Reset (clear)
H		l	l	X	L	q0	q1	q2	Shift right
H		l	h	X	H	q0	q1	q2	
H		h	X	l	L	L	L	L	Parallel load
H		h	X	h	H	H	H	H	

- H = High voltage level
- h = High voltage level one set-up time prior to the High-to-Low clock transition
- L = Low voltage level
- l = Low voltage level one set-up time prior to the High-to-Low clock transition
- qn = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the High-to-Low clock transition
- X = Don't care
- Z = High impedance "OFF" state
- = High-to-Low clock transition

INPUTS		OUTPUTS		3-STATE BUFFER OPERATING MODES
OE	Qn (Register)	Q0, Q1, Q2, Q3	Qs	
L	L	L	L	Read
L	H	H	H	
H	L	Z	L	Disable buffers
H	H	Z	H	

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V _{CC}	Supply voltage	-0.5 to +7.0	V
V _{IN}	Input voltage	-0.5 to +7.0	V
I _{IN}	Input current	-30 to +5	mA
V _{OUT}	Voltage applied to output in High output state	-0.5 to +5.5	V
I _{OUT}	Current applied to output in Low output state	Qs	40
		Q0–Q3	48
T _{amb}	Operating free-air temperature range	0 to +70	°C
T _{stg}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5.0	5.5	V
V _{IH}	High-level input voltage	2.0			V
V _{IL}	Low-level input voltage			0.8	V
I _{IK}	Input clamp current			-18	mA
I _{OH}	High-level output current	Qs		-1	mA
		Q0–Q3		-3	mA
I _{OL}	Low-level output current	Qs		20	mA
		Q0–Q3		24	mA
T _{amb}	Operating free-air temperature range	0		70	°C

4-bit cascadable shift register (3-State)

74F395

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS ¹			LIMITS			UNIT
						MIN	TYP ²	MAX	
V _{OH}	High-level output voltage	Q _s	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN	I _{OH} = -1mA	±10%V _{CC}	2.5			V
					±5%V _{CC}	2.7	3.4		V
		Q0-Q3		I _{OH} = -3mA	±10%V _{CC}	2.4			V
					±5%V _{CC}	2.7			V
V _{OL}	Low-level output voltage		V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN	I _{OL} = MAX	±10%V _{CC}		0.35	0.50	V
					±5%V _{CC}		0.35	0.50	V
V _{IK}	Input clamp voltage		V _{CC} = MIN, I _I = I _{IK}				-0.73	-1.2	V
I _I	Input current at maximum input voltage		V _{CC} = MAX, V _I = 7.0V					100	μA
I _{IH}	High-level input current		V _{CC} = MAX, V _I = 2.7V					20	μA
I _{IL}	Low-level input current		V _{CC} = MAX, V _I = 0.5V					-0.6	mA
I _{ozH}	Off-state output current High level of voltage applied	Q0-Q3 only	V _{CC} = MAX, V _O = 2.7V					50	μA
I _{ozL}	Off-state output current Low level of voltage applied	Q0-Q3 only	V _{CC} = MAX, V _O = 0.5V					-50	μA
I _{OS}	Short-circuit output current ³		V _{CC} = MAX				-60	-150	mA
I _{CC}	Supply current (total)	I _{CCH}	V _{CC} = MAX	MR=PE=Dn=Ds=4.5V, OE=GND, CP=			33	48	mA
		I _{CCL}		MR=OE=Dn=Ds=GND, PE=4.5V, CP=			35	50	mA
		I _{CCZ}		MR=Dn=Ds=GND, OE=4.5V			32	46	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
- Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

4-bit cascadable shift register (3-State)

74F395

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$V_{CC} = +5V$ $T_{amb} = +25^{\circ}C$ $C_L = 50pF, R_L = 500\Omega$			$V_{CC} = +5V \pm 10\%$ $T_{amb} = 0^{\circ}C \text{ to } +70^{\circ}C$ $C_L = 50pF, R_L = 500\Omega$		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	Waveform 1	105	120				MHz
t_{PLH} t_{PHL}	Propagation delay \overline{CP} to Q_n	Waveform 1	3.5 5.0	6.0 8.0	8.5 11.0	3.5 5.0	9.5 11.5	ns
t_{PLH} t_{PHL}	Propagation delay \overline{CP} to Q_s	Waveform 1	4.5 5.5	6.0 7.5	8.5 10.0	4.0 5.0	9.5 10.5	ns
t_{PHL}	Propagation delay \overline{MR} to Q_n	Waveform 2	5.0	7.5	10.0	5.0	10.5	ns
t_{PHL}	Propagation delay \overline{MR} to Q_s	Waveform 2	4.5	7.0	9.0	4.5	9.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	Waveform 4 Waveform 5	4.0 3.5	6.5 6.0	9.0 8.0	4.0 3.5	10.0 8.5	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level	Waveform 4 Waveform 5	1.0 1.0	2.5 3.5	4.5 5.5	1.0 1.0	5.5 6.5	ns

AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$V_{CC} = +5V$ $T_{amb} = +25^{\circ}C$ $C_L = 50pF, R_L = 500\Omega$			$V_{CC} = +5V \pm 10\%$ $T_{amb} = 0^{\circ}C \text{ to } +70^{\circ}C$ $C_L = 50pF, R_L = 500\Omega$		
			MIN	TYP	MAX	MIN	MAX	
$t_s(H)$ $t_s(L)$	Setup time, High or Low Dn to \overline{CP}	Waveform 3	2.5 1.5			3.0 2.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low Dn to \overline{CP}	Waveform 3	1.5 1.5			1.5 1.5		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low PE to \overline{CP}	Waveform 3	6.5 6.0			7.0 6.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low PE to \overline{CP}	Waveform 3	0 0			0 0		ns
$t_W(H)$ $t_W(L)$	\overline{CP} Pulse width High or Low	Waveform 1	5.0 4.0			5.5 4.5		ns
$t_W(L)$	\overline{MR} Pulse width Low	Waveform 2	2.5			3.0		ns
t_{REC}	Recovery time \overline{MR} to \overline{CP}	Waveform 2	6.0			7.0		ns

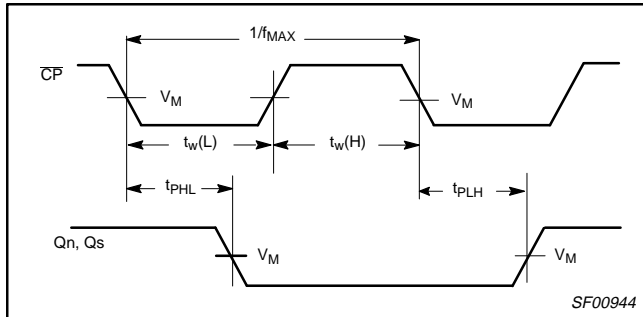
4-bit cascadable shift register (3-State)

74F395

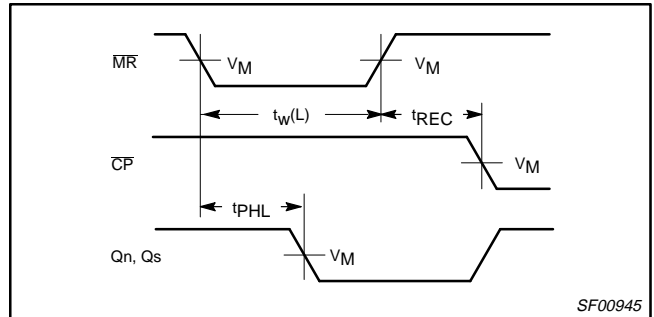
AC WAVEFORMS

For all waveforms, $V_M = 1.5V$.

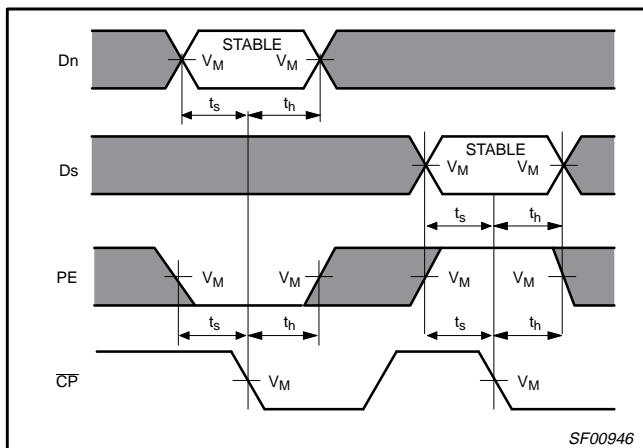
The shaded areas indicate when the input is permitted to change for predictable output performance.



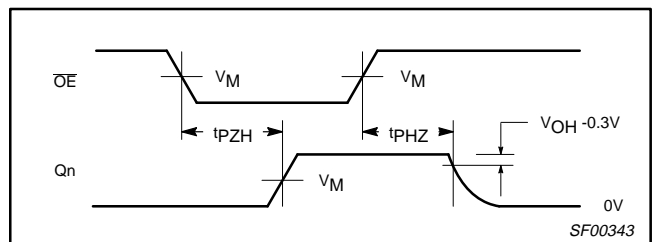
Waveform 1. Propagation Delay, Clock Input to Output, Clock Widths, and Maximum Clock Frequency



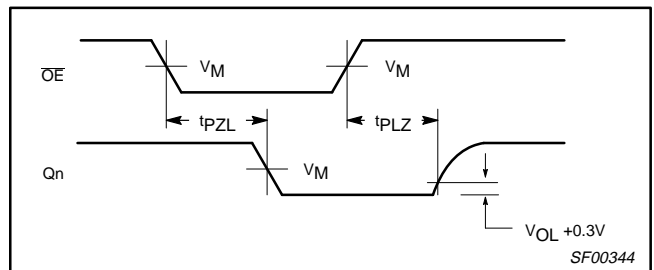
Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay, and Master Reset to Clock Recovery Time



Waveform 3. Parallel Enable and Data Setup Time and Hold Time



Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level

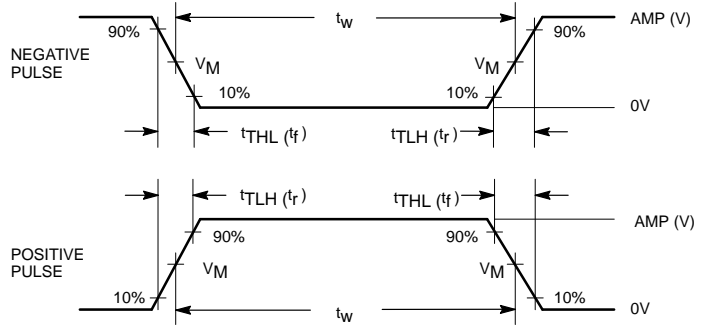
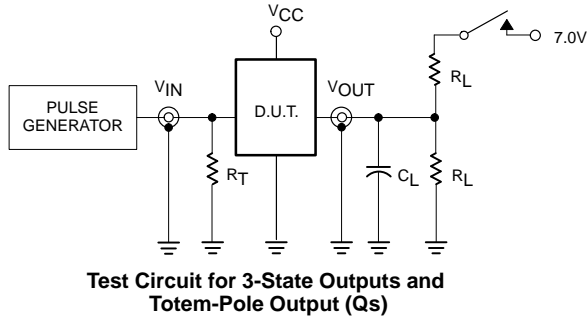


Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

4-bit cascadable shift register (3-State)

74F395

TEST CIRCUIT AND WAVEFORMS



SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

- R_L = Load resistor; see AC electrical characteristics for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
- R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00957