R8050
T-1 SERIAL TRANSMITTER

DESCRIPTION

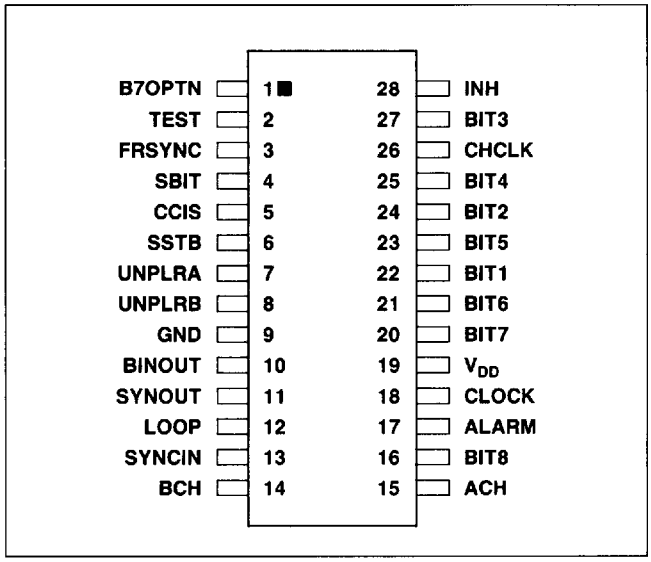
The Rockwell T-1 Serial Transmitter formats data to be serially transmitted according to T-1 D2 or T-1 D3 specifications, inserting framing and signalling bits along with 24 channels of 8-bit channel data. The T-1 Serial Transmitter also provides for alarm reporting via the Bit 2 inhibit method or, with minimal external logic, via the multiframe alignment signal (F_S) modification method.

Figure 1 is a functional block diagram of the T-1 Serial Transmitter. The Mod 193 counter is driven by the clock at 1.544 MHz and is either synchronized to the driving system by input signal SYNCIN or provides synchronization via output signal SYNOUT. Input signal FRSYNC applies synchronization to a Mod 12 counter, which identifies the frame of the 12-frame multiframe being processed.

The input data register latches data during each bit period, when the 8th bit of a channel sample is being transmitted. The data selector outputs the proper sequence of bits, as controlled by a bit count and frame count.

The zero channel monitor function causes Bit 8 or Bit 7 to be transmitted as a "one" if the channel data sample is all "zeros." Input INH provides a means to inhibit the zero channel monitor function. Input B7OPTN controls the particulars of the insertion method.

Two types of transmit formats are provided, a binary output and a paired unipolar output. The unipolar pair provides a means to externally create a single bipolar output with minimal logic.



Pin Configuration

FEATURES

- Single 5V supply, low power Schottky TTL compatible.
- Accepts 8 bits of parallel data as input.
- Generates output as 193 bit serial data stream in T-1, D2, D3 or D4 Mode 3 data format.
- Provides a channel and frame timing signal.
- Provides alternate control for alarm reporting and signalling.
- Provides automatic bit insertion for all-zero channel samples.

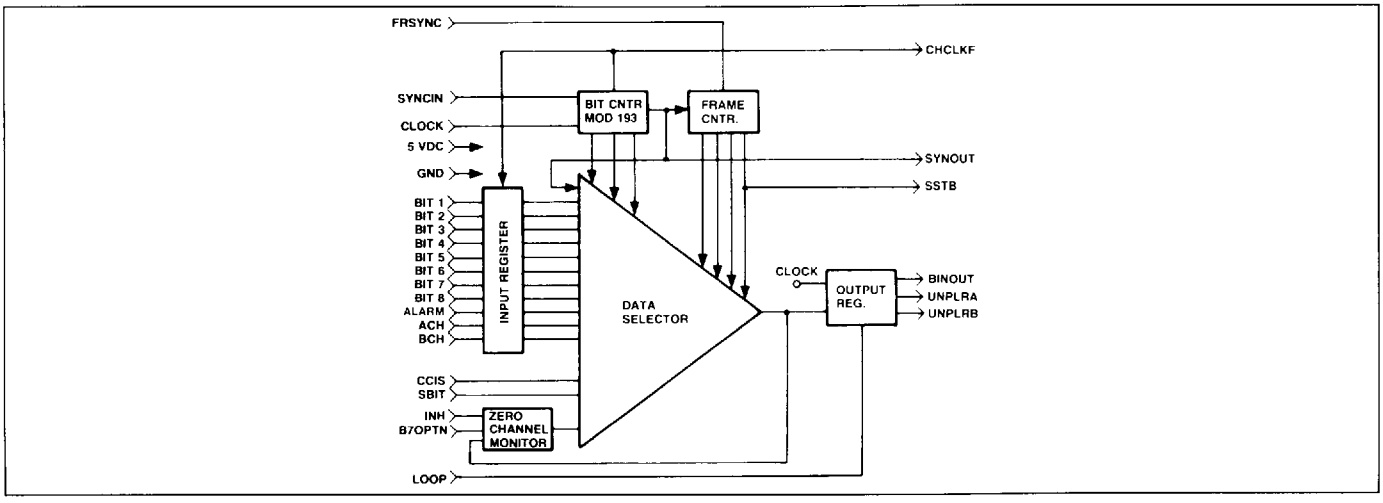


Figure 1. T-1 Serial Transmitter

T-1 TRANSMITTER INPUTS

Any input ≤0.8V = logic 0, low. Any input ≥2.0V = logic 1, high. The transition from a low level to a high level is called a rising edge, while the converse is defined as a falling edge.

FRSYNC: FRAME SYNCHRONIZATION

Frame sync allows external synchronization of the transmitter's internal frame counter. When FRSYNC becomes high, the frame counter is directly set to frame 1, the first of the twelve frames. If FRYSYNC is held high and does not return to zero before a rising edge of CLOCK, the subsequent states of BINOUT, UNPLRA and UNPLRB are high, high and low, respectively, regardless of the states of any other inputs. The latter mechanism is useful for device and/or board testing only and will cause bit errors and/or bipolar violations if used during field operations. See Figures 6 and 7.

SYNCIN: SYNCHRONIZATION INPUT

SYNCIN allows external synchronization of the internal Modulo 193 bit/channel counter. When SYNCIN becomes high, the Modulo 193 counter is directly set to the state corresponding to the output of the framing (F_T or F_S) bit. The first bit of channel one will be output on BINOUT (and UNPLRA or UNPLRB) as a result of the first rising edge of CLOCK following the return of SYNCIN to logic 0. See Figures 5 and 7.

TEST: ROCKWELL DEVICE TEST INPUT

Used only for Rockwell device testing. **Keep this input grounded.**

CLOCK: T-1 CLOCK

Maximum frequency = 1.6 MHz
Minimum pulse width = 275 ns
The T-1 bit period is bounded by the rising edges of this input.

INH: INHIBIT ZERO CHANNEL MONITOR

If INH is high, the zero channel monitor function is disabled, and Bits 7 and 8 are transmitted per corresponding inputs received. See Table 1.

For channels in signalling frames (6 or 12) in which the first six data bits and the signalling highway are all "zero," BIT 7 will be forced to one if INH is low. For any frame except a signalling frame Bit 8 or Bit 7 as selected by B7OPTN will be transmitted as a "one" if the channel input data is "zero" and INH is low.

BITS 1–8: PARALLEL CHANNEL DATA INPUTS

Bit 1, the sign bit, will be serially transmitted first, followed by Bits 2 through 8. The falling edge of CHCLKF indicates input channel data has been clocked into the input register and always occurs during the transmission of the final bit (Bit 8) of each channel data sample.

ACH: "A" CHANNEL HIGHWAY SIGNALLING

ACH allows the user to transmit one bit of signalling per channel as Bit 8 of each channel data sample in Frame 6 only. ACH is clocked into the input register by the falling edge of CHCLKF. Refer to Table 1 and Figure 4.

BCH: "B" CHANNEL HIGHWAY SIGNALLING

BCH allows the user to transmit one bit of signalling per channel as Bit 8 of each channel data sample in Frame 12 only. BCH is clocked into the input register by the falling edge of CHCLKF. Refer to Table 1 and Figure 4.

S-BIT: MULTIFRAME SIGNALLING BIT

SBIT, in conjunction with CCIS, provides an alternate way to control the multiframe signalling bit (F_S) transmission. The S-Bit input is transmitted as the multiframe signalling bit (F_S) if CCIS is held high. Refer to Table 2.

ALARM: LOCAL ALARM

Used for reporting alarm conditions. If the ALARM signal is high, Bit 2 (the most-significant bit) of every channel data sample of every frame is transmitting as a zero. This is commonly called remote alarm signalling. ALARM is clocked into the input register at the falling edge of CHCLKF. Refer to Table 1 and Figure 4.

LOOP: LOOP STRAP

Provided to aid testing of user applications. When enabled to a high level, LOOP forces the unipolar outputs to transmit alternating ones and zeros, regardless of input conditions, while BINOUT continues to provide normal data outputs. Refer to Figure 3.

CCIS: COMMON CHANNEL INTEROFFICE SIGNALLING STRAP

Provides optional control for replacing the automatic F_S pattern with a 4-kilobit common channel signalling path. When CCIS is high, the SBIT input replaces the F_S pattern and the insertion of ACH and BCH is suspended. The CCIS input may also be used to provide the alternate method of alarm reporting. See Figure 4.

B7OPTN: BIT 7 OPTION

Provides Bit 7 as an alternate bit position for "one" stuffing, as programmed by the zero channel monitor function. Refer to Table 1.

VSS, VDD: GROUND AND POWER

V_{DD} = +5 ±0.25 Vdc
V_{SS} = Ground, 0 Vdc

T-1 TRANSMITTER OUTPUTS

Low power TTL Schottky compatible. "1" ≥ 2.4 Vdc, "0" ≤ 0.4 Vdc, CMOS — 12KΩ pullup to V_{DD} required.

SSTB: 4 kHz SIGNALLING CHANNEL STROBE

SSTB is the least-significant bit of the frame counter. Unless it is directly set by FRSYNC, SSTB will go high as each framing bit (F_T) is serially transmitted, and will return low as each multiframe alignment signal (F_S) is transmitted. Refer to Figure 2.

SYNOUT: CHANNEL SYNC OUTPUT

SYNOUT provides a means to synchronize to the internal bit counter (Mod 193). SYNOUT is high for one bit time, beginning just prior to the first data bit of a frame being serially transmitted. Refer to Figure 7. SYNOUT is the only output determined by the falling edge of CLOCK.

CHCLKF: CHANNEL CLOCK FALSE

The falling edge of CHCLKF, occurring as Bit 8 of any channel is being serially transmitted, indicates input data has been clocked into the input register. With the exception of an extra bit period extending the low level duration at frame bit time, CHCLKF is a divide-by-eight of CLOCK. Refer to Figure 2.

BINOUT: SERIAL DATA OUTPUT, BINARY FORMATTED

BINOUT is the binary formatted serial conversion of the parallel input data. The programmed format of BINOUT follows Tables 1 and 2.

BINOUT is synchronously transmitted as a high level if FRSYNC remains high during the rising edge of CLOCK. Refer to Figures 6 and 7.

UNPLRA, UNPLRB: T-1 SERIAL DATA UNIPOLAR OUTPUTS

Two paired unipolar outputs are provided for the purpose of creating a single serial data output transmission in bipolar format. The unipolar output register toggles for each "one" bit to be serially transmitted. UNPLRA and UNPLRB are transmitted as complements for "one" data bits and as low levels for "zero" data bits. See Figure 3.

The input signal LOOP, if high, forces the unipolar outputs to toggle every bit time, regardless of input data.

FRSYNC perturbs the current bits being transmitted by UNPLRA and UNPLRB. If FRSYNC remains high during the rising edge of CLOCK, UNPLRA will be transmitted as a high level and UNPLRB will be low. Refer to Figures 6 and 7.

Table 1. Serial Channel Sample Output Data Truth Table

Inputs X = don't care													Current Frame Number	Binout Serial Output Channel Bit Position								Notes
ALARM	INH	B7OPTN	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7	BIT 8	ACH	BCH		1	2	3	4	5	6	7	8	
1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	1
X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	1
0	X	X	P	Q	R	S	T	U	V	X	A	X	6	P	Q	R	S	T	U	V	A	2
0	X	X	P	Q	R	S	T	U	V	X	X	B	12	P	Q	R	S	T	U	V	B	2
0	X	X	P	Q	R	S	T	U	V	W	X	X	Y	P	Q	R	S	T	U	V	W	2,3
0	1	X	0	0	0	0	0	0	0	X	A	X	6	0	0	0	0	0	0	0	A	
0	1	X	0	0	0	0	0	0	0	X	X	B	12	0	0	0	0	0	0	0	B	
0	1	X	0	0	0	0	0	0	0	W	X	X	Y	0	0	0	0	0	0	0	W	3
0	0	X	0	0	0	0	0	0	0	X	0	X	6	0	0	0	0	0	0	1	0	
0	0	X	0	0	0	0	0	0	0	X	X	0	12	0	0	0	0	0	0	1	0	
0	0	1	0	0	0	0	0	0	0	0	X	X	Y	0	0	0	0	0	0	1	0	3
0	0	0	0	0	0	0	0	0	0	0	X	X	Y	0	0	0	0	0	0	0	1	3

NOTES: (1) ALARM = 1 has the same effect as BIT 2 = 0
(2) P, Q, R, S, T, U and V may not simultaneously be zero, unles A, B or W is 1
(3) Y is any frame $\neq$ 6 and $\neq$ 12 with CCIS = 0, or all frames with CCIS = 1

Table 2. Framing Bit (F_T & F_S) Output Data

Frame Number	Processed Bit	Binout	
		CCIS = 0	CCIS = 1
1	F_T	1	1
2	F_S	0	SBIT
3	F_T	0	0
4	F_S	0	SBIT
5	F_T	1	1
6	F_S	1	SBIT
7	F_T	0	0
8	F_S	1	SBIT
9	F_T	1	1
10	F_S	1	SBIT
11	F_T	0	0
12	F_S	0 (NOTE 1)	SBIT

Notes: (1) Alternate remote alarm reporting may be accomplished by holding SBIT and CCIS both high just prior to initiation of Frame 12.
(2) F_T bit insertion is automatic and no optional control is provided.

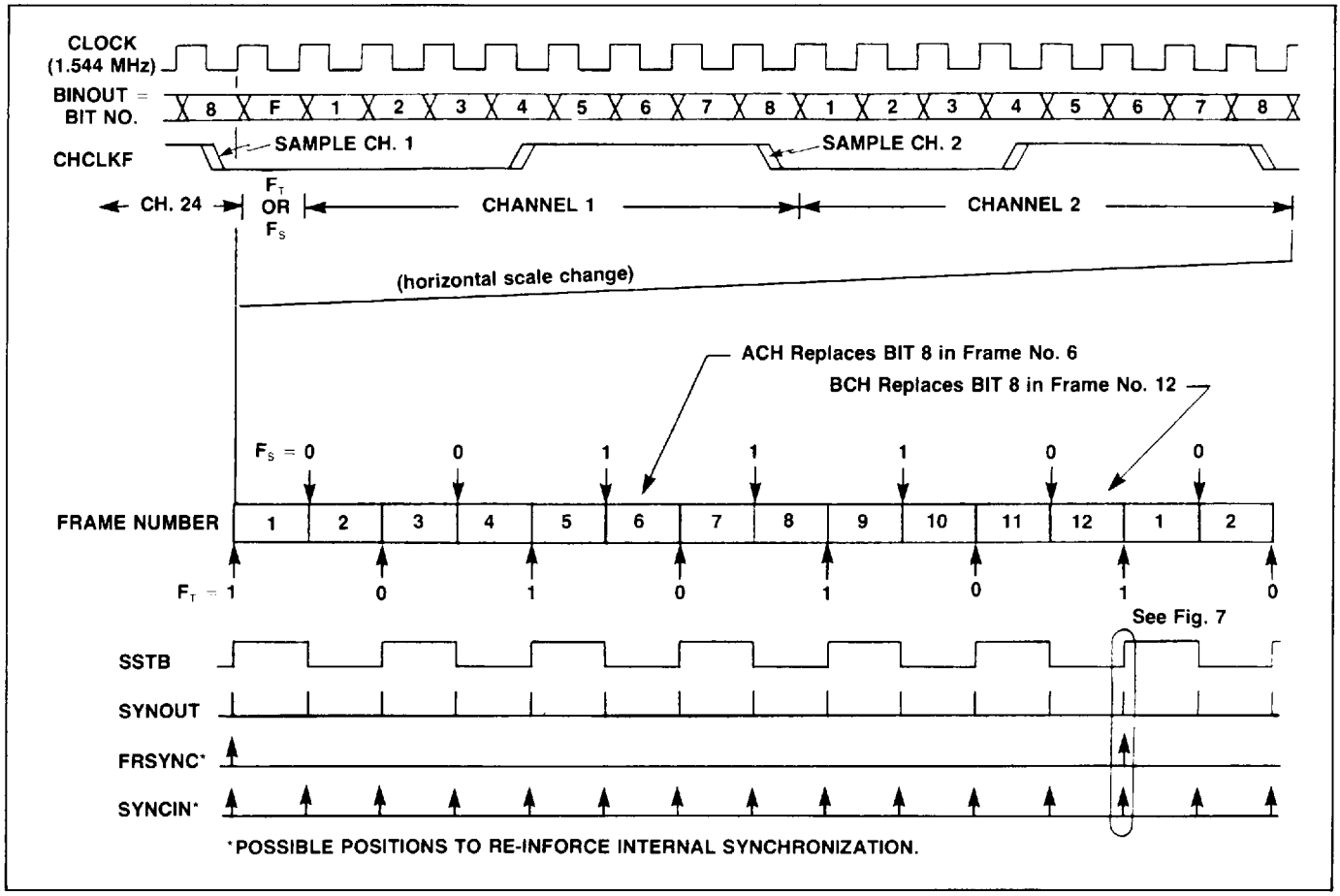


Figure 2. Transmitter Input-Output Signal Relationships

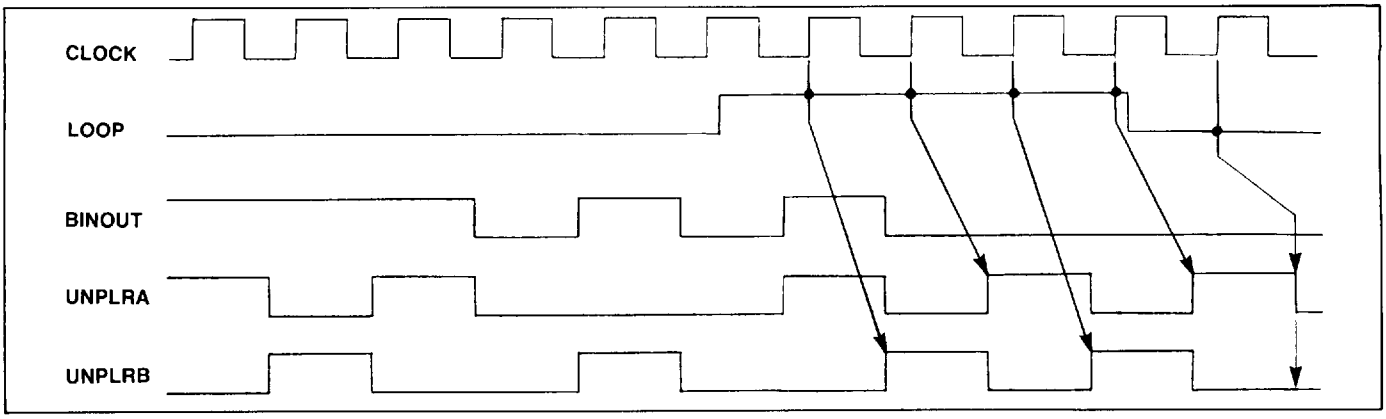


Figure 3. Transmitter Binary, Unipolar Outputs

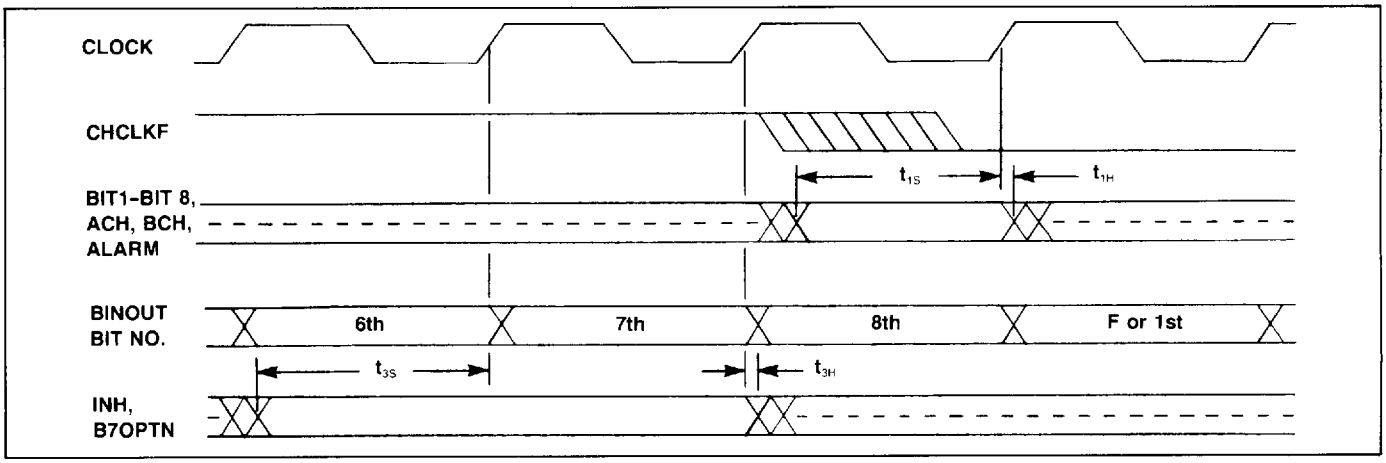


Figure 4 (a). Channel Input Timing

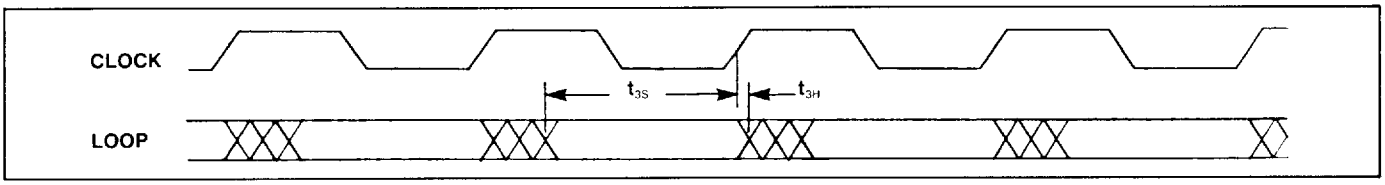
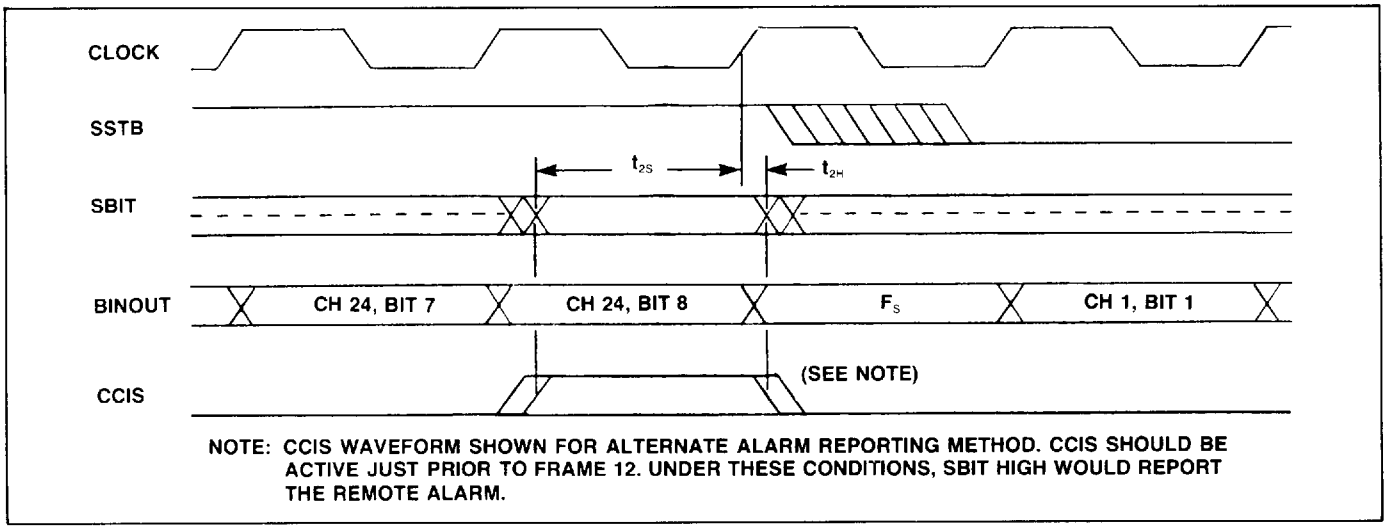


Figure 4 (b). LOOP Input Timing



NOTE: CCIS WAVEFORM SHOWN FOR ALTERNATE ALARM REPORTING METHOD. CCIS SHOULD BE ACTIVE JUST PRIOR TO FRAME 12. UNDER THESE CONDITIONS, SBIT HIGH WOULD REPORT THE REMOTE ALARM.

Figure 4 (c). Control Input Timing

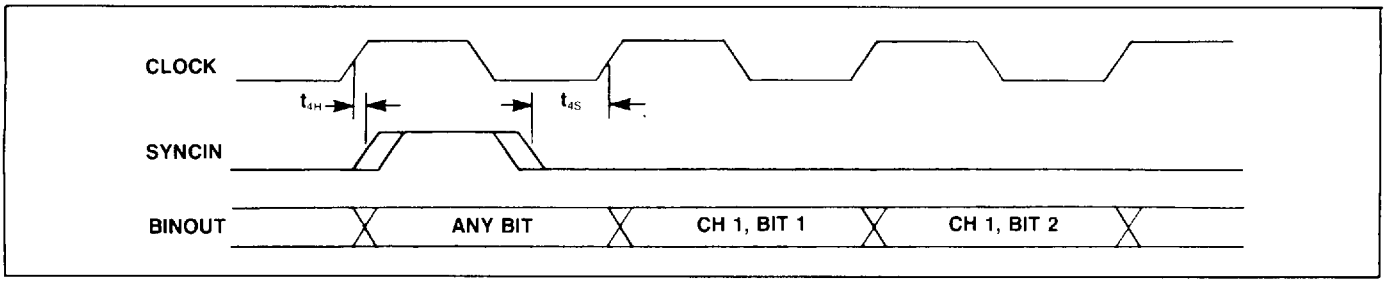


Figure 5. SYNCIN Timing Relationship

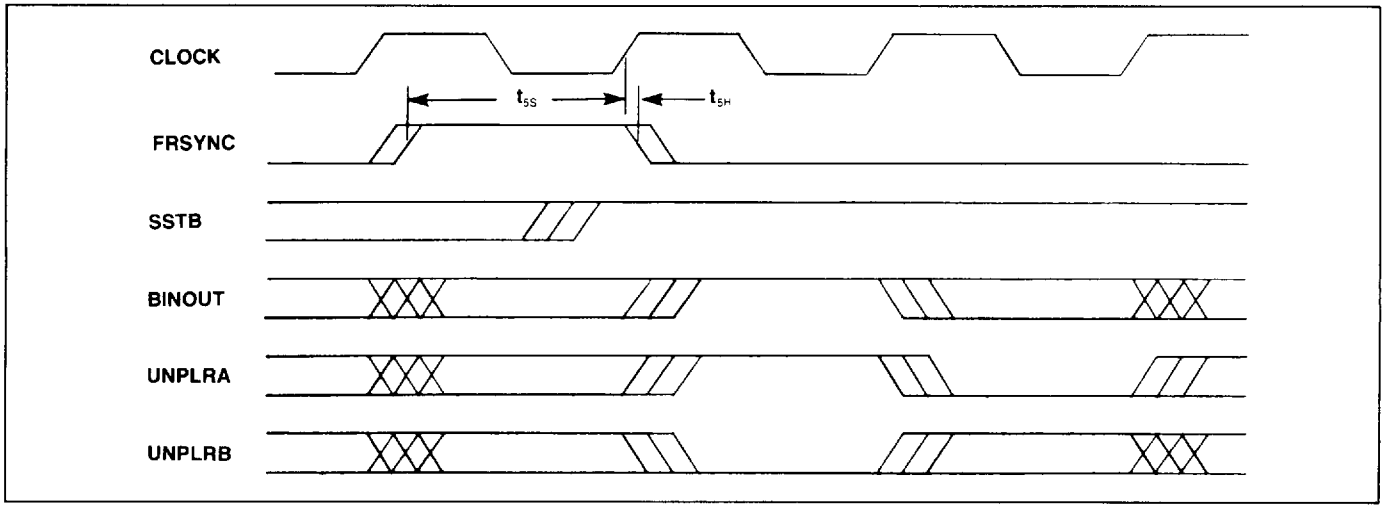


Figure 6. Non-return-to-zero FRSYNC Timing

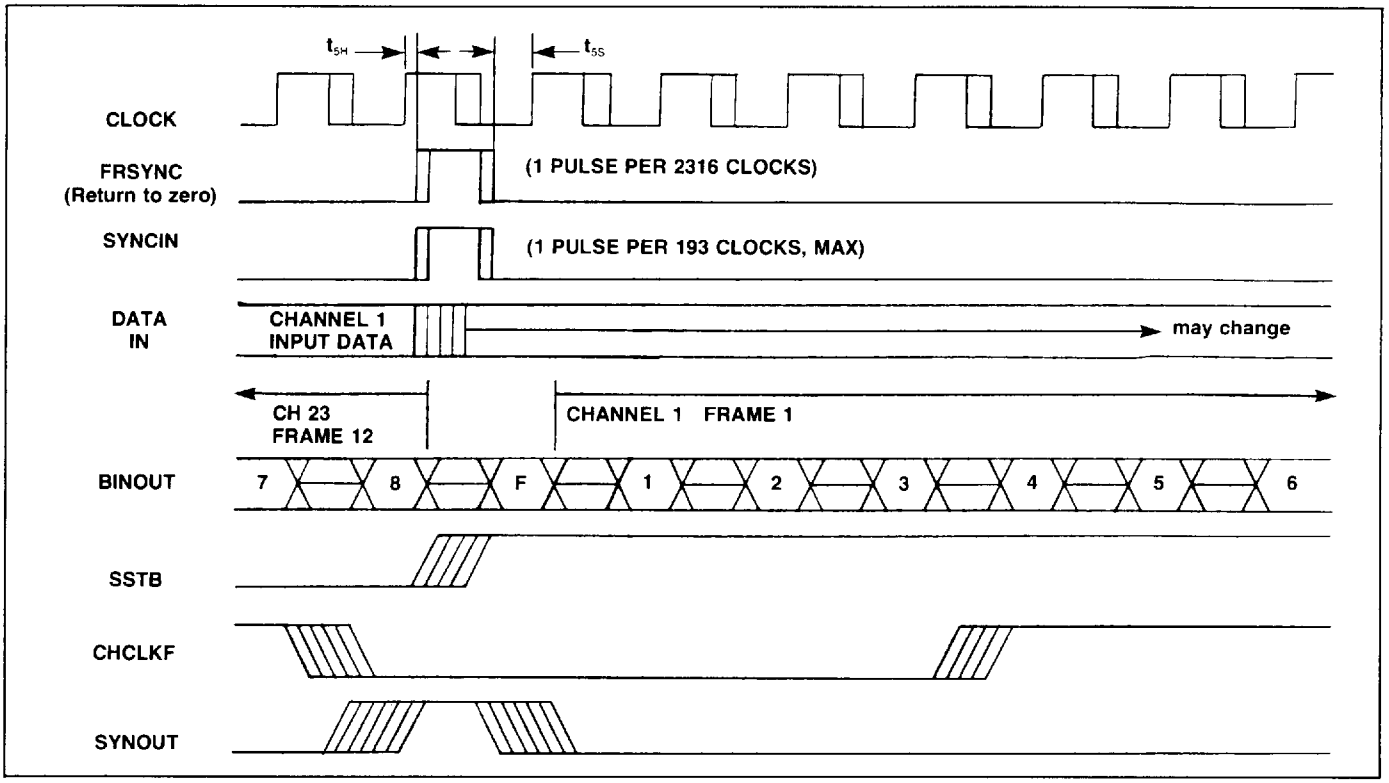


Figure 7. Transmitter External Synchronization (Return-to-zero FRSYNC)

Table 3. Input Timing

Symbol	Parameter	Min	Max	Unit
t_{1S}	Buffered Data Setup Time	450		ns
t_{1H}	Buffered Data Hold Time	0		ns
t_{2S}	Control Input Setup Time	400		ns
t_{2H}	Control Input Hold Time	20		ns
t_{3S}	Asynchronous Control Input Setup Time	350		ns
t_{3H}	Asynchronous Control Input Hold Time	20		ns
t_{4S}	SYNCIN Setup Time	200		ns
t_{4H}	SYNCIN Hold Time	20		ns
	SYNCIN Pulse Width	100		ns
t_{5S}	Frame Sync Setup Time (Return to Zero)	250		ns
t_{5H}	Frame Sync Hold Time (Return to Zero)	20		ns
	Frame Sync Pulse Width	200		ns
t_{5S}	Frame Sync Setup Time (Non-Return to Zero)	525		ns
t_{5H}	Frame Sync Hold Time (Non-Return to Zero)	20		ns

Table 4. Output Propagation Delay, Worst Case
(Measured from Rising Edge of Clock Unless Stated Otherwise)

Output	Max Delay	Unit
SSTB	500	ns
SYNOUT	500	ns
Ref from Falling Edge of Clock		
CHCLKF	500	ns
BINOUT	500	ns
UNPLRA	500	ns
UNPLRB	500	ns

MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	+4.75 to +5.25	Vdc
Operating Temperature	T_{OP}	0 to 70	°C
Storage Temperature	T_{STG}	−55 to +150	°C

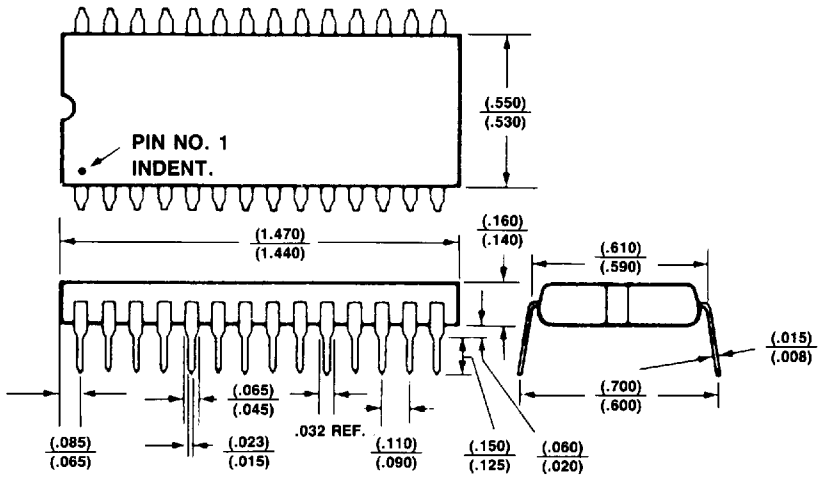
***NOTE:** Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 5.0 ±5%)

Parameter	Symbol	Min	Max	Unit
Logical "1" Input Voltage	V_{OH}	2.0	V_{DD} + 0.3	V
Logicical "0" Input Voltage	V_{IL}	−0.3	0.8	V
Logicical "1" Output Voltage	V_{OH}	2.4	—	V
Logic "0" Output Voltage	V_{OL}	—	0.4	V
Output Source Current	I_{OH}	−100	—	μA
Output Sink Current	I_{OL}	400	—	μA
Capacitance Load (any output)	C	—	25	pF
Input Capacitance (any input)	C_{IN}	—	5	pF
Clock Frequency		—	1.6	MHz
Power Dissipation	P_D	—	250	mW

PACKAGE DIMENSIONS



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