TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC94A29FAG, TC94A29FB

Single-Chip CD Processor with Built-in Controller (CD-CX)

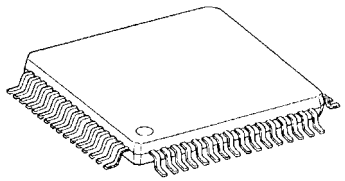
The TC94A29FAG/FB is a single-chip CD processor for digital servo, which incorporates a 4-bit microcontroller.

The controller features an LCD driver, 4-channel 6-bit AD converter, 1 port 2-channel 2/3-line or UART serial interface module, a buzzer, 20-bit general-purpose counter function, interrupt function, and 8-bit timer/counter. The CPU can select one of four operating clocks (16.9344-MHz, 75-kHz or 32.768-kHz crystal oscillator and CR oscillator), facilitating interface with the CD processor.

The CD processor incorporates sync separation protection and interpolation, EFM demodulator, error correction, digital equalizer for servo, and servo controller. The CD processor also incorporates a 1-bit DA converter. In combination with the TA2157F/FN digital servo head amplifier, the TC94A29FAG/FB can very simply configure an adjustment-free CD player.

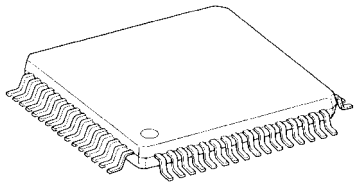
Thus, the IC is suitable for CD systems for automobiles and radio-cassette players.

TC94A29FAG



LQFP64-P-1010-0.50

TC94A29FB



QFP64-P-1212-0.65

Weight
LQFP64-P-1010-0.50: 0.32 g (typ.)
QFP64-P-1212-0.65: 0.45 g (typ.)

Features

- Single-chip CD processor with on-chip CMOS LCD driver and 4-bit microcontroller
- Operating supply voltage:
  - CD in operation: V_{DD} = 3.0 to 3.6 V (3.3 V typ.)
  - CD stopped: V_{DD} = 1.8 to 3.6 V (only CPU in operation)
- Supply current:
  - CD in operation: I_{DD} = 30 mA (typ.)
  - CD stopped: I_{DD} = 1.5 mA (CD standby mode, with 16.9344-MHz crystal oscillator, CPU in operation)
  - CD stopped: I_{DD} = 50 μA (CD standby mode, with 75-kHz crystal oscillator, CPU in operation)
- Operating temperature range: Ta = −40 to 85°C
- Package: LQFP/QFP-64 (0.5/0.65-mm pitch, 1.4 mm thick)
- E^2PROM: TC94AE29FAG/FB

4-bit Microcontroller

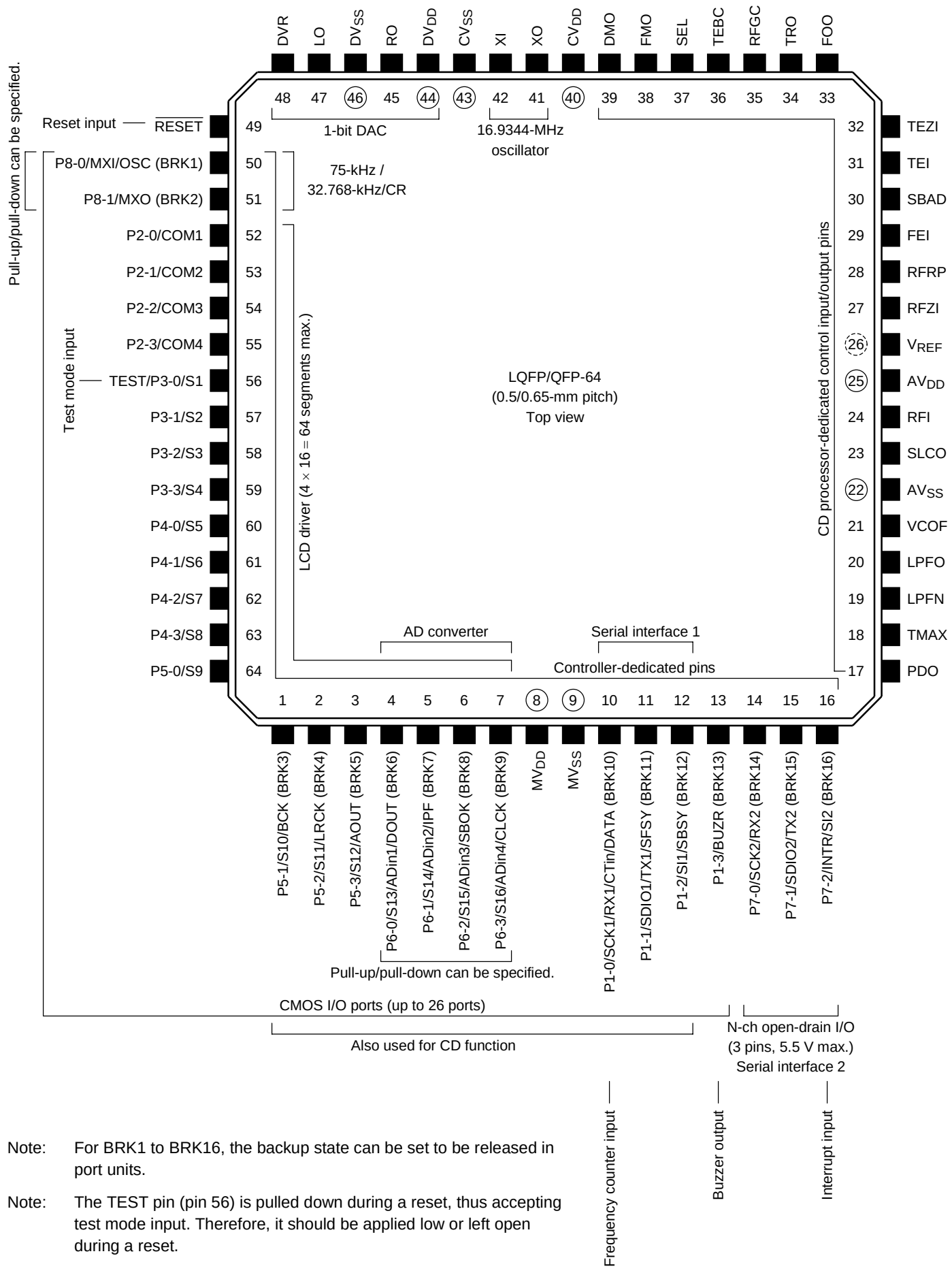
- Program memory (ROM): 16 bits × 8 Ksteps
- Data memory (RAM): 4 bits × 512 words
- Instruction execution time: 1.42 μs, 40 μs, 91.6 μs, TOSC × 3 (Every instruction consists of a single word.)
- Crystal oscillator frequency: 16.9344 MHz, 75 kHz, 32.768 kHz, CR oscillation frequency
- Stack levels: 6
- AD converter: 6 bits × 4 channels
- LCD driver: 1/4 duty, 1/2 or 1/3 bias method, 64 segments (max.)
- I/O ports: CMOS I/O ports: 26 (max.)
  N-channel open-drain I/O ports (for up to 5.5 V): 3 (max.)
- Timer/counter: 8 bits (timer mode, pulse width detector and measure function)
- General-purpose counter: 20 bits, 0.1 MHz to 20 MHz, Vin = 0.2 Vpp (min.), input amplifier incorporated
- Serial interface module: 1 port 2 channel supporting 2/3-line method or UART (two input channels)
- Four buzzer types: 0.75 kHz, 1 kHz, 1.5 kHz, and 3 kHz
- Four modes: continuous, single-shot, 10 Hz intermittent, and 10 Hz intermittent at 1 Hz intervals
- Interrupts: 1 external, 3 internal (CD sub-sync, serial interface, 8-bit timer)
- Back-up mode: Four types: CD standby (CD processor stopped)
  Clock stop (oscillator stopped)
  Hardware wait (only crystal oscillator in operation)
  Software wait (CPU in intermittent operation)
- Reset function: Power-on reset circuit, supply voltage detector (detection voltage = 1.5 V typ.)

CD Processor

- Reliable sync pattern detection, sync signal protection and interpolation
- Built-in EFM demodulator and subcode decoder
- High-correction capability using Cross Interleave Read Solomon Code (CIRC) logical equation
  C1 correction: dual
  C2 correction: quadruple
- Jitter absorption capability of ± 6 frames
- Built-in 16 KB RAM
- Built-in digital output circuit
- Built-in L/R independent digital attenuator
- Bilingual audio output
- Audio output: 32fs, 48fs or 64fs selectable
- Subcode Q data is read-timing free and can be driven out in sync with audio data.
- Built-in data slicer and analog PLL (adjustment-free VCO used) circuit
- Automatic adjustment of loop gain, offset, and balance at focus servo and tracking servo
- Built-in RF gain auto-adjusting circuit
- Built-in digital equalizer for phase compensation
- Supports different pickups using on-chip digital equalizer coefficient RAM.
- Built-in focus and tracking servo control circuit
- Search control supports all modes and realizes high-speed, stable search.
- Lens kick and feed kick use speed control method.
- Built-in AFC and APC circuits for disc motor CLV servo
- Built-in defect/shock detector
- Built-in 8 times over-sampling digital filter and 1-bit DA converter
- Built-in analog filter for 1-bit DA converter
- Built-in zero-data detection output circuit
- Supports double-speed operation.

Note: Output pins for subcode Q data and audio data have multiplexed functions for controller-dedicated pins. The function of each pin can be switched by program.

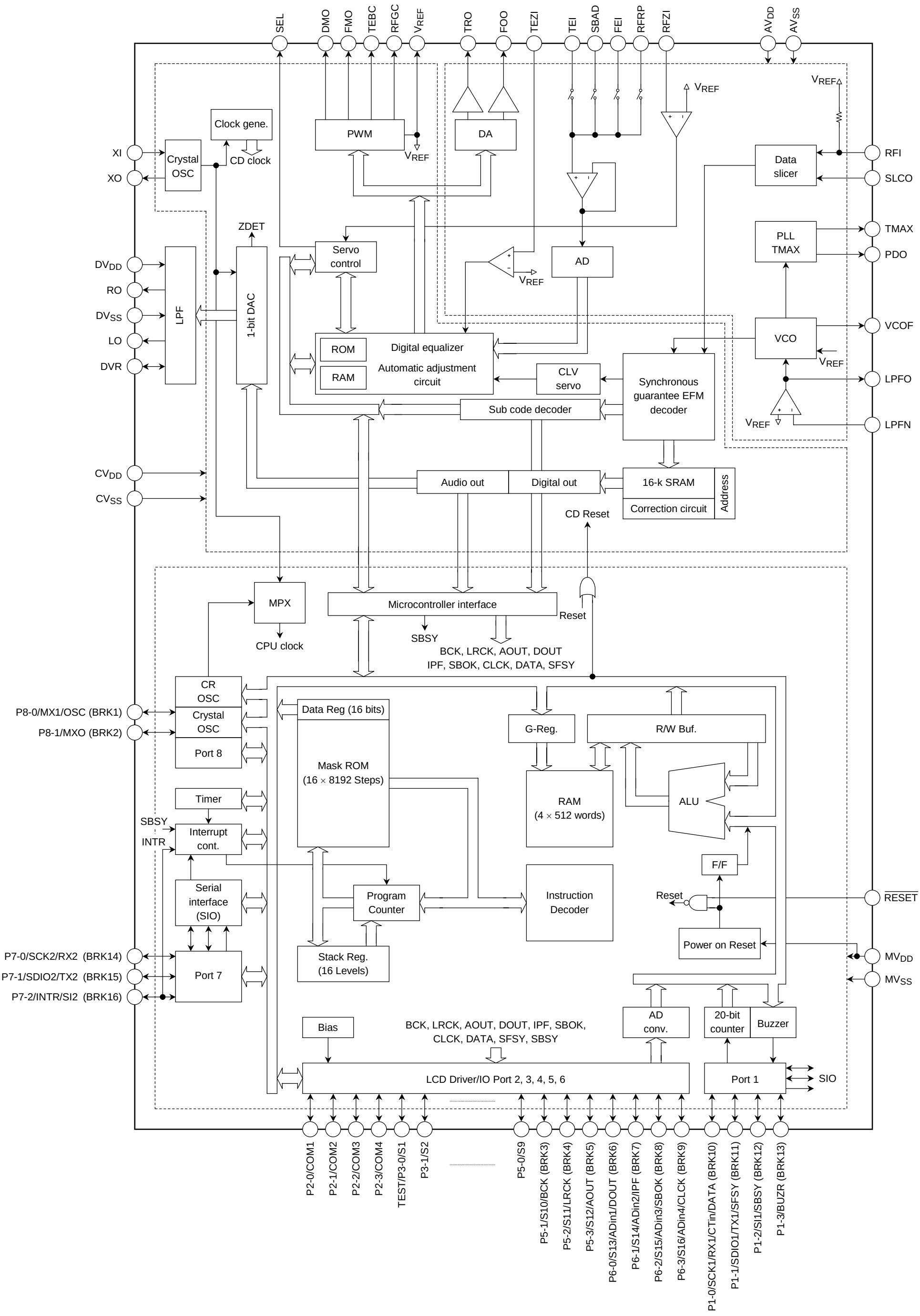
Pin Connections



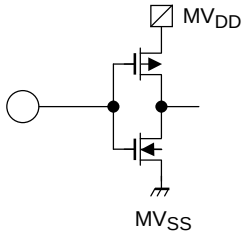
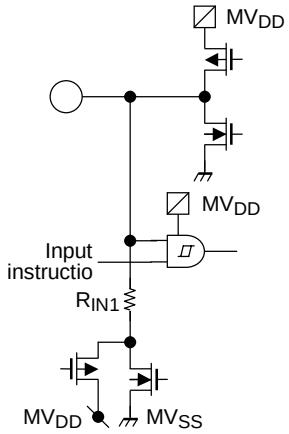
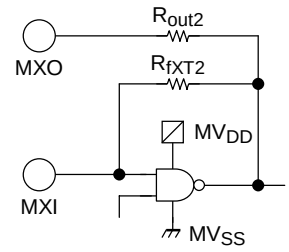
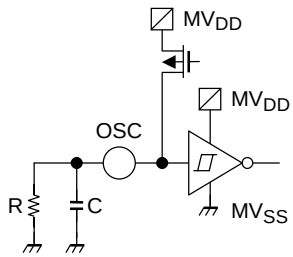
Note: For BRK1 to BRK16, the backup state can be set to be released in port units.

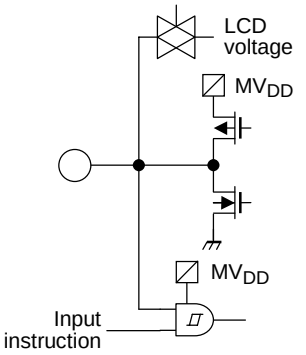
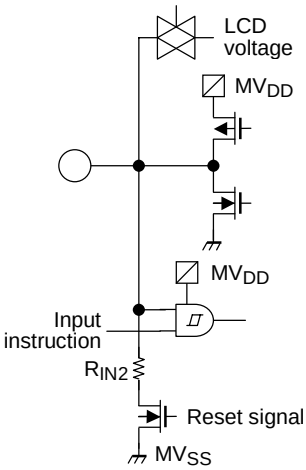
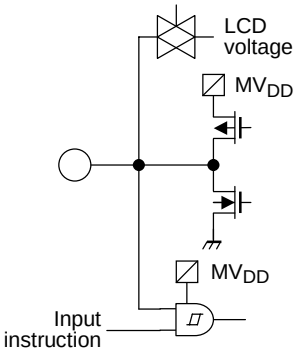
Note: The TEST pin (pin 56) is pulled down during a reset, thus accepting test mode input. Therefore, it should be applied low or left open during a reset.

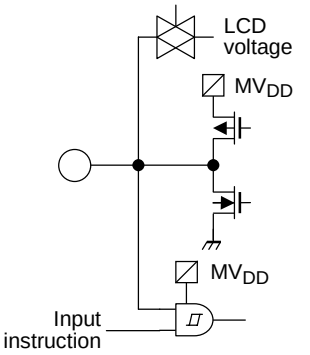
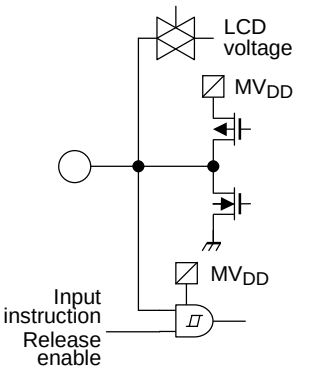
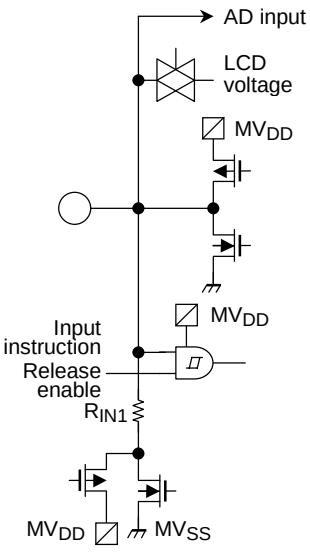
Block Diagram

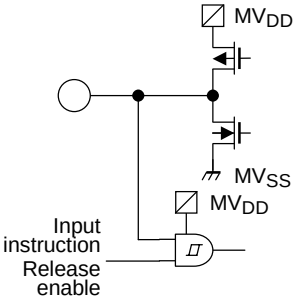
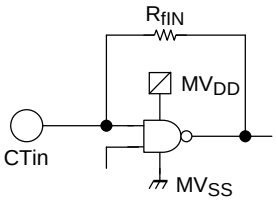
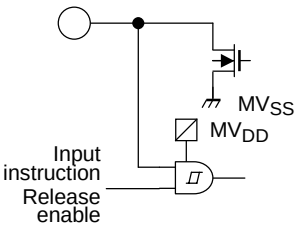


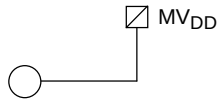
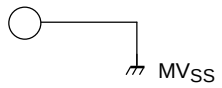
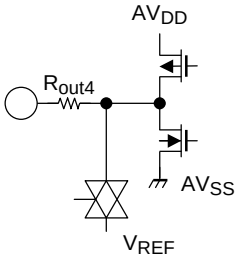
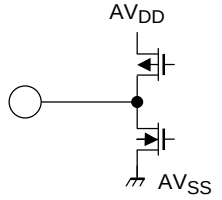
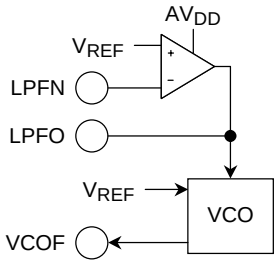
Pin Functions

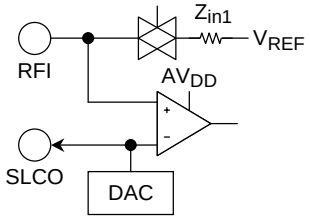
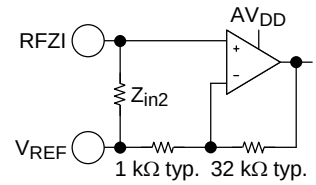
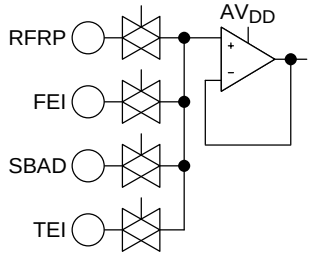
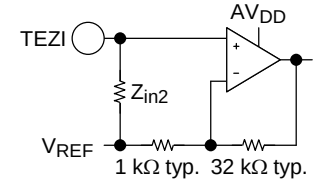
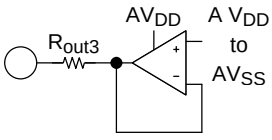
Pin No.	Symbol	Pin Name	Function and Operation	Remarks
49	$\overline{\text{RESET}}$	Reset input	System reset input pin for the device. A reset is applied while the $\overline{\text{RESET}}$ signal is low. When it is high, the 16.9344-MHz crystal oscillator (XI, XO) starts operating. The controller counts clock pulses from this oscillator and waits a specified standby time (approximately 50 ms) before starting the controller program from address 0. The CD processor is placed in the standby state at this time. Normally, raising the voltage on MVDD from 0 to 1.8 V or higher triggers a system reset (power-on reset) so that the $\overline{\text{RESET}}$ pin should be held at high.	
50 51	P8-0 /MXI /OSC (BRK1) P8-1 /MXO (BRK2)	I/O port 8-0 /crystal oscillator /CR oscillator I/O port 8-1 /crystal oscillator	2-bit CMOS I/O port. Input/output can be specified for each bit. When the pins are used as I/O port input, each pin can be pulled up or down by program. When backup release for clock stop mode or wait mode is enabled for the pins, a change in a pin can release the backup state. The program can set these pins to be used for a 75-kHz or 32.768-kHz dedicated crystal oscillator. The P8-0 pin can also be used for a CR oscillator. These clocks are used for the operation of the controller and peripheral devices. Upon a system reset, the 16.9344-MHz crystal oscillator (XI, XO) is selected as the clock for controller and peripheral device operation. The program can subsequently set the pins to oscillator pins and switch the clock generated from the oscillator to the controller clock. When the pins are used for an oscillator, executing the CKSTP instruction causes its oscillation to stop. (Note) When the P8-0 pin is used for a CR oscillator, the P8-1 pin can used as an I/O port pin. (Note) Backup release is enabled for both pins simultaneously. (Note) Use a crystal oscillator having a good startup characteristic. (Note) Upon a system reset, the pins are set to I/O port input. (Note) After setting the pins to oscillator pins, wait until oscillation settles before switching the controller clock.	 (When used for I/O port)  (When used for crystal oscillator)  (When P8-0 is used for CR oscillator)

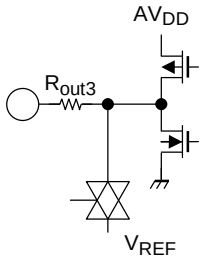
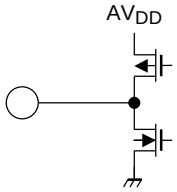
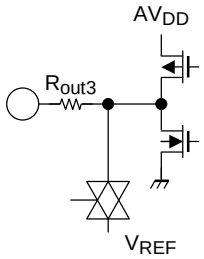
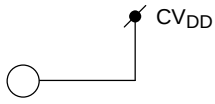
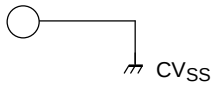
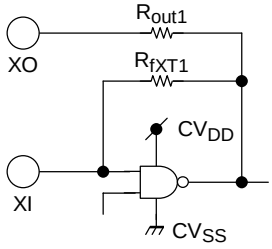
Pin No.	Symbol	Pin Name	Function and Operation	Remarks
52 53 54 55	P2-0/COM1 P2-1/COM2 P2-2/COM3 P2-3/COM4	I/O port 2 /LCD common output	24-bit CMOS I/O port and 3-bit N-channel open-drain I/O port. Input/output can be specified for each bit. When the P6-0 to P6-3 pins are used as I/O port input, each pin can be pulled up or down by program. When the P5-1 (BRK3) to P7-2 (BRK16) pins are used as I/O port input and backup release for clock stop mode or wait mode is enabled for those pins (enabled/disabled in port units), a change in any of the pins can release the backup state. The P7-0 to P7-2 pins constitute an N-channel open-drain I/O port, to which a voltage of up to 5.5 V can be applied. I/O ports 2 to 6 can be set to LCD driver output pins by program. The COM1 to COM4 pins drive common signals to the LCD panel while the S1 to S16 pins drive segment signals. The COM1 to COM4 signals configure a matrix with the S1 to S16 signals to display up to 64 segments. When the LCDoff bit is set to 0, the COM1 to COM4 and S1 to S4 pins are collectively set to LCD output. For S5 to S16, the program can specify either I/O port or segment output individually for each pin. The LCD can be driven by the 1/4-duty, 1/2-bias method (frame frequency: 62.5 Hz) or the 1/4-duty, 1/3-bias method (frame frequency: 125 Hz). When the 1/2 bias method is set, three common output levels (MVDD, 1/2MVDD and GND) and two segment output levels (MVDD and GND) appear on the pins. When the 1/3 bias method is set, four common and segment output levels (MVDD, 1/3MVDD, 2/3MVDD and GND) appear on the pins. Upon a system reset or after clock stop mode is released, a non-select waveform (bias voltage) is driven and the DISP OFF bit is set to 0, after which the common signals are driven. During a system reset ($\overline{\text{RESET}}$ = low), the TEST/P3-0/S1 pin is pulled down and accepts test mode input. This pin should be left open or applied low level during a reset. The P5-1 to P6-3 and P1-0 to P1-2 pins can be set to CD processor-dedicated pins on a per pin basis. The CD processor functions are as follows: (Continued on next page)	
56	TEST /P3-0/S1	Test input /I/O port 3-0 /LCD segment output		
57 58 59	P3-1/S2 P3-2/S3 P3-3/S4	I/O port 3 /LCD segment output		
60 61 62 63	P4-0/S5 P4-1/S6 P4-2/S7 P4-3/S8	I/O port 4 /LCD segment output		

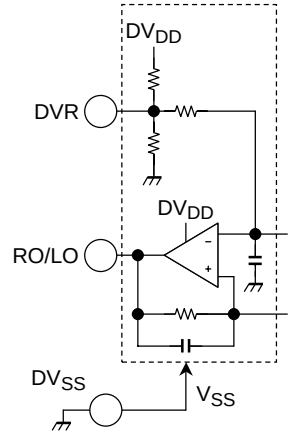
Pin No.	Symbol	Pin Name	Function and Operation	Remarks
64	P5-0/S9	I/O port 5-0 /LCD segment output	●BCK: Bit clock output pin. One of three frequencies, 32, 48 or 64 can be specified using a CD command. At normal speed: 32 f_S = 1.4112 MHz ●LRCK: LR channel clock output pin. For the L channel, this pin drives a low level. For the R channel, it drives a high level. The polarity can be inverted using a CD command. At normal speed: 44.1 kHz ●AOUT: Audio data output pin. Either MSB first or LSB first can be specified using a CD command. ●DOUT: Digital data output pin. It drives data at up to double speed (complying with CP-1201). ●IPF: Correction flag output pin. If the AOUT output is C2 error detection/correction, a high level appears to indicate an uncorrectable symbol. (Also called C2PO) ●SBOK: CRCC test result output pin for subcode Q data. A high level appears when the data has passed the test. ●CLCK: Clock input/output pin for reading subcode P to W data. The input/output polarity can be inverted using a CD command. ●DATA: Subcode P to W data output pin. ●SFSY: Frame sync signal output pin for playback. ●SBSY: Block sync signal output pin for subcode. When a subcode sync is detected, a high level appears at S1. The controller enables CD interrupts. When an interrupt occurs on the falling edge of the SBSY signal, the program jumps to address 2. (Note) Interrupts should not be enabled when CD processor operation is undefined. P6-0 to P6-3 pins have multiplexed functions for the on-chip 6-bit 4-channel AD converter analog input. The on-chip AD converter uses successive approximation. The conversion time is 242 μs when the 16.9344-MHz crystal oscillator is used and 7 instruction cycles (280 μs) when the 75-kHz crystal oscillator is used. The program can specify necessary pins for AD analog input on a per bit basis. The internal power supply (MV_{DD}) is used as the reference voltage. When the P6-0 to P6-3 pins are used as I/O port input, each pin can be pulled up or down by program. (Continued on next page)	
1 2 3	P5-1/S10 /BCK (BRK3) P5-2/S11 /LRCK (BRK4) P5-3/S12 /AOUT (BRK5)	I/O port 5 /LCD segment output /CD processor function		
4 5 6 7	P6-0/S13 /ADin1 /DOUT (BRK6) P6-1/S14 /ADin2 /IPF (BRK7) P6-2/S15 /ADin3 /SBOK (BRK8) P6-3/S16 /ADin4 /CLCK (BRK9)	I/O port 6 /LCD segment output /CD processor function		

Pin No.	Symbol	Pin Name	Function and Operation	Remarks
10	P1-0/SCK1 /RX1 /CTin /DATA (BRK10)	I/O port 1-0 /serial clock input/output 1 /serial receive data 1 /counter clock input /CD processor function	The P1-0 pin has multiplexed functions for general-purpose counter input. The input frequency is 0.1 MHz to 20 MHz. The counter incorporates an input amplifier and operates with capacitance-coupled small amplitudes. The counter is a 20-bit counter and can store 20-bit data directly in memory. The gate time can be selected from among 1 ms, 4 ms, 16 ms and 64 ms (when the 75-kHz crystal oscillator is used). In manual mode, the gate can be turned on and off within the specified time using instructions. The P1-0 to P1-2 and P7-0 to P7-2 pins have multiplexed functions for serial interface (SIO) circuit input/output pins. The SIO is a serial interface supporting 2-line and 3-line methods as well as UART. The TC94A29FAG/FB has CMOS input/output pins (SCK1/RX1, SDIO1/TX1, SI1) and N-channel open-drain (supporting up to 5.5 V) input/output pins (SCK2/RX2, SDIO2/TX2, SI2). One of the two sets of pins can be selected as serial interface. The serial interface circuit supports various options, including the number of the clock edge to be used, the serial clock input/output, and the clock frequency. These options facilitate controlling the LSI and communications between the controllers. When SIO interrupts are enabled, an interrupt is generated as soon as execution of the SIO completes, causing the program to jump to address 4. The P1-3 pin has multiplexed functions for a buzzer output pin. One of four frequencies within the range from 0.75 kHz, 1 kHz, 1.5 kHz and 3 kHz can be selected for buzzer output (when the 75-kHz clock is used). The buzzer is driven at the selected frequency in one of four modes: continuous, single-shot, 10-Hz intermittent, and 10-Hz intermittent at 1-Hz intervals. The P7-2 pin has multiplexed functions for an external interrupt input pin. When interrupts are enabled and a pulse of 1.65 μs to 4.96 μs or more (13.3 μs to 40 μs when the 75-kHz clock is used) is applied to this pin, an interrupt is generated and the program jumps to address 1. The input logic and rising/falling edge can be selected for interrupt inputs. This input can be applied as the clock gate signal to the internal 8-bit timer/counter, which allows input pulse width to be detected and measured. (Note) Backup release is enabled or disabled in port units. (Note) Upon a system reset, the pins are set to I/O port input. (Note) When the 32.768-kHz crystal oscillator or the CR oscillator is used, the general-purpose counter is used as a timer.	 (When used for I/O port)  (When P1-0 is used for general-purpose counter)
11	P1-1/SDIO1 /TX1 /SFSY (BRK11)	I/O port 1-1 /serial data input/output 1 /serial transmit data 1 /CD processor function		
12	P1-2/SI1 /SBSY (BRK12)	I/O port 1-2 /serial data input 1 /CD processor function		
13	P1-3/BUZR (BRK13)	I/O port 1-3 /buzzer output		
14	P7-0/SCK2 /RX2 (BRK14)	I/O port 7-0 /serial clock input/output 2 /serial receive data 2		
15	P7-1/SDIO2 /TX2 (BRK15)	I/O port 7-1 /serial data input/output 2 /serial transmit data 2		
16	P7-2/INTR /SI2 (BRK16)	I/O port 7-2 /interrupt input /serial data input 2		

Pin No.	Symbol	Pin Name	Function and Operation	Remarks
8	MV_{DD}	Power supply pins for controller block	Power supply pins for the controller block. Normally, V_{DD} = 3.0 to 3.6 V. When only the CPU operates (when the 75-kHz/32.768-kHz oscillator is used), it can operate at V_{DD} = 1.8 to 3.6 V. In the backup state (when the CKSTP instruction is executed), current dissipation decreases (10 μA or below), allowing the power supply voltage to be reduced to 1.0 V. Raising the voltage on MVDD pin from 0 V to 1.8 V or higher triggers a system reset, causing the program to start from address 0 (power-on reset). (Note) At power-on reset operation, allow 1 ms to 50 ms while the device power supply voltage rises. (Note) The backup current is the total of currents for CV_{DD}, MV_{DD} and DV_{DD}.	
9	MV_{SS}			
17	PDO	CD processor control input/output pin	Output pin for a phase error signal between the EFM and PLCK signals. Drives one of four values: AV_{DD}, Hi-Z, V_{REF}, AV_{SS}	
18	TMAX		TMAX detection result output pin. Longer than specified cycle: Drives a high level (AV_{DD}) Shorter than specified cycle: Drives a low level (AV_{SS}) Within specified cycle: Hi-Z	
19	LPFN		Inverted input pin for PLL low-pass filter amplifier.	
20	LPFO		Output pin for PLL low-pass filter amplifier.	
21	VCOF		VCO filter pin	
22	AV_{SS}		Ground pin for analog block	—

Pin No.	Symbol	Pin Name	Function and Operation	Remarks
23	SLCO	CD processor control input/output pin	DAC output pin for generating data slice level.	
24	RFI		RF signal input pin. The value of Zin1 can be selected using a CD command.	
25	AV_{DD}		Power supply pin for analog block. Normally, V_{DD} = 3.0 to 3.6 V. In CD standby mode, turn this power supply off.	—
26	V_{REF}		Analog reference voltage pin. Normally, a voltage of 1/2 AV_{DD} is supplied (when V_{DD} = 3.3 V, V_{REF} = 1.65 V).	—
27	RFZI		RFRP zero-cross signal input pin	
28	RFRP		RF ripple signal input pin	
29	FEI		Focus error signal input pin	
30	SBAD		Sunbeam addition signal input pin	
31	TEI		Tracking error input pin. The pin is read when tracking servo is turned on.	
32	TEZI		Tracking error/zero-cross signal input pin	
33	FOO		Focus equalizer output pin	
34	TRO		Tracking equalizer output pin	

Pin No.	Symbol	Pin Name	Function and Operation	Remarks
35	RFGC	CD processor control input/output pin	Control signal output pin for adjusting RF amplitude. Drives three-level PWM signal (PWM carrier = 88.2 kHz).	
36	TEBC		Tracking balance control signal output pin. Drives three-level PWM signal (PWM carrier = 88.2 kHz).	
37	SEL		APC circuit ON/OFF signal output pin. When laser is turned on, this pin will be in a high-impedance state.	
38	FMO		Feed equalizer output pin. Drives three-level PWM signal (PWM carrier = 88.2 kHz).	
39	DMO		Disc equalizer output pin. Drives three-level PWM signal (PWM carrier = 88.2 kHz).	
40	CV_{DD}	Power supply pins	Logic power supply pins for the CD processor block and 16.9344-MHz dedicated crystal oscillator. Normally, the same power supply as that for the MV_{DD} and MV_{SS} pins is connected. In CD standby mode, current dissipation decreases.	
43	CV_{SS}			
41	XO	Crystal oscillator pins	Input/output pins for the CD processor-dedicated crystal oscillator. Connect a 16.9344-MHz crystal oscillator. This clock is used as the CD processor system clock and controller system clock. Upon a system reset, this clock is supplied as the controller system clock and starts the CPU. The crystal oscillator can be stopped by program. If the 75/32.768-kHz or CR oscillator is selected as the controller system clock, the CD processor oscillator is stopped by program when the CD processor is turned off. (Note) When switching the controller system clock from the controller oscillator to the CD crystal oscillator, make sure that the CD crystal oscillator is sufficiently stable.	
42	XI			

Pin No.	Symbol	Pin Name	Function and Operation	Remarks
44	DV_{DD}	Audio DAC output	DA converter block power supply pin The TC94A39FAG/FB consumes less current in CD standby mode.	
45	RO		R-channel data forward rotation output pin	
46	DV_{SS}		DA converter block ground pin	
47	LO		L-channel data forward rotation output pin	
48	DVR		Reference voltage pin	

Maximum Ratings (Ta = 25°C, $CV_{DD} = DV_{DD} = AV_{DD} = MV_{DD}$)

Characteristic		Symbol	Rating	Units
Supply voltage		V_{DD}	−0.3 to 4.0	V
Input voltage (Note 1)	CV_{DD} pin	V_{IN1}	−0.3 to CV_{DD} + 0.3	V
	AV_{DD} pin	V_{IN2}	−0.3 to AV_{DD} + 0.3	
	DV_{DD} pin	V_{IN3}	−0.3 to DV_{DD} + 0.3	
	MV_{DD} pin	V_{IN4}	−0.3 to MV_{DD} + 0.3	
		V_{IN5}	−0.3 to 6.0	
Power dissipation	TC94A29FAG	P_D	400	mW
	TC94A29FB		500	
Operating temperature		T_{opr}	−40 to 85	°C
Storage temperature		T_{stg}	−65 to 150	°C

Note 1: V_{IN1}; Pins 41 and 42
V_{IN2}; Pins 17 to 39 (excluding power supply pins)
V_{IN3}; Pins 45, 47 and 48
V_{IN4}; Pins 1 to 13 and 49 to 64 (excluding power supply pins)
V_{IN5}; Pins 14, 15 and 16

Electrical Characteristics

(Ta = 25°C, CV_{DD} = MV_{DD} = DV_{DD} = AV_{DD} = 3.3 V, V_{REF} = 1.65 V unless otherwise stated)

Parameter	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Units
Operating supply voltage range	V_{DD1}	—	CPU and CD in operation MV_{DD} = CV_{DD} ≧ DV_{DD} = AV_{DD} (Note 4)	3.0	~	3.6	V
	V_{DD2}		CPU in operation (CD standby, 16.9344-MHz crystal oscillator/CR oscillator used) (Note 4)	3.0	~	3.6	
	V_{DD3}		Only CPU in operation (CD standby, 75-kHz/32.768-kHz crystal oscillator used) (Note 5)	1.8	~	3.6	
Memory hold voltage range	MV_{HD}	—	Crystal oscillator stopped (CKSTP instruction executed) (Note 4)	1.0	~	3.6	V
Operating power supply current (Note 2)	I_{DD1}	—	CPU and CD in operation (XI = 16.9344-MHz crystal oscillator used)	—	30	50	mA
	I_{DD2}		Only CPU in operation (XI = 16.9344-MHz crystal oscillator used)	—	1.5	—	
	I_{DD3}		CPU in operation (MXI = 75-kHz crystal oscillator connected)	—	50	100	μA
	I_{DD4}		CPU in operation (OSC = 0.5-MHz oscillation)	—	2.0	—	mA
	I_{DD5}		Standby mode (only crystal oscillator in operation, MXI = 75 kHz)	—	40	80	μA
Memory hold current	MI_{HD}	—	(CV_{DD}/MV_{DD}/AV_{DD}/DV_{DD}) Crystal oscillator stopped (CKSTP instruction executed)	—	0.1	10	μA
Oscillation frequency	f_{MXT}	—	(MXI-MXO) Crystal oscillator selected (Note 3) (Note 5)	30	~	100	kHz
	f_{XT}		(XI-XO) (Note 4)	—	16.9344	—	MHz
	f_{OSC}		(OSC) CR oscillator selected	0.01	~	0.75	
Oscillating frequency error	Δf_{OSC}	—	(OSC) CR oscillator selected	—	—	15	%
Crystal oscillator start time	t_{st}	—	(MXI-MXO) Crystal oscillator f_{mxt} = 75 kHz/32.768 kHz	—	—	1.0	s
Crystal oscillator amplifier feedback resistance	R_{fXT1}	—	(XI-XO)	0.5	1.0	2.0	MΩ
	R_{fXT2}		(MXI-MXO)	—	16	—	
Crystal oscillator output resistance	R_{out1}	—	(XO)	0.25	0.5	1.0	kΩ
	R_{out2}		(MXO)	50	100	200	
Dropout voltage detect voltage	V_{DET}	—	(MV_{DD}) Dropout voltage detector enabled	1.4	1.5	1.6	V
Dropout voltage detector operating current	I_{DD}-V_D	—		—	100	—	μA

Note 2: The operating power supply current includes the total current through all CV_{DD}, MV_{DD}, DV_{DD} and AV_{DD} power supply pins.

Note 3: Design and specify constants according to the crystal oscillator to be connected.

Note 4: The values are guaranteed when CV_{DD} = MV_{DD} = DV_{DD} = AV_{DD} = 3.0 to 3.6 V, Ta = –40 to 85°C.

Note 5: The values are guaranteed when CV_{DD} = MV_{DD} = DV_{DD} = AV_{DD} = 1.8 to 3.6 V, Ta = –30 to 75°C.

General-purpose counter (CTin)

Parameter	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Units
Frequency range	f_{CT}	—	V_{IN} = 0.2 V_{P-P} (Note 4)	0.1	—	20	MHz
Input amplitude range	V_{CT}	—	(Note 4)	0.2	—	2.0	V_{P-P}
Operating power supply current	I_{DD-CT}	—	General-purpose counter operating current, f_{in} = 20 MHz	—	0.7	—	mA
Input amplifier feedback resistance	R_{fIN}	—	(CTin)	200	350	1000	kΩ

Note 4: The values are guaranteed when CV_{DD} = MV_{DD} = DV_{DD} = AV_{DD} = 3.0 to 3.6 V, Ta = −40 to 85°C.

LCD common and segment outputs (COM1 to COM4, S1 to S16)

Parameter		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Units
Output current	High level	I_{OH1}	—	V_{OH} = 2.9 V (LCD output)	—	−300	—	μA
	Low level	I_{OL1}		V_{OL} = 0.4 V (LCD output)	—	450	—	
Bias current	1/2 level	V_{BS2}	—	No load (common output, 1/2 bias method)	2.3	2.5	2.7	V
	1/3 level	V_{BS1}		No load (LCD output, 1/3 bias method)	1.47	1.67	1.87	
	2/3 level	V_{BS3}			3.13	3.33	3.53	
LCD operating power supply current		I_{DD}-LCD	—	LCD driver operating current	—	50	—	μA

I/O ports (P1-0 to P6-3, P8-0, P8-1, P7-0 to P7-3)

Parameter		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Units
Output current	High level	I_{OH2}	—	V_{OH} = 2.9 V (P1-0~P6-3, P8-0, P8-1)	−1.0	−2.0	—	mA
	Low level	I_{OL2}		V_{OL} = 0.4 V (P1-0~P6-3, P8-0, P8-1)	1.0	2.0	—	
		I_{OL3}		V_{OL} = 0.4 V (P7-0 to P7-3)	5	15	—	
Input leakage current		I_{LI}	—	V_{IH} = 3.3 V, V_{IL} = 0 V (P1-0 to P6-3, P8-0, P8-1)	—	—	±1.0	μA
				V_{IH} = 5.5 V, V_{IL} = 0 V (P7-0 to P7-3)	—	—	±1.0	
Input voltage	High level	V_{IH}	—	—	V_{DD} × 0.8	~	MV_{DD}	V
	Low level	V_{IL}		—	0	~	MV_{DD} × 0.2	
Input pull-up/down resistance		R_{IN1}	—	(P6-0 to P6-3, P8-0, P8-1) Pull-down/up specified	25	50	120	kΩ
		R_{IN2}		(P3-0) Test input pulled down	—	10	—	

AD converter (ADin1 to ADin4)

Parameter	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Units
Analog input voltage range	V_{AD}	—	ADin1 to ADin4	0	~	MV_{DD}	V
Resolution	V_{RES}	—	—	—	6	—	bit
Total conversion error	—	—	MV_{DD} = 1.8~3.6V, Ta = −30~75°C (Note 6)	—	—	±2.0	LSB
			MV_{DD} = 2.0~3.6V, Ta = −40~85°C (Note 6)	—	—	±1.0	
Analog input leakage current	I_{LI}	—	V_{IH} = 3.3 V, V_{IL} = 0 V (ADin1 to ADin4)	—	—	±1.0	μA

Note 6: The values are guaranteed when CV_{DD} = DV_{DD} = AV_{DD} = 3.0 to 3.6 V.

PDO, TMAX, RFGC, TEBC, FMO, DMO, TRO, FOO, and SEL output

Parameter		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Units
Output current	High level	I_{OH6}	—	V_{OH} = 2.9 V (SEL, TMAX)	−2.0	—	—	mA
	Low level	I_{OL4}		V_{OL} = 0.4 V (SEL, TMAX)	2.0	—	—	
Output resistance		R_{out3}	—	(RFGC, TEBC, FMO, DMO, TRO, FOO)	—	3.0	—	kΩ
		R_{out4}		(PDO)	—	5.0	—	
V_{REF} output ON resistance		R_{on}	—	(RFGC, TEBC, FMO, DMO, PDO)	—	—	500	Ω

Transfer delay time (BCK, LRCK, AOUT, DOUT, IPF, SBOK, CLCK, DATA, SFSY, SBSY)

Parameter		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Units
Transfer delay time	High level	t_{pLH}	—	—	—	10	—	ns
	Low level	t_{pHL}		—	—	10	—	

CD processor AD conversion block (FEI, TEI, RFRP, SBAD)

Parameter	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Units
Resolution	—	—	(FEI, TEI, RFRP, SBAD)	—	8	—	bit
Sampling frequency	—	—	(FEI, TEI, RFRP)	—	176.4	—	kHz
			(SBAD)	—	88.2	—	
Conversion input range	—	—	AV_{DD} = 3.3 V (FEI, TEI, RFRP, SBAD)	0.15 × AV_{DD}	—	0.85 × AV_{DD}	V

CD processor DA conversion block (focus tracking system)

Parameter	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Units
Number of bits	—	—	(FOO, TRO)	—	5	—	bit
Sampling frequency	—	—	(FOO, TRO)	—	2.8	—	MHz
Conversion output range	—	—	AV_{DD} = 3.3 V (FOO, TRO)	AV_{SS}	—	AV_{DD}	V

CD processor PLL/VCO block

Parameter	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Units
Input/output signal range	—	—	(LPFN, LPFO)	AV_{SS}	—	AV_{DD}	V
Frequency characteristic	—	—	(LPFN-LPFO) −3dB point (Gain = 1)	—	8	—	MHz
Oscillation center frequency	—	—	LPFO = V_{REF}	—	34	—	MHz
Frequency variable range	—	—	[VCOGSL] bit = Low	−30	—	+30	%
			[VCOGSL] bit = High	−40	—	+40	

CD processor comparator (TEZI, RFZI)

Parameter	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Units
Input range	—	—	(TEZI, RFZI)	AV_{SS}	—	AV_{DD}	V
Hysteresis voltage	—	—	(TEZI, RFZI) V_{REF} reference	−50	—	+50	mV
Input resistance	Z_{in2}	—	(TEZI, RFZI)	—	10	—	kΩ

CD processor data slicer (RFI/SLCO)

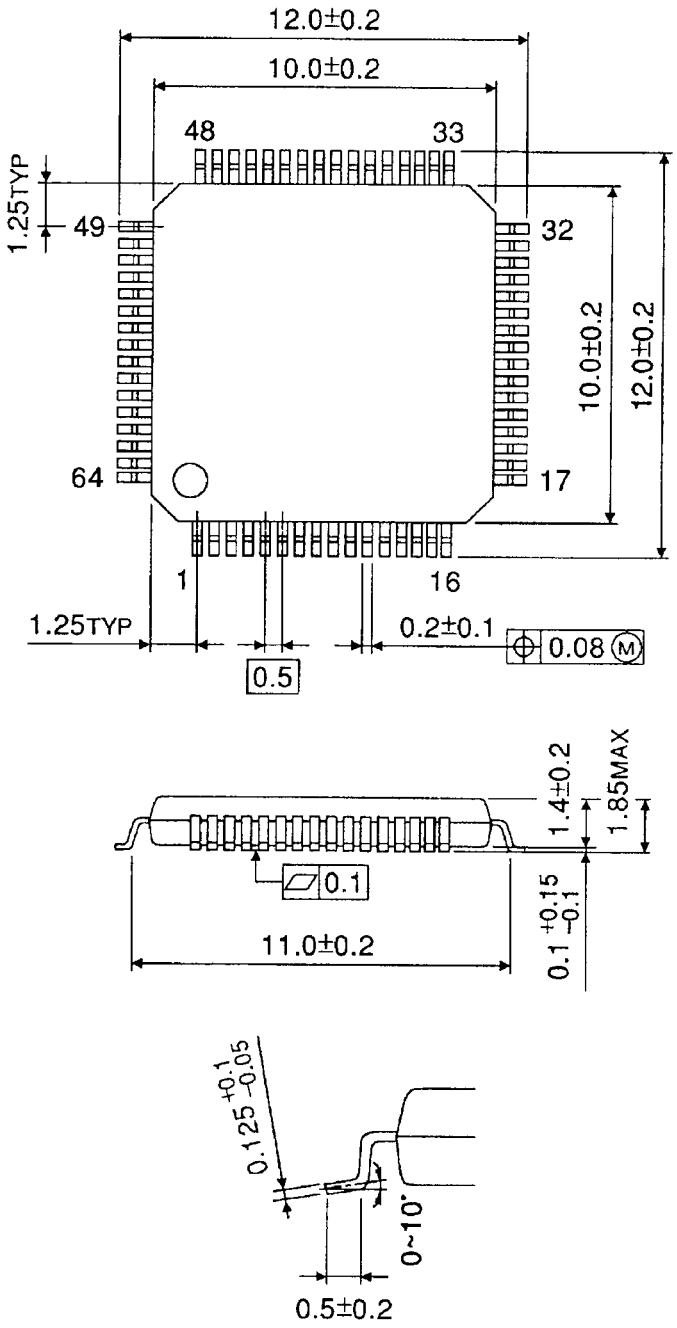
Parameter	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Units
Input amplitude	—	—	(RFI) V_{REF} reference	0.6	1.2	2.0	V_{P-P}
Input resistance	Z_{in1}	—	(RFI) Set resistance by CD command	—	20	—	kΩ
				—	10	—	
DAC resolution	—	—	(SLCO) R-2R DAC	—	6	—	bit
DAC output conversion range	—	—	(SLCO) R-2R DAC	0.75 × V_{REF}	—	1.25 × V_{REF}	V
DAC output impedance	—	—	(SLCO) R-2R DAC	—	2.5	—	kΩ

1-bit DA converter

Parameter	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Units
Total harmony distortion	THD + N	—	1-kHz sine wave, full-scale input	—	−85	−77	dB
S/N ratio	S/N (1)	—	Internal Zero detect = OFF	85	91	—	dB
	S/N (2)		Internal Zero detect = ON	95	100	—	
Dynamic range	DR	—	1-kHz sine wave, input reduction of −60dB	83	90	—	dB
Crosstalk	CT	—	1-kHz sine wave, full-scale input	—	−90	−83	dB
Analog output level	DACout	—	1-kHz sine wave, full-scale input	790	825	860	mVrms

Package Dimensions

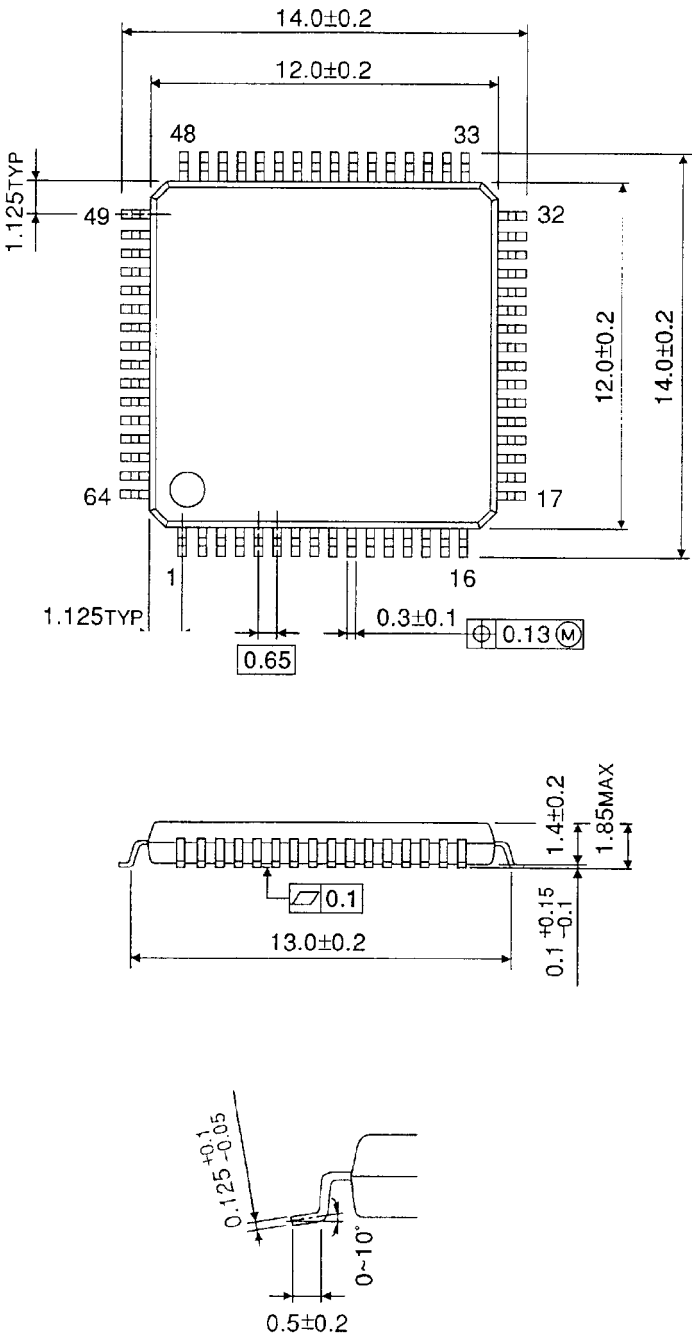
LQFP64-P-1010-0.50 Unit : mm



Weight: 0.32 g (typ.)

Package Dimensions

QFP64-P-1212-0.65 Unit : mm



Weight: 0.45 g (typ.)

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