Low Voltage / Low Power CMOS 16-Bit Microcontrollers

TMP93CS40F / TMP93CS41F
TMP93CS40DF / TMP93CS41DF

1. OUTLINE AND DEVICE CHARACTERISTICS

The TMP93CS40/S41 are high-speed advanced 16-bit microcontrollers developed for controlling medium-to large-scale equipment. The TMP93CS41 does not have a ROM; the TMP93CS40 has a built-in ROM. Otherwise, the devices function in the same way.

The TMP93CS40/S41F are housed in a 100-pin flat package.

The device characteristics are as follows:

(1) Original 16-bit CPU (900/L CPU)
- TLCS-90 instruction mnemonic upward-compatible
- 16-Mbyte linear address space
- General-purpose registers, register bank system
- 16-bit multiplication / division and bit transfer / arithmetic instructions
- Micro DMA : 4 channels (1.6 μs / 2 bytes at 20 MHz)

(2) Minimum instruction execution time : 200 ns at 20 MHz

(3) Internal RAM : 2 Kbyte

Internal ROM :

TMP93CS40	64-Kbyte ROM
TMP93CS41	None

(4) External memory expansion
- Can be expanded to up to16M bytes (for both programs and data).
- AM8 / $\overline{16}$ pin (selects the external data bus width)
- Can mix 8- and 16-bit external data buses.
  ··· Dynamic bus sizing

(5) 8-bit timer : 2 channels

(6) 8-bit PWM timer : 2 channels

(7) 16-bit timer : 2 channels

(8) Pattern generator : 2 channels

(9) 4-bit serial interface : 2 channels

(10) 10-bit A/D converter : 8 channels

(11) Watchdog timer

(12) Chip select / wait controller : 3 blocks

(13) Interrupt functions : 29
- 9 CPU interrupts ····· SWI instruction, and Illegal instruction
- 14 internal interrupts
- 6 external interrupts

7-level priority can be set.

(14) I/O ports
79 pins for TMP93CS40 and 61 pins for TMP93CS41

(15) Standby function : 4 Halt modes (Run, Idle2, Idle1, Stop)

(16) Clock gear function
- Dual clock operation
- Clock gear: High-frequency clock can be varied from fc to fc / 16.

(17) Wide Operating Voltage

- Vcc = 2.7 to 5.5 V

(18) Package

Type No.	Package
TMP93CS40F TMP93CS41F	QFP100-P-1414-0.50
TMP93CS40DF TMP93CS41DF	QFP100-P-1414-0.50C

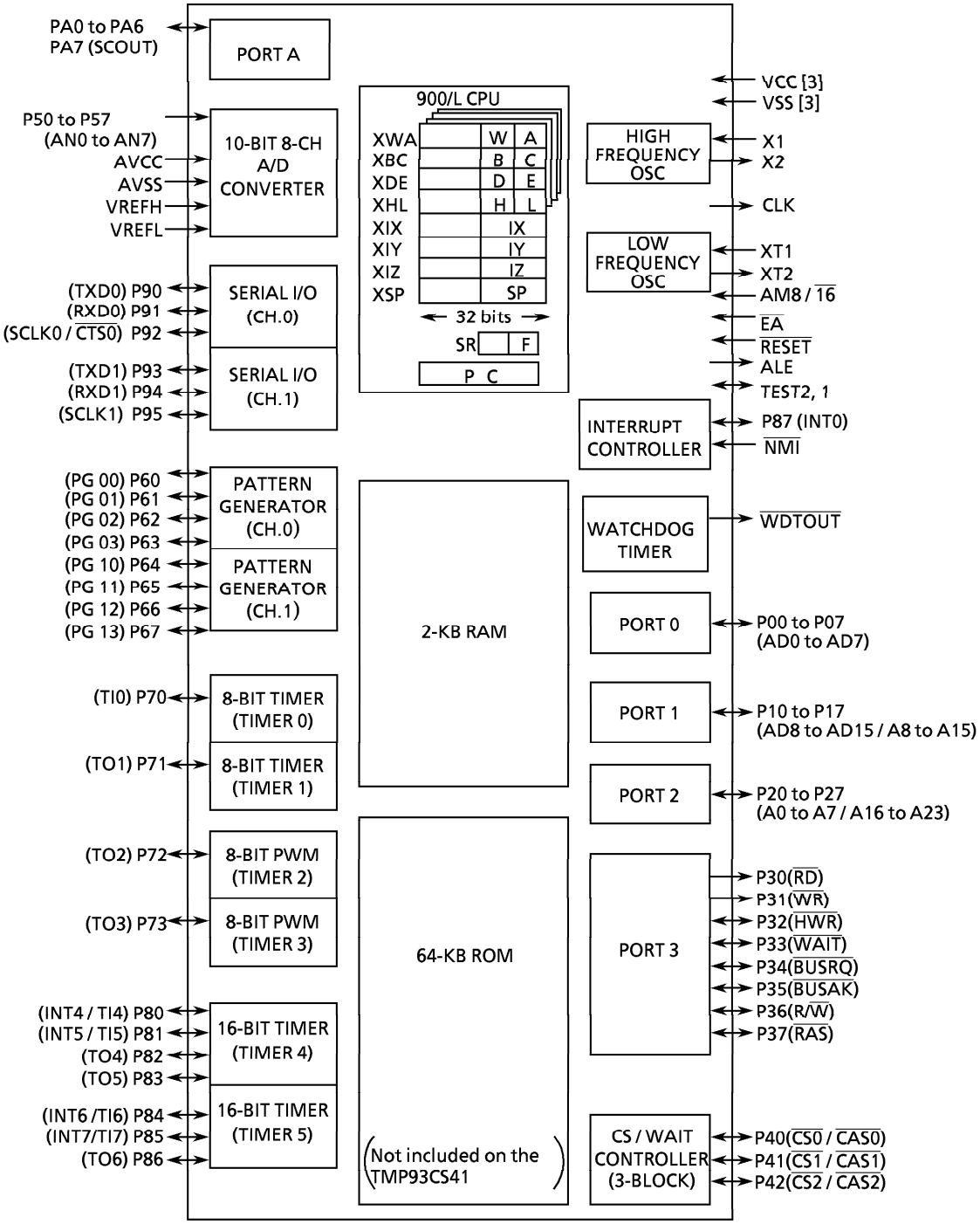


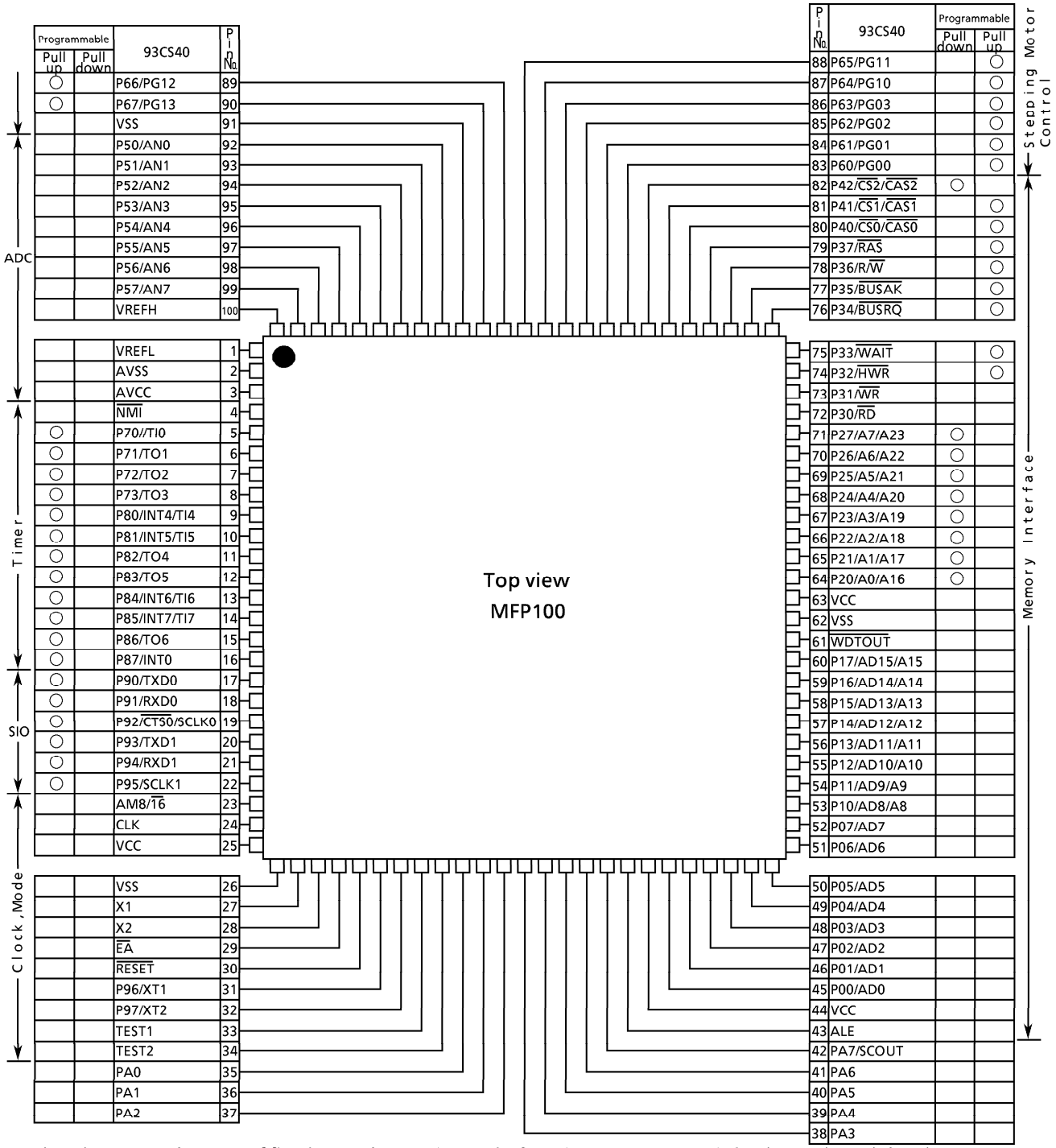
Figure 1 TMP93CS40/TMP93CS41 Block Diagram

2. PIN ASSIGNMENT AND FUNCTIONS

The assignment of input / output pins on the TMP93CS40/TMP93CS41, their names and outline functions are described below.

2.1 Pin Assignment

Figure 2.1 shows the pin assignment for the TMP93CS40F/S41F and TMP93CS40DF/S41DF.



(Note) Because the TMP93CS41 does not have an internal ROM, pins P00 to P17 are tied to AD0 to AD15 (when AM8 / $\overline{16}$ = 0), or to AD0 to AD7 and A8 to A15 (when AM8 / $\overline{16}$ = 1). P30 is tied to $\overline{RD}$, P31 to $\overline{WR}$.

Figure 2.1 Pin Assignment (100-pin MFP)

2.2 Pin Names and Functions

The names of the input / output pins and their functions are described below.

Table 2.2 Pin Names and Functions

Pin Name	Number of Pins	I/O	Function
P00 to P07 AD0 to AD7	8	I/O Tri-State	Port 0: I/O port that allows at the bit level Address/data (lower): Bits 0 to 7 of address/data bus
P10 to P17 AD8 to AD15 A8 to A15	8	I/O Tri-State Output	Port 1: I/O port that allows at the bit level Address data (upper): Bits 8 to 15 of address/data bus Address: Bits 8 to 15 of address bus
P20 to P27 A0 to A7 A16 to A23	8	I/O Output Output	Port 2: I/O port that allows selection of I/O at the bit level (with pull-down resistor) Address: bits 0 to 7 of address bus Address: bits 16 to 23 of address bus
P30 $\overline{RD}$	1	Output Output	Port 30: Output port Read: Strobe signal for reading external memory
P31 $\overline{WR}$	1	Output Output	Port 31: Output port Write: Strobe signal for writing data on pins AD0 to AD7
P32 $\overline{HWR}$	1	I/O Output	Port 32: I/O port (with pull-up resistor) High write: Strobe signal for writing data on pins AD8 to AD15
P33 $\overline{WAIT}$	1	I/O Input	Port 33: I/O port (with pull-up resistor) Wait: Pin used to request CPU bus wait
P34 $\overline{BUSRQ}$	1	I/O Input	Port 34: I/O port (with pull-up resistor) Bus request: Signal used to request bus release
P35 $\overline{BUSAK}$	1	I/O Output	Port 35: I/O port (with pull-up resistor) Bus acknowledge: Signal used to acknowledge bus release
P36 R/$\overline{W}$	1	I/O Output	Port 36: I/O port (with pull-up resistor) Read/write: 1 represents read or dummy cycle; 0 represents write cycle.
P37 $\overline{RAS}$	1	I/O Output	Port 37: I/O port (with pull-up resistor) Row address strobe: Outputs $\overline{RAS}$ strobe for DRAM.
P40 $\overline{CS0}$ $\overline{CAS0}$	1	I/O Output Output	Port 40: I/O port (with pull-up resistor) Chip select 0: Outputs 0 when address is within specified address area. Column address strobe 0: Outputs $\overline{CAS}$ strobe for DRAM when address is within specified address area.

Note : This device's built-in memory or built-in I/O cannot be accessed by an external DMA controller using the $\overline{BUSRQ}$ and $\overline{BUSAK}$ signals.

Pin Name	Number of Pins	I/O	Function
P41 $\overline{CS1}$ $\overline{CAS1}$	1	I/O Output Output	Port 41: I/O port (with pull-up resistor) Chip select 1: Outputs 0 if address is within specified address area. Column address strobe 1: Outputs $\overline{CAS}$ strobe for DRAM if address is within specified address area.
P42 $\overline{CS2}$ $\overline{CAS2}$	1	I/O Output Output	Port 42: I/O port (with pull-down resistor) Chip select 2: Outputs 0 if address is within specified address area. Column address strobe 2: Outputs $\overline{CAS}$ strobe for DRAM if address is within specified address area.
P50 to P57 AN0 to AN7	8	Input Input	Port 5: Input port Analog input: Analog signal input for A/D converter
VREFH	1	Input	Pin for high level reference voltage input to A/D converter
VREFL	1	Input	Pin for low level reference voltage input to A/D converter
P60 to P63 PG00 to PG03	4	I/O Output	Ports 60 - 63: I/O ports that allow selection of I/O at the bit level (with pull-up resistor) Pattern generator ports: 00 to 03
P64 to P67 PG10 to PG13	4	I/O Output	Ports 64 - 67: I/O ports that allow selection of I/O on a bit basis (with pull-up resistor) Pattern generator ports: 10 to 13
P70 TI0	1	I/O Input	Port 70: I/O port (with pull-up resistor) Timer input 0: Timer 0 input
P71 TO1	1	I/O Output	Port 71: I/O port (with pull-up resistor) Timer output 1: Timer 0 or timer 1 output
P72 TO2	1	I/O Output	Port 72: I/O port (with pull-up resistor) PWM output 2: 8-bit PWM timer 2 output
P73 TO3	1	I/O Output	Port 73: I/O port (with pull-up resistor) PWM output 3: 8-bit PWM timer 3 output
P80 TI4 INT4	1	I/O Input Input	Port 80: I/O port (with pull-up resistor) Timer input 4: Timer 4 count / capture trigger signal input Interrupt request pin 4: Interrupt request pin with programmable rising / falling edge
P81 TI5 INT5	1	I/O Input Input	Port 81: I/O port (with pull-up resistor) Timer input 5: Timer 5 count / capture trigger signal input Interrupt request pin 5: Interrupt request pin with rising edge
P82 TO4	1	I/O Output	Port 82: I/O port (with pull-up resistor) Timer output 4: Timer 4 output pin
P83 TO5	1	I/O Output	Port 83: I/O port (with pull-up resistor) Timer output 5: Timer 4 output pin

Pin Name	Number of Pins	I/O	Function
P84 TI6 INT6	1	I/O Input Input	Port 84: I/O port (with pull-up resistor) Timer input 6: Timer 5 count / capture trigger signal input Interrupt request pin 6: Interrupt request pin with programmable rising / falling edge
P85 TI7 INT7	1	I/O Input Input	Port 85: I/O port (with pull-up resistor) Timer input 7: Timer 5 count / capture trigger signal input Interrupt request pin 7: Interrupt request pin with rising edge
P86 TO6	1	I/O Output	Port 86: I/O port (with pull-up resistor) Timer output 6: Timer 5 output pin
P87 INT0	1	I/O Input	Port 87: I/O port (with pull-up resistor) Interrupt request pin 0: Interrupt request pin with programmable level / rising edge
P90 TXD0	1	I/O Output	Port 90: I/O port (with pull-up resistor) Serial data send 0
P91 RXD0	1	I/O Input	Port 91: I/O port (with pull-up resistor) Serial data receive 0
P92 $\overline{CTS0}$ SCLK0	1	I/O Input I/O	Port 92: I/O port (with pull-up resistor) Serial data send enable 0 (Clear to Send) Serial Clock I/O 0
P93 TXD1	1	I/O Output	Port 93: I/O port (with pull-up resistor) Serial data send 1
P94 RXD1	1	I/O Input	Port 94: I/O port (with pull-up resistor) Serial data receive 1
P95 SCLK1	1	I/O I/O	Port 95: I/O port (with pull-up resistor) Serial clock I/O 1
PA0 to PA6	7	I/O	Ports A0 to A6: I/O ports
PA7 SCOUT	1	I/O Output	Port A7: I/O port System Clock Output: Outputs f_{FPH} or f_{SYS} clock.
$\overline{WDTOUT}$	1	Output	Watchdog timer output pin
$\overline{NMI}$	1	Input	Non-maskable interrupt request pin: Interrupt request pin with programmable falling edge or with both edges programmable.
CLK	1	Output	Clock output: Outputs 「$f_{SYS} \div 2$」 clock. Pulled-up during reset. Can be disabled to reduce noise.
$\overline{EA}$	1	Input	External access: On the TMP93CS41, the Vss pin should be connected. On the TMP93CS40, the Vcc pin should be connected.

Pin Name	Number of Pins	I/O	Function
AM8 / $\overline{16}$	1	Input	Address Mode: Selects external Data Bus width. (On the TMP93CS40) The Vcc pin should be connected. The Data Bus Width for external access is set by the Chip Select / WAIT Control register, Port 1 Control register. (On the TMP93CS41) The Vss pin should be connected to access either fixed 16-bit Bus width, or 16-bit Bus interchangeable with 8-bit Bus. The Vcc pin should be connected to access a fixed 8-bit Bus Width.
ALE	1	Output	Address Latch Enable (Can be disabled to reduce noise.)
$\overline{\text{RESET}}$	1	Input	Reset: Initializes TMP93CS40/TMP93CS41. (with pull-up resistor)
X1/X2	2	I/O	High Frequency Oscillator connecting pin
P96 XT1	1	I/O Input	Port 96: I/O port (open drain output) Low Frequency Oscillator connecting pin
P97 XT2	1	I/O Output	Port 97: I/O port (open drain output) Low Frequency Oscillator connecting pin
TEST1 / TEST2	2	Output / Input	TEST1: should be connected to TEST2 pin.
VCC	3		Power supply pin (All V_{CC} pins should be connected to the power supply pin.)
VSS	3		GND pin (0 V) (All V_{SS} pins should be connected to GND (0V).)
AVCC	1		Power supply pin for A/D converter
AVSS	1		GND pin for A/D converter (0 V)

Note : All pins that have built-in pull-up/down resistors (other than the $\overline{\text{RESET}}$ pin) can be disconnected from the built-in pull-up/down resistor by software.

3. Operation

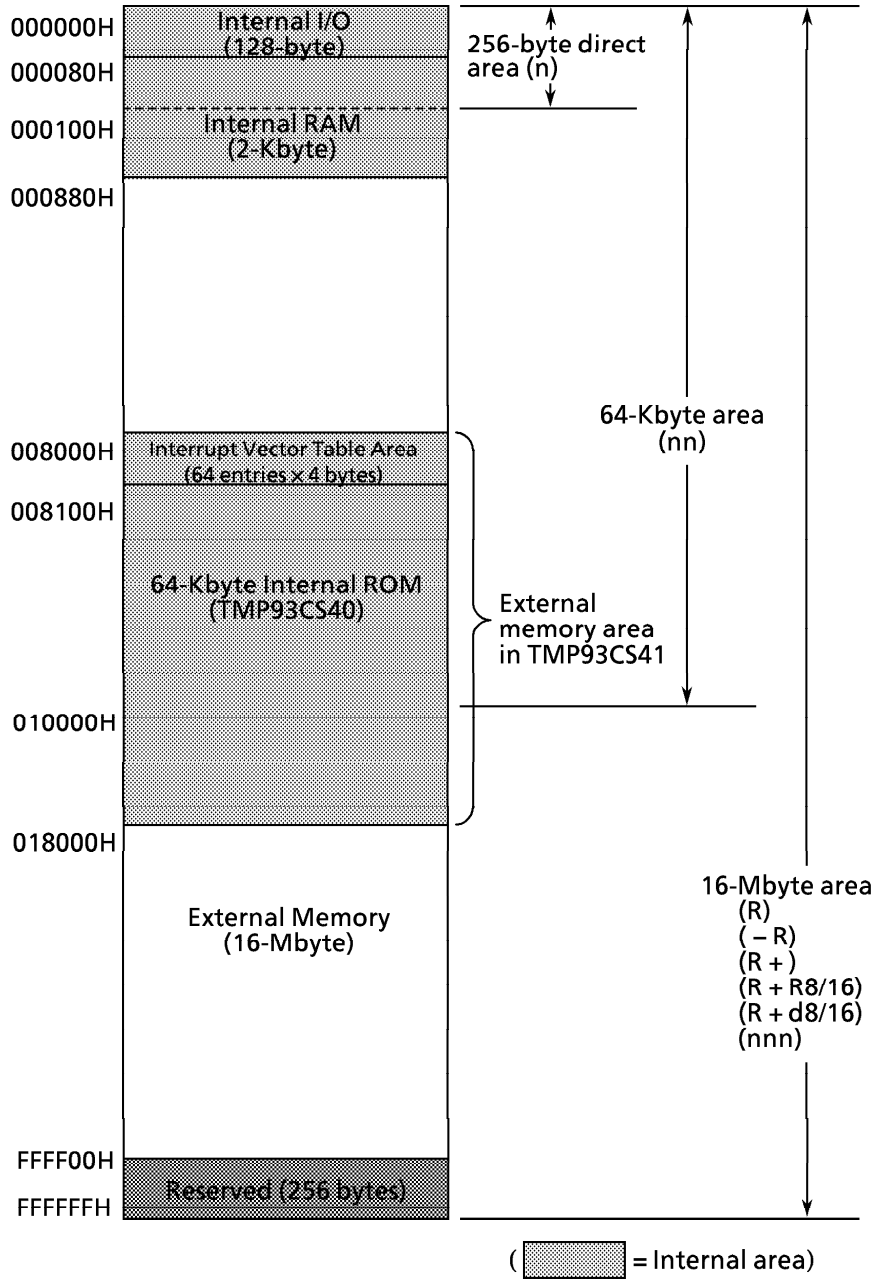
This section describes the functions and basic operation of all blocks of the TMP93CS40/S41 devices.

3.1 CPU

The TMP93CS40/S41 devices have a built-in high-performance 16-bit CPU (900/L CPU). (For a description of this CPU's operation, see the sub-section TLCS-900/L CPU in the previous section.

3.2 Memory Map

Figure 3.2 is a memory map of the TMP93CS40 / S41.



Note: The 256-byte area from FFFF00H to FFFFFFH cannot be used.

Figure 3.2 Memory Map

4. ELECTRICAL CHARACTERISTICS

"X" used in an expression shows a frequency for the clock f_{FPH} selected by SYSCR1<SYSCK>. The value of X changes according to whether a clock gear or a low speed oscillator is selected. An example value is calculated for fc, with gear = 1/fc (SYSCR1<SYSCK, GEAR 2 to 0> = 0000).

4.1 Absolute Maximum Ratings

(TMP93CS40F, TMP93CS41F
TMP93CS40DF, TMP93CS41DF)

Symbol	Parameter	Rating	Unit
V cc	Power Supply Voltage	– 0.5 to 6.5	V
V IN	Input Voltage	– 0.5 to Vcc + 0.5	V
Σ IOL	Output Current (total)	120	mA
Σ IOH	Output Current (total)	– 80	mA
P D	Power Dissipation (Ta = 85℃)	600	mW
T SOLDER	Soldering Temperature (10 s)	260	℃
T STG	Storage Temperature	– 65 to 150	℃
T OPR	Operating Temperature	– 40 to 85	℃

4.2 DC Characteristics (1/2)

Ta = – 40 to 85 °C

Symbol	Parameter		Min.	Typ (Note 1)	Max.	Unit	Condition
V cc	Power Supply Voltage (AVCC = VCC, AVCC = VSS = 0V)		4.5		5.5	V	fc = 4 to 20 MHz, fs = 30 to 34 kHz
			2.7				fc = 4 to 12.5 MHz, fs = 30 to 34 kHz
V_{IL}	Input Low Voltage	AD0 to 15	– 0.3		0.8	V	$V_{CC} \geqq 4.5$ V
					0.6		$V_{CC} < 4.5$ V
V_{IL1}		Port 2 to A (except P87, P5)			0.3 Vcc		V_{CC} = 2.7 to 5.5 V
V_{IL2}		RESET, NMI, INT0			0.25 Vcc		
V_{IL3}		EA, AM8/16			0.3		
V_{IL4}		X1, P5			0.2 Vcc		
V_{IH}	Input High Voltage	AD0 to 15	2.2		Vcc + 0.3		$V_{CC} \geqq 4.5$ V
			2.0				$V_{CC} < 4.5$ V
V_{IH1}		Port 2 to A (except P87)	0.7Vcc				V_{CC} = 2.7 to 5.5 V
V_{IH2}		RESET, NMI, INT0	0.75Vcc				
V_{IH3}		EA, AM8/16	Vcc – 0.3				
V_{IH4}		X1	0.8Vcc				
V_{OL}	Output Low Voltage				0.45	V	I OL = 1.6 mA (V_{CC} = 2.7 to 5.5 V)
V_{OH1}	Output High Voltage		2.4				I OH = – 400 μA (V_{CC} = 3 V ± 10 %)
V_{OH2}			4.2				I OH = – 400 μA (V_{CC} = 5 V ± 10 %)

(Note 1) Typical values are for Ta = 25 °C and V_{CC} = 5 V unless otherwise noted.

4.2 DC Characteristics (2/2)

Symbol	Parameter	Min.	Typ. (Note 1)	Max.	Unit	Condition
I DAR (Note 2)	Darlington Drive Current (8 Output Pins Max)	− 1.0		− 3.5	mA	V EXT = 1.5 V R EXT = 1.1 kΩ (when Vcc = 5 V ± 10 %)
I LI	Input Leakage Current		0.02	± 5	μA	0.0 ≦ V_{IN} ≦ V_{CC}
I LO	Output Leakage Current		0.05	± 10		0.2 ≦ V_{IN} ≦ V_{CC} − 0.2
V STOP	Powerdown Voltage (at Stop, RAM Back-up)	2.0		6.0	V	V IL2 = 0.2Vcc, V IH2 = 0.8Vcc
R RST	$\overline{\text{RESET}}$ Pull-up Resistor	50		150	kΩ	Vcc = 5 V ± 10 %
		80		200		Vcc = 3 V ± 10 %
C IO	Pin Capacitance			10	pF	fc = 1 MHz
V TH	Schmitt Width $\overline{\text{RESET}}$, NMI, INT0	0.4	1.0		V	
RKL	Programmable Pull-down Resistor	10		80	kΩ	Vcc = 5 V ± 10 %
		30		150		Vcc = 3 V ± 10 %
RKH	Programmable Pull-up Resistor	50		150		Vcc = 5 V ± 10 %
		100		300		Vcc = 3 V ± 10 %
I cc	Normal (Note 3)		19	25	mA	Vcc = 5 V ± 10 % fc = 20 MHz
	Normal2 (Note 4)		24	30		
	Run		17	25		
	Idle2		10	15		
	Idle1		3.5	5		
	Normal (Note 3)		6.5	10	mA	Vcc = 3 V ± 10 % fc = 10 MHz (Typ: Vcc = 3.0 V)
	Normal2 (Note 4)		9.5	13		
	Run		5.0	9		
	Idle2		3.0	5		
	Idle1		0.8	1.5		
	Slow (Note 3)		20	35	μA	Vcc = 3 V ± 10 % fs = 32.768 kHz (Typ: Vcc = 3.0 V)
	Run		16	30		
	Idle2		10	20		
	Idle1		5	15		
	Stop		0.2	10	μA	Vcc = 2.7 to5.5 V

Note 1: Typical values are for Ta = 25 °C and V_{CC} = 5 V unless otherwise noted.
Note 2: I-DAR is guaranteed for up to eight ports.
Note 3: I_{CC} measurement conditions (Normal, Slow):
Only CPU is operational; output pins are open and input pins are fixed.
Note 4: I_{CC} measurement conditions (Normal2):
All functions are operational; output pins are open and input pins are fixed.

4.3 AC Characteristics

(1) Vcc = 5 V ± 10 %

No.	Symbol	Parameter	Variable		16 MHz		20 MHz		Unit
			Min	Max	Min	Max	Min	Max	
1	t_{OSC}	Osc. Period (= x)	50	31250	62.5		50		ns
2	t_{CLK}	CLK Width	2x – 40		85		60		ns
3	t_{AK}	A0 to A23 Valid→ CLK Hold	0.5x – 20		11		5		ns
4	t_{KA}	CLK Valid→ A0 to A23 Hold	1.5x – 70		24		5		ns
5	t_{AL}	A0 to A15 Valid→ ALE Fall	0.5x – 15		16		10		ns
6	t_{LA}	ALE Fall→ A0 to A15 Hold	0.5x – 20		11		5		ns
7	t_{LL}	ALE High Width	x – 40		23		10		ns
8	t_{LC}	ALE Fall→ $\overline{RD}/\overline{WR}$ Fall	0.5x – 25		6		0		ns
9	t_{CL}	$\overline{RD}/\overline{WR}$ Rise→ ALE Rise	0.5x – 20		11		5		ns
10	t_{ACL}	A0 to A15 Valid→ $\overline{RD}/\overline{WR}$ Fall	x – 25		38		25		ns
11	t_{ACH}	A0 to A23 Valid→ $\overline{RD}/\overline{WR}$ Fall	1.5x – 50		44		25		ns
12	t_{CA}	$\overline{RD}/\overline{WR}$ Rise→ A0 to A23 Hold	0.5x – 25		6		0		ns
13	t_{ADL}	A0 to A15 Valid→ D0 to D15 Input		3.0x – 55		133		95	ns
14	t_{ADH}	A0 to A23 Valid→ D0 to D15 Input		3.5x – 65		154		110	ns
15	t_{RD}	$\overline{RD}$Fall →D0 to D15 Input		2.0x – 60		65		40	ns
16	t_{RR}	$\overline{RD}$ Low Pulse Width	2.0x – 40		85		60		ns
17	t_{HR}	$\overline{RD}$Rise→ D0 to D15 Hold	0		0		0		ns
18	t_{RAE}	$\overline{RD}$Rise→ A0 to A15 Output	x – 15		48		35		ns
19	t_{WW}	$\overline{WR}$ Low Pulse Width	2.0x – 40		85		60		ns
20	t_{DW}	D0 to D15 Valid→ $\overline{WR}$ Rise	2.0x – 55		70		45		ns
21	t_{WD}	$\overline{WR}$ Rise →D0 to D15 Hold	0.5x – 15		16		10		ns
22	t_{AWH}	A0 to A23 Valid→ $\overline{WAIT}$ Input (1 WAIT + n mode)		3.5x – 90		129		85	ns
23	t_{AWL}	A0 to A15 Valid→ $\overline{WAIT}$ Input (1 WAIT + n mode)		3.0x – 80		108		70	ns
24	t_{CW}	$\overline{RD}/\overline{WR}$ Fall→$\overline{WAIT}$ Hold (1 WAIT + n mode)	2.0x + 0		125		100		ns
25	t_{APH}	A0 to A23 Valid→ PORT Input		2.5x – 120		36		5	ns
26	t_{APH2}	A0 to A23 Valid→ PORT Hold	2.5x + 50		206		175		ns
27	t_{CP}	$\overline{WR}$ Rise→ PORT Valid		200		200		200	ns
28	t_{ASRH}	A0 to A23 Valid→ $\overline{RAS}$ Fall	1.0x – 40		23		10		ns
29	t_{ASRL}	A0 to A15 Valid→ $\overline{RAS}$ Fall	0.5x – 15		16		10		ns
30	t_{RAC}	$\overline{RAS}$ Fall→ D0 to D15 Input		2.5x – 70		86		55	ns
31	t_{RAH}	$\overline{RAS}$ Fall→ A0 to A15 Hold	0.5x – 15		16		10		ns
32	t_{RAS}	$\overline{RAS}$ Low Pulse Width	2.0x – 40		85		60		ns
33	t_{RP}	$\overline{RAS}$ High Pulse Width	2.0x – 40		85		60		ns
34	t_{RSH}	$\overline{CAS}$ Fall→ $\overline{RAS}$ Rise	1.0x – 40		23		10		ns
35	t_{RSC}	$\overline{RAS}$ Rise→ $\overline{CAS}$ Rise	0.5x – 25		6		0		ns
36	t_{RCD}	$\overline{RAS}$ Fall→ $\overline{CAS}$ Fall	1.0x – 40		23		10		ns
37	t_{CAC}	$\overline{CAS}$ Fall→ D0 to D15 Input		1.5x – 65		29		10	ns
38	t_{CAS}	$\overline{CAS}$ Low Pulse Width	1.5x – 30		64		40		ns

AC Measuring Conditions

- Output Level : High 2.2 V / Low 0.8 V , CL = 50 pF
  (However, CL = 100 pF for AD0 to AD15, A0 to A23, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{HWR}$, R/$\overline{W}$, CLK, $\overline{RAS}$, $\overline{CAS0}$ to $\overline{CAS2}$)
- Input Level : High 2.4 V / Low 0.45 V (AD0 to AD15)
  High 0.8 Vcc / Low 0.2 Vcc(except for AD0 to AD15)

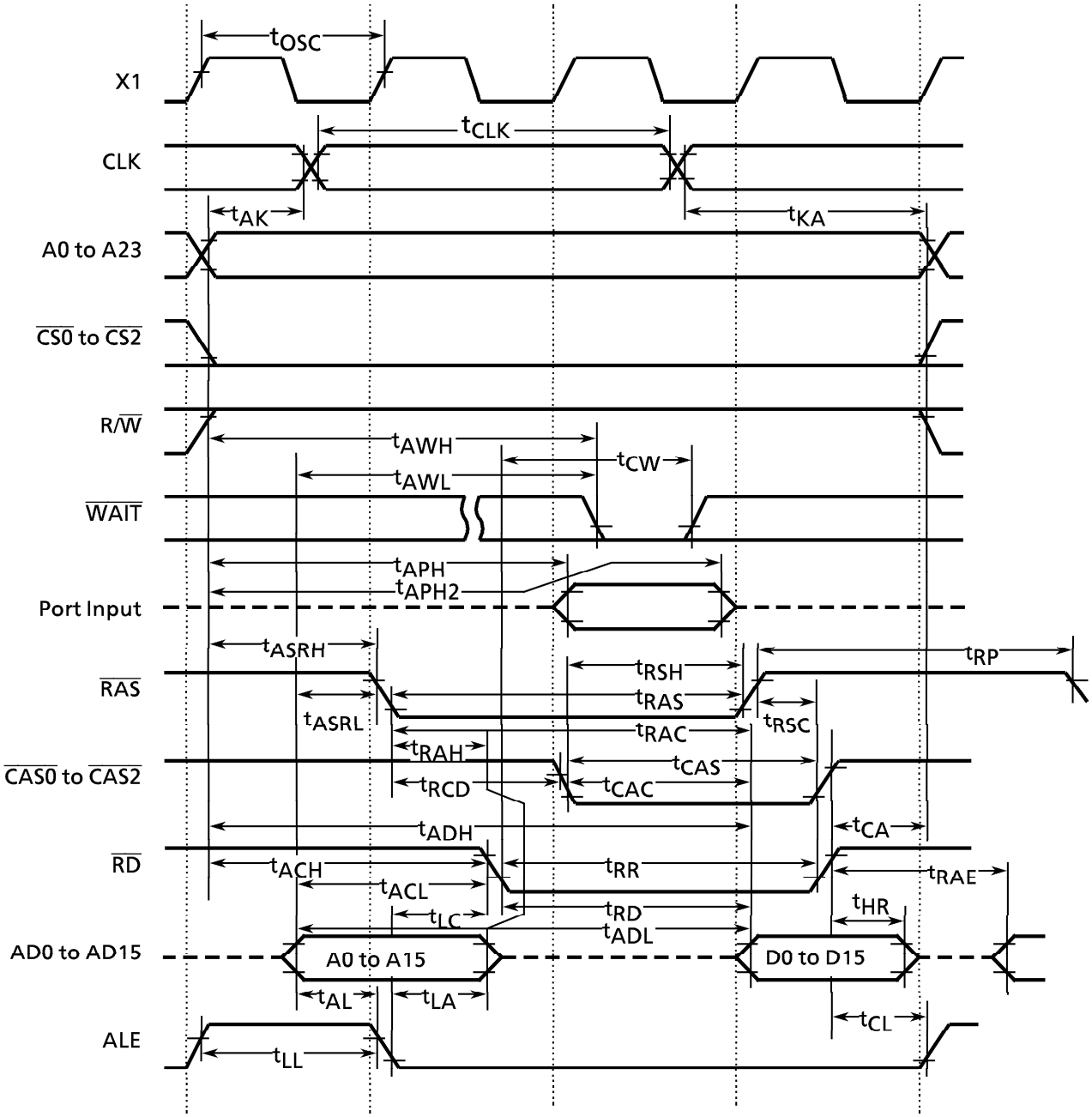
(2) Vcc = 3 V ± 10 %

No.	Symbol	Parameter	Variable		12.5 MHz		Unit
			Min	Max	Min	Max	
1	t_{OSC}	Osc. Period (= x)	80	31250	80		ns
2	t_{CLK}	CLK Width	2x – 40		120		ns
3	t_{AK}	A0 to A23 Valid→ CLK Hold	0.5x – 30		10		ns
4	t_{KA}	CLK Valid→ A0 to A23 Hold	1.5x – 80		40		ns
5	t_{AL}	A0 to A15 Valid→ ALE Fall	0.5x – 35		5		ns
6	t_{LA}	ALE Fall→ A0 to A15 Hold	0.5x – 35		5		ns
7	t_{LL}	ALE High Width	x – 60		20		ns
8	t_{LC}	ALE Fall→ $\overline{RD}/\overline{WR}$ Fall	0.5x – 35		5		ns
9	t_{CL}	$\overline{RD}/\overline{WR}$ Rise→ ALE Rise	0.5x – 40		0		ns
10	t_{ACL}	A0 to A15 Valid→ $\overline{RD}/\overline{WR}$ Fall	x – 50		30		ns
11	t_{ACH}	A0 to A23 Valid→ $\overline{RD}/\overline{WR}$ Fall	1.5x – 50		70		ns
12	t_{CA}	$\overline{RD}/\overline{WR}$ Rise→ A0 to A23 Hold	0.5x – 40		0		ns
13	t_{ADL}	A0 to A15 Valid→ D0 to D15 Input		3.0x – 110		130	ns
14	t_{ADH}	A0 to A23 Valid→ D0 to D15 Input		3.5x – 125		155	ns
15	t_{RD}	$\overline{RD}$Fall →D0 to D15 Input		2.0x – 115		45	ns
16	t_{RR}	$\overline{RD}$ Low Pulse Width	2.0x – 40		120		ns
17	t_{HR}	$\overline{RD}$Rise→ D0 to D15 Hold	0		0		ns
18	t_{RAE}	$\overline{RD}$Rise→ A0 to A15 Output	x – 25		55		ns
19	t_{WW}	$\overline{WR}$ Low Pulse Width	2.0x – 40		120		ns
20	t_{DW}	D0 to D15 Valid→ $\overline{WR}$ Rise	2.0x – 120		40		ns
21	t_{WD}	$\overline{WR}$ Rise →D0 to D15 Hold	0.5x – 40		0		ns
22	t_{AWH}	A0 to A23 Valid→ $\overline{WAIT}$ Input (1 WAIT + n mode)		3.5x – 130		150	ns
23	t_{AWL}	A0 to A15 Valid→ $\overline{WAIT}$ Input (1 WAIT + n mode)		3.0x – 100		140	ns
24	t_{CW}	$\overline{RD}/\overline{WR}$ Fall→ $\overline{WAIT}$ Hold (1 WAIT + n mode)	2.0x + 0		160		ns
25	t_{APH}	A0 to A23 Valid→ PORT Input		2.5x – 120		80	ns
26	t_{APH2}	A0 to A23 Valid→ PORT Hold	2.5x + 50		250		ns
27	t_{CP}	$\overline{WR}$ Rise→ PORT Valid		200		200	ns
28	t_{ASRH}	A0 to A23 Valid→ $\overline{RAS}$ Fall	1.0x – 60		20		ns
29	t_{ASRL}	A0 to A15 Valid→ $\overline{RAS}$ Fall	0.5x – 40		0		ns
30	t_{RAC}	$\overline{RAS}$ Fall→ D0 to D15 Input		2.5x – 90		110	ns
31	t_{RAH}	$\overline{RAS}$ Fall→ A0 to A15 Hold	0.5x – 25		15		ns
32	t_{RAS}	$\overline{RAS}$ Low Pulse Width	2.0x – 40		120		ns
33	t_{RP}	$\overline{RAS}$ High Pulse Width	2.0x – 40		120		ns
34	t_{RSH}	$\overline{CAS}$ Fall→ $\overline{RAS}$ Rise	1.0x – 55		25		ns
35	t_{RSC}	$\overline{RAS}$ Rise→ $\overline{CAS}$ Rise	0.5x – 25		15		ns
36	t_{RCD}	$\overline{RAS}$ Fall→ $\overline{CAS}$ Fall	1.0x – 40		40		ns
37	t_{CAC}	$\overline{CAS}$ Fall→ D0 to D15 Input		1.5x – 120		0	ns
38	t_{CAS}	$\overline{CAS}$ Low Pulse Width	1.5x – 30		80		ns

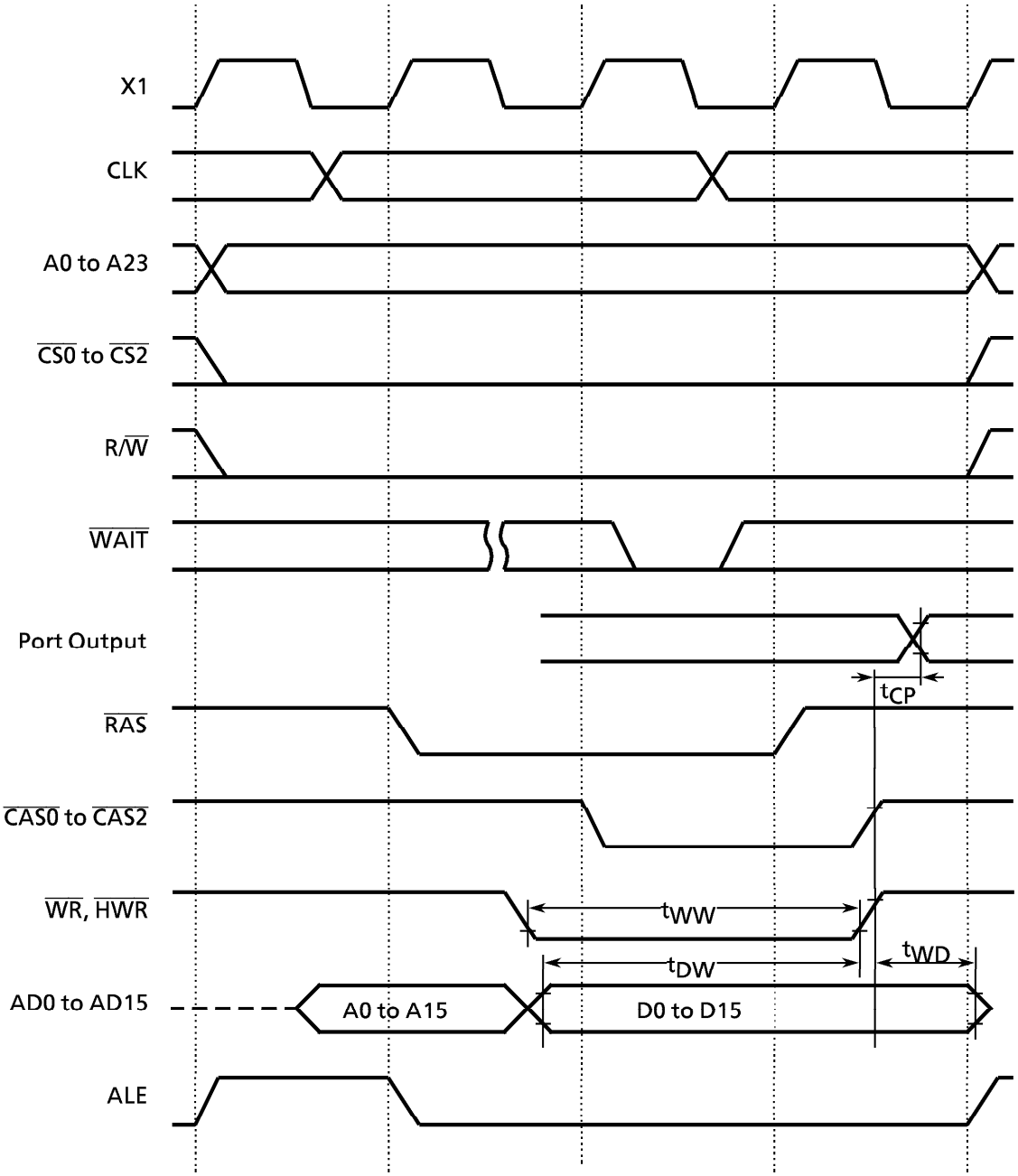
AC Measuring Conditions

- Output Level: High $0.7 \times V_{CC}$ / Low $0.3 \times V_{CC}$, CL = 50 pF
- Input Level: High $0.9 \times V_{CC}$ / Low $0.1 \times V_{CC}$

(1) Read Cycle


tOSC
X1
tCLK
CLK
tAK
tKA
A0 to A23
CS0 to CS2
R/W
tAWH
tCW
tAWL
WAIT
tAPH
tAPH2
Port Input
tASRH
tRSH
tRP
RAS
tRAS
tASRL
tRSC
tRAC
tRAH
tCAS
CAS0 to CAS2
tRCD
tCAC
tADH
tCA
RD
tACH
tRR
tRAE
tACL
tRD
tHR
tLC
tADL
AD0 to AD15
A0 to A15
D0 to D15
tAL
tLA
tCL
ALE
tLL

(2) Write Cycle



4.4 A/D Conversion Characteristics

AVCC = VCC, AVSS = VSS

Symbol	Parameter	Power Supply	Min	Typ	Max	Unit
V_{REFH}	Analog Reference Voltage (+)	V_{CC} = 5V ± 10 %	V_{CC} – 1.5V	V_{CC}	V_{CC}	V
		V_{CC} = 3V ± 10 %	V_{CC} – 0.2V	V_{CC}	V_{CC}	
V_{REFL}	Analog Reference Voltage (–)	V_{CC} = 5V ± 10 %	V_{SS}	V_{SS}	V_{SS} + 0.2V	
		V_{CC} = 3V ± 10 %	V_{SS}	V_{SS}	V_{SS} + 0.2V	
V_{AIN}	Analog Input Voltage Range		VREFL		VREFH	
I_{REF} (V_{REFL} = 0 V)	Analog Current for Analog Reference Voltage <VREFON> = 1	V_{CC} = 5V ± 10 %		0.5	1.5	mA
		V_{CC} = 3V ± 10 %		0.3	0.9	
	<VREFON> = 0	V_{CC} = 2.7 to 5.5V		0.02	5.0	μA
–	Error (not including quantizing errors)	V_{CC} = 5V ± 10 %		± 1.0	± 3.0	LSB
		V_{CC} = 3V ± 10 %		± 1.0	± 3.0	

Note 1 : 1LSB = (VREFH – VREFL) / 2^{10} [V]
Note 2 : The operation of this A/D converter is guaranteed only using fc (the high-frequency oscillator). It is not guaranteed for fs.
The operation above is guaranteed for $f_{FPH} \geqq 4$ MHz.
Note 3 : The value I_{CC} includes the current which flows through the AV_{CC} pin.

4.5 Serial Channel Timing

(1) I/O Interface Mode

① SCLK Input Mode

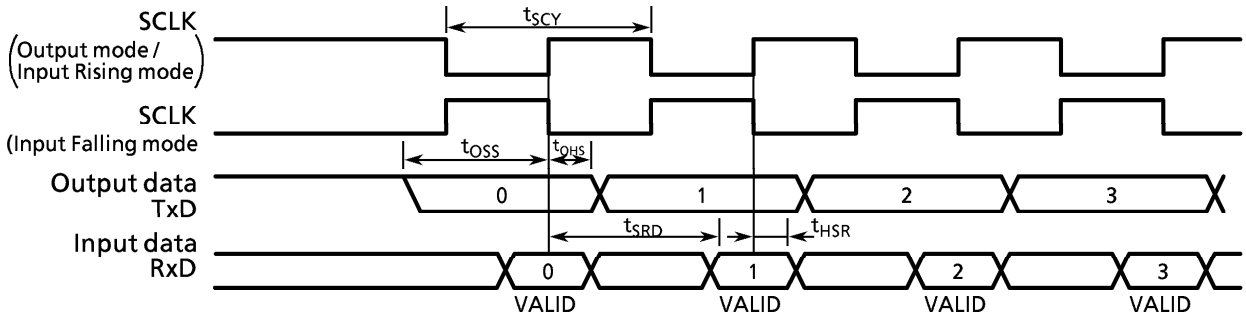
Symbol	Parameter	Variable		32.768 MHz (Note)		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{SCY}	SCLK Cycle	16X		488 μs		1.28		0.8		μs
t_{OSS}	Output Data → Rising Edge or Falling Edge* of SCLK	t_{SCY}/2 – 5X – 50		91.5 μs		190		100		ns
t_{OHS}	SCLK Rising Edge or Falling Edge* → Output Data Hold	5X – 100		152 μs		300		150		ns
t_{HSR}	SCLK Rising Edge or Falling Edge* → Input Data Hold	0		0		0		0		ns
t_{SRD}	SCLK Rising Edge or Falling Edge* → Effective Data Input		t_{SCY} – 5X – 100		336 μs		780		450	ns

Note: System clock is fs, or input clock to prescaler is divisor clock of fs.
* The rising edge is used in SCLK Rising mode.
The falling edge is used SCLK Falling mode.

② SCLK Output Mode

Symbol	Parameter	Variable		32.768 MHz (Note)		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{SCY}	SCLK Cycle (Programmable)	16X	8192X	488 μs	250 ms	1.28	655.36	0.8	409.6	μs
t_{OSS}	Output Data → SCLK Rising Edge	t_{SCY} – 2X – 150		427 μs		970		550		ns
t_{OHS}	SCLK Rising Edge→ Output Data Hold	2X – 80		60 μs		80		20		ns
t_{HSR}	SCLK Rising Edge→ Input Data Hold	0		0		0		0		ns
t_{SRD}	SCLK Rising Edge→ Effective Data Input		t_{SCY} – 2X – 150		428 μs		970		550	ns

Note: System clock is fs, or input clock to prescaler is divisor clock of fs.



4.6 Timer/Counter Input Clock (TI0, TI4, TI5, TI6, TI7)

Symbol	Parameter	Variable		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t_{VCK}	Clock Cycle	8X + 100		740		500		ns
t_{VCKL}	Low Level Clock Pulse Width	4X + 40		360		240		ns
t_{VCKH}	High Level Clock Pulse Width	4X + 40		360		240		ns

4.7 Interrupt and Capture

(1) $\overline{NMI}$, INT0 interrupts

Symbol	Parameter	Variable		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t_{INTAL}	$\overline{NMI}$, INT0 Low Level Pulse Width	4X		320		200		ns
t_{INTAH}	$\overline{NMI}$, INT0 High Level Pulse Width	4X		320		200		ns

(2) INT4 to 7 interrupts, capture

The INT4 to 7 input pulse width depends on the CPU operation clock and timer (9-bit prescaler). The following shows the pulse width for each clock.

System clock selected <SYSCK>	Prescaler clock selected <PRCK1 to 0>	t_{INTBL} (INT4 to 7 low level pulse width)		t_{INTBH} (INT4 to 7 high level pulse width)		Unit
		Variable	20 MHz	Variable	20 MHz	
		Min	Min	Min	Min	
0 (fc)	00 (f_{FPH})	8X + 100	500	8X + 100	500	ns
	01 (fs)	8XT + 0.1	244.3	8XT + 0.1	244.3	μs
	10 (fc/16)	128X + 0.1	6.5	128X + 0.1	6.5	
1 (fs) (Note 2)	00 (f_{FPH})	8XT + 0.1	244.3	8XT + 0.1	244.3	
	01 (fs)					

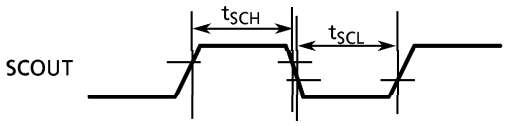
Note 1: XT represents the frequency of the low frequency clock fs. Calculated at fs = 32.768 kHz.
Note 2: When using fs as the system clock, fc/16 cannot be selected as the prescaler clock.

4.8 SCOUT pin AC characteristics

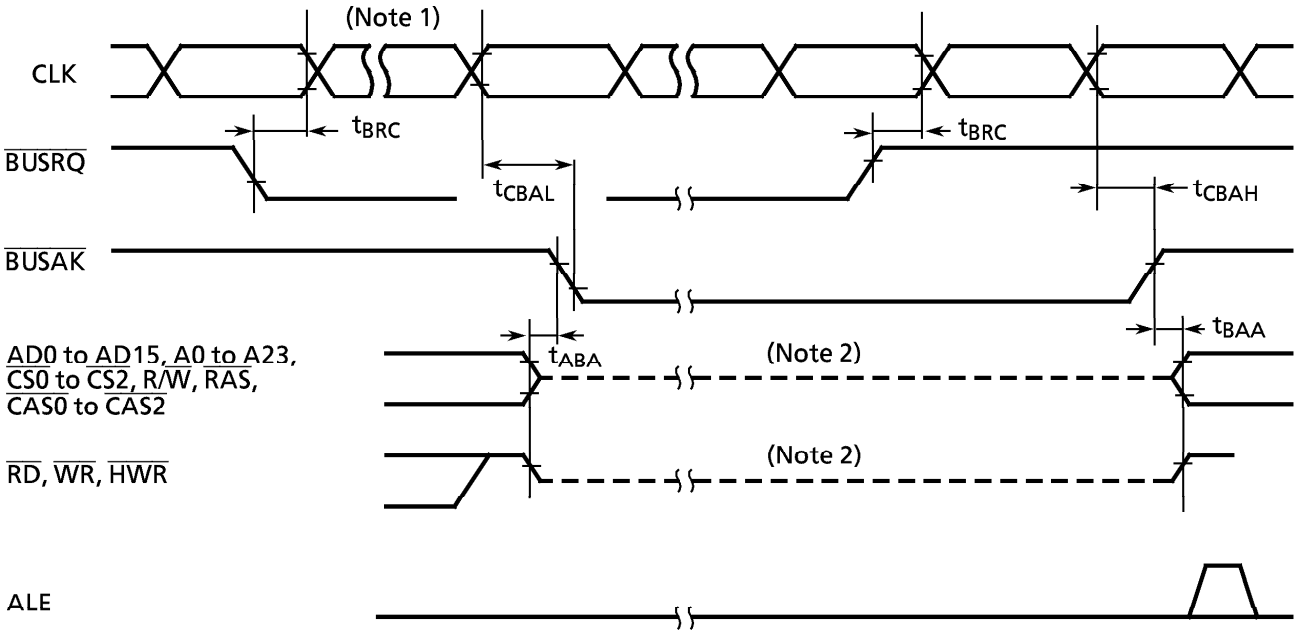
Symbol	Parameter	Variable		10 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t_{SCH}	High-Level Pulse Width V_{CC} = 5 V ± 10 %	0.5X – 10		30		15		ns
	High-Level Pulse Width V_{CC} = 3 V ± 10 %	0.5X – 20		20		–	–	
t_{SCL}	Low-Level Pulse Width V_{CC} = 5 V ± 10 %	0.5X – 10		30		15		ns
	Low-Level Pulse Width V_{CC} = 3 V ± 10 %	0.5X – 20		20		–	–	

Measurement condition

- Output level: High 2.2 V / Low 0.8 V, CL = 10 pF



4.9 Timing Chart for Bus Request ($\overline{BUSRQ}$) / Bus Acknowledge ($\overline{BUSAK}$)



Symbol	Parameter	Variable		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t_{BRC}	$\overline{BUSRQ}$ Set-up Time to CLK	120		120		120		ns
t_{CBAL}	CLK→ $\overline{BUSAK}$ Falling Edge		1.5X + 120		240		195	ns
t_{CBAH}	CLK→ $\overline{BUSAK}$ Rising Edge		0.5X + 40		80		65	ns
t_{ABA}	Output Buffer off to $\overline{BUSAK}$ ↓	0	80	0	80	0	80	ns
t_{BAA}	$\overline{BUSAK}$ ↑ to Output Buffer on	0	80	0	80	0	80	ns

Note 1: Even if the $\overline{BUSRQ}$ signal goes low, the bus will not be released while the $\overline{WAIT}$ signal is low. The bus will only be released when $\overline{BUSRQ}$ goes low while $\overline{WAIT}$ is high.

Note 2: This line shows only that the output buffer is in the off state.
It does not indicate that the signal level is fixed.
Just after the bus is released, the signal level set before the bus was released is maintained dynamically by the external capacitance. Therefore, to fix the signal level using an external resistor during bus release, careful design is necessary, as fixing of the level is delayed.
The internal programmable pull-up/pull-down resistor is switched between the active and non-active states by the internal signal.

4.10 Recommended oscillator

The TMP93CM40/M41 are evaluated with vasious resonators. The evaluation results are displayed below to enable appropriate selection for any given application.

Note : The load capacitance of the resonator consists of the load capacitors C1 and C2 which are to be connected and the floating capacitance of the target board.

Even if the specified values of C1 and C2 are used, there is a possibility that the oscillator will malfunction due to varying load capacitance on the target boards. Hence the oscillator's wiring patterns on the board should be designed to be as short as possible.

It is recommended that evaluation of the resonators be conducted on the target board.

(1) Examples of Resonator Connection

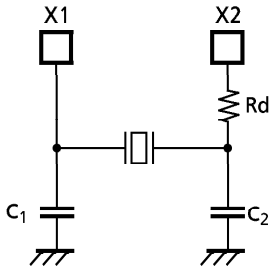


Figure 1: Example of High Frequency Resonator Connection

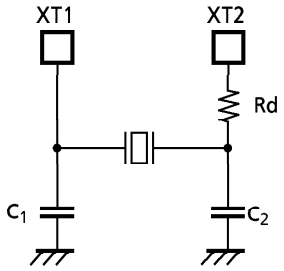


Figure 2: Example of Low Frequency Resonator Connection

(2) Ceramic resonator: Toyama Murata Mfg. Co., Ltd (Note 1)

Ta = – 20 to 80°C

Parameter	Frequency (MHz)	Recommended resonator	Recommended value			Vcc [V]
			C_1 [pF]	C_2 [pF]	Rd [kΩ]	
High-frequency oscillation	4.00	CSA4.00MG	30	30	0	2.7 to 5.5
		CST4.00MGW	(30) (Note 2)	(30) (Note 2)		
	10.00	CSA10.0MTZ093	30	30		
		CST10.0MTW093	(30) (Note 2)	(30) (Note 2)		
	12.50	CSA12.5MTZ093	30	30		
		CST12.5MTW093	(30) (Note 2)	(30) (Note 2)		
	16.00	CSA16.00MXZ040	5	5		4.5 to 5.5
		CST16.00MXW0C1	(5) (Note 2)	(5) (Note 2)		
	20.00	CSA20.00MXZ040	3	3		

Note 1 : TOYAMA MURATA MFG. CO., LTD. (JAPAN)
Product Engineering Service Section
Phone : 0764-29-1221, Fax : 0764-29-4962

Note 2 : For built-in condenser type

(3) Crystal resonator: Nihon Denpa Kogyo (Note 1)

Ta = – 10 to 60 °C

Parameter	Frequency (MHz)	Recommended resonator	Recommended value			Vcc [V]
			C_1 [pF]	C_2 [pF]	Rd [kΩ]	
High-frequency oscillation	4.00	NT040016A	12	12	0	2.7 to 5.5
	10.00	NT100016A	10	10		
	12.50	NT125016A	10	10		
	16.00	NT160016A	10	10		4.5 to 5.5
	20.00	NT200016A	7	7		
Low-frequency oscillation	32.768 kHz	NT0003125A	15	15	470	2.7 to 5.5

Note 1 : NDK AMERICA, INC. : U.S.A Phone : 1-510-623-6500, Fax : 1-510-623-6590
NDK ELECTRONICS SINGAPORE PTE, LTD. Phone : 65-298-9878, Fax : 65-293-1150
NDK ELECTRONICS (HK) LIMITED: HONG KONG Phone : 852-2956-3181, Fax : 852-2956-1567
NDK EUROPE LIMITED: ENGLAND Phone : 44-181-390-8344, Fax : 44-181-390-6926
NDK FRANCE SARL : FRANCE Phone : 33-1-43-04-0000, Fax : 33-1-43-04-0634
NDK ITALY SRL : ITALY Phone : 39-2-96702920, Fax : 39-2-96703284
NDK SCANDINAVIA AB : SWEDEN Phone : 46-8-632-0001, Fax : 46-8-632-0070

Note 2 : High-frequency resonator
NR-18 : Lead mount type
AT-51 : Lead mount type
CP12A : Surface mount type

Note 3 : Low-frequency resonator
MX-38T : Lead mount type