CMOS 8-Bit Microcontroller

TMPA8700CHN/F, TMPA8700CKN/F, TMPA8700CMN/F, TMPA8700CPN/F, TMPA8700CSN/F

The A8700CH/CK/CM/CP/CS is the high speed and high performance 8 bit single chip microcomputer. This MCU contains CPU core, ROM, RAM, input / output ports, six multi-function timer / counter, serial interface, on-screen display, data slicer, jitter elimination circuit, PWM, 8 bit A/D converter and remote control signal processor on a chip.
The functions of the OSD circuit conform to the on-screen display functions of closed caption decoders based on FCC standards.

Part No.	ROM	RAM	Package	OTP MCU
TMPA8700CHN/F	16 Kbytes	1 Kbytes	SDIP42-P-600-1.78	TMPA8700PSN/F
TMPA8700CKN/F	24 Kbytes			
TMPA8700CMN/F	32 Kbytes			
TMPA8700CPN/F	48 Kbytes	2 Kbytes		
TMPA8700CSN/F	60 Kbytes			

Features

◆8 bit single chip microcomputer TLCS-870 Series
◆Instruction execution time : 0.5 μs (At 8 MHz)
◆412 basic instructions
- Multiplication and Division (8 bits × 8 bits, 16 bits ÷ 8 bits)
  : Instruction execution time 3.5 μs (At 8 MHz)
- Bit manipulations (Set / Clear / Complement / Move / Test / Exclusive Or)
- 16 bit data operations
- 1 byte jump / subroutine-call (Short relative jump / Vector call)

◆14 interrupt sources (External : 5, Internal : 9)
- All sources have independent latches each, and nested interrupt control is available.
- Three edge-selectable external interrupts with noise reject
- High-speed task switching by register bank changeover

◆Input / Output ports (33 pins)
◆Two 16 bit Timer / Counters
- Timer, Event counter, Pulse width measurement, External trigger timer, Window modes

◆Two 8 bit Timer / Counters
- Timer, Event counter, Capture (Pulse width / duty measurement) modes

◆Time Base Timer
- Interrupt frequency : 1 Hz to 16384 Hz

◆Watchdog Timer

◆Serial bus Interface
- I^2C-bus (Single master) / 8 bits SIO timeshared 2ch

◆On-screen display circuit
- Character patterns : 251 characters
- Character displayed : 32 columns 8 rows
- Composition : 8 × 9 dots
- Size of character : 3 kinds (Line by line)
- Color of character : 7 kinds (Character by character)
- Variable display position : Horizontal 128 steps, Vertical 256 steps
- Fringing, Smoothing function
- Conform to US CLOSED CAPTION DECODER REGULATION

◆PWM outputs
- 14 bit PWM output (1 channel)
- 7 bit PWM outputs (9 channels)

◆8 bit successive approximate type A / D converter with sample and hold
- 6 analog inputs
- Conversion time : 23 μs at 8 MHz

◆High current outputs : LED direct drive capability (Typ. 20 mA × 4 bits).

◆Remote control signal processor

◆Data slicer circuit 1 ch

◆Jitter elimination circuit

◆Test video signal generator

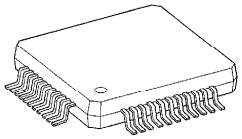
◆ROM corrective function

◆Two Power saving operating modes
- STOP mode : Oscillation stops. Battery / Capacitor back-up. Port output hold / high-impedance.
- IDLE mode : CPU stops, and Peripherals operate using high-frequency clock. Release by interrupts.

◆Emulation Pod : BMA8700CSN0A

Package

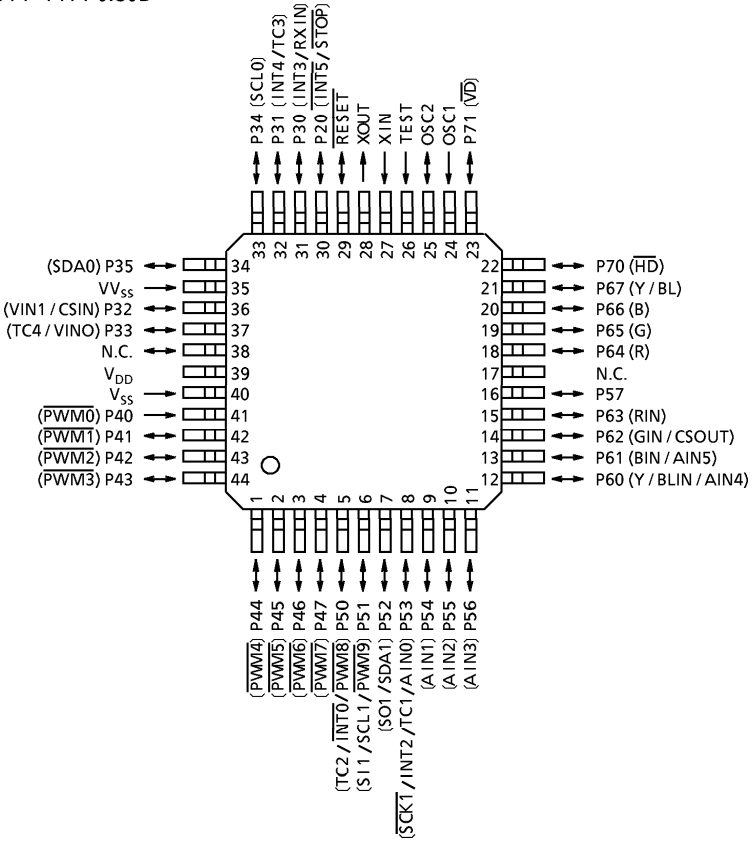
QFP44-P-1414-0.80D



TMPA8700CHF
TMPA8700CKF
TMPA8700CMF
TMPA8700CPF
TMPA8700CSF

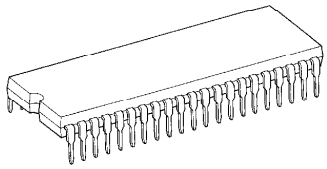
Pin Assignments (Top View)

QFP44-P-1414-0.80D



Package

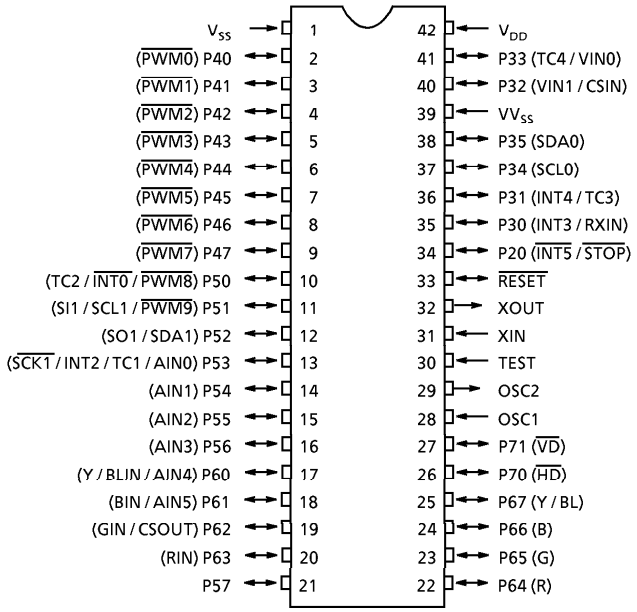
SDIP42-P-600-1.78



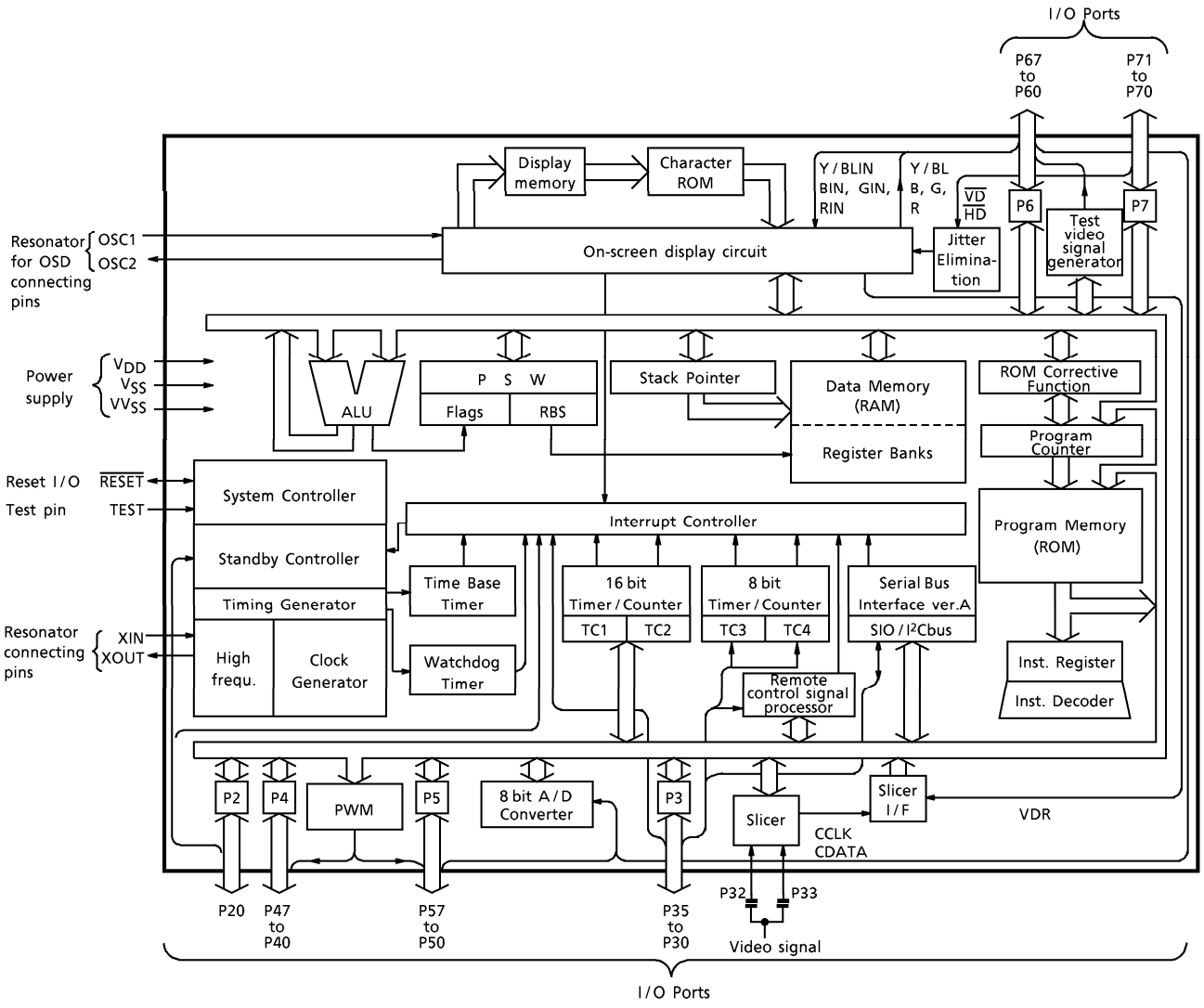
TMPA8700CHN
TMPA8700CKN
TMPA8700CMN
TMPA8700CPN
TMPA8700CSN

Pin Assignments (Top View)

SDIP42-P-600-1.78



Block Diagram



Pin Function

Pin No.	Pin Name	Input / Output	Function	
34	P20 ($\overline{INT5}$ / $\overline{STOP}$)	I / O (Input, Input)	1 bit input / output port with latch. When used as an input port, an interrupt input or STOP mode release signal input, the latch must be set to "1".	External interrupt input 5 / STOP mode release signal input
38	P35 (SDA0)	I / O (I / O)	6 bit programmable input / output port. (tri-state) Each bit of this port can be individually as an input or an output under software control. During reset, all bits are configured as inputs. When used as an input port, a timer / counter input, a remote control signal processor input, data slicer input, or an interrupt input, the pin must be set to the input mode. When used as a serial bus interface input / output, the pin must be set to the sink open drain mode, the latch must be set to "1", and the pin must be set to the output mode.	I^2C bus 0 serial data input / output
37	P34 (SCL0)	I / O (I / O)		I^2C bus 0 serial clock input / output
41	P33 (TC4 / VIN0)	I / O (Input, Input)		Timer / counter 4 input / Video signal input 0
40	P32 (VIN1 / CSIN)	I / O (Input, Input)		Video signal input 1 / Composite sync input
36	P31 (INT4 / TC3)	I / O (Input, Input)		External interrupt input 4 / Timer / Counter 3 input
35	P30 (INT3 / RXIN)	I / O (Input, Input)		External interrupt input 3 / Remote control signal processor input
9 to 3	P47 ($\overline{PWM7}$) to P41 ($\overline{PWM1}$)	I / O (Output)	8 bit programmable input / output port (tri-state). Each bit of this port can be individually as an input or an output under software control. During reset, all bits are configured as inputs. When used as a PWM output, the latch must be set to "1" and the pin must be set to the output mode.	7 bit PWM outputs
2	P40 ($\overline{PWM0}$)			14 bit PWM output
21	P57	I / O	8 bit programmable input / output port. (tri-state) Each bit of this port can be individually as an input or an output under software control. During reset, all bits are configured a as inputs. When used as an input port, a serial bus interface input, the pin must be set to the input mode. When used as a PWM output, serial bus interface output, the latch must be set to "1", and the pin must be set to the output mode. When used as a serial bus interface input / output, the pin must be set to the sink open drain mode, the latch must be set to "1", and the pin must be set to the output mode.	
16 to 14	P56 (AIN3) to P54 (AIN1)	I / O (Input)		A / D converter analog input
13	P53 (AIN0 / TC1 / INT2 / $\overline{SCK1}$)	I / O (Input, Input, Input, I / O)		A / D converter analog input / Timer / Counter 1 input / External interrupt input / SIO1 serial clock data input
12	P52 (SDA1 / SO1)	I / O (I / O, Output)		I^2C bus 1 serial data input / output SIO1 serial data output
11	P51 ($\overline{PWM9}$ / SCL1 / SI1)	I / O (Output, I / O, Input)		I^2C bus 1 serial clock input / output / 7 bit PWM outputs/SIO1 serial data input
10	P50 ($\overline{PWM8}$ / $\overline{INT0}$ / TC2)	I / O (Output, Input, Input)		7 bit PWM outputs / External interrupt input 0 / Timer / Counter 2 input
27	P71 ($\overline{VD}$)	I / O (Input)	2 bit input / output port with latch. When used as an input port, a vertical synchronous signal input, or a horizontal synchronous signal input, the latch must be set to "1".	Vertical synchronous signal input
26	P70 ($\overline{HD}$)			Horizontal synchronous signal input
25	P67 (Y / BL)	I / O (Output)	8 bit programmable input / output port (tri-state, P63 to P60 : High current output). Each bit of this port can be individually as an input or an output under software control. During reset, all bits are configured as inputs. When P67 to P64 ports are used as output port, bits 7 to 4 of address $0F91_H$ must be set to "1". When P63 to P60 port used as RIN, GIN, BIN, Y / BLIN input, these ports must be set to the input mode.	R, G, B, Y / BL output
24	P66 (B)			
23	P65 (G)			
22	P64 (R)			
20	P63 (RIN)	I / O (Input)		G, B, Y / BL input: Test video signal generator output
19	P62 (GIN / CSOUT)	I / O (Input / Output)		
18	P61 (BIN / AIN5)	I / O (Input / Input)		G, B, Y / BL input: A / D converter analog input
17	P60 (Y / BLIN / AIN4)	I / O (Input / Input)		
28, 29	OSC1, OSC2	Input, Output	Resonator connecting pin of on-screen display circuit	
31, 32	XIN, XOUT		Resonator connecting pin (High frequency). For external clock input, XIN is used and XOUT is opened.	
33	$\overline{RESET}$	I / O	Reset signal input or watchdog timer output / address-trap-reset output / system-clock-reset output.	
30	TEST	Input	Test pin for out-going test. Be tied to low.	
42 ; 1, 39	V_{DD}, V_{SS}, VV_{SS}	Power Supply	+ 5 V, 0 V (GND)	

Operational Description

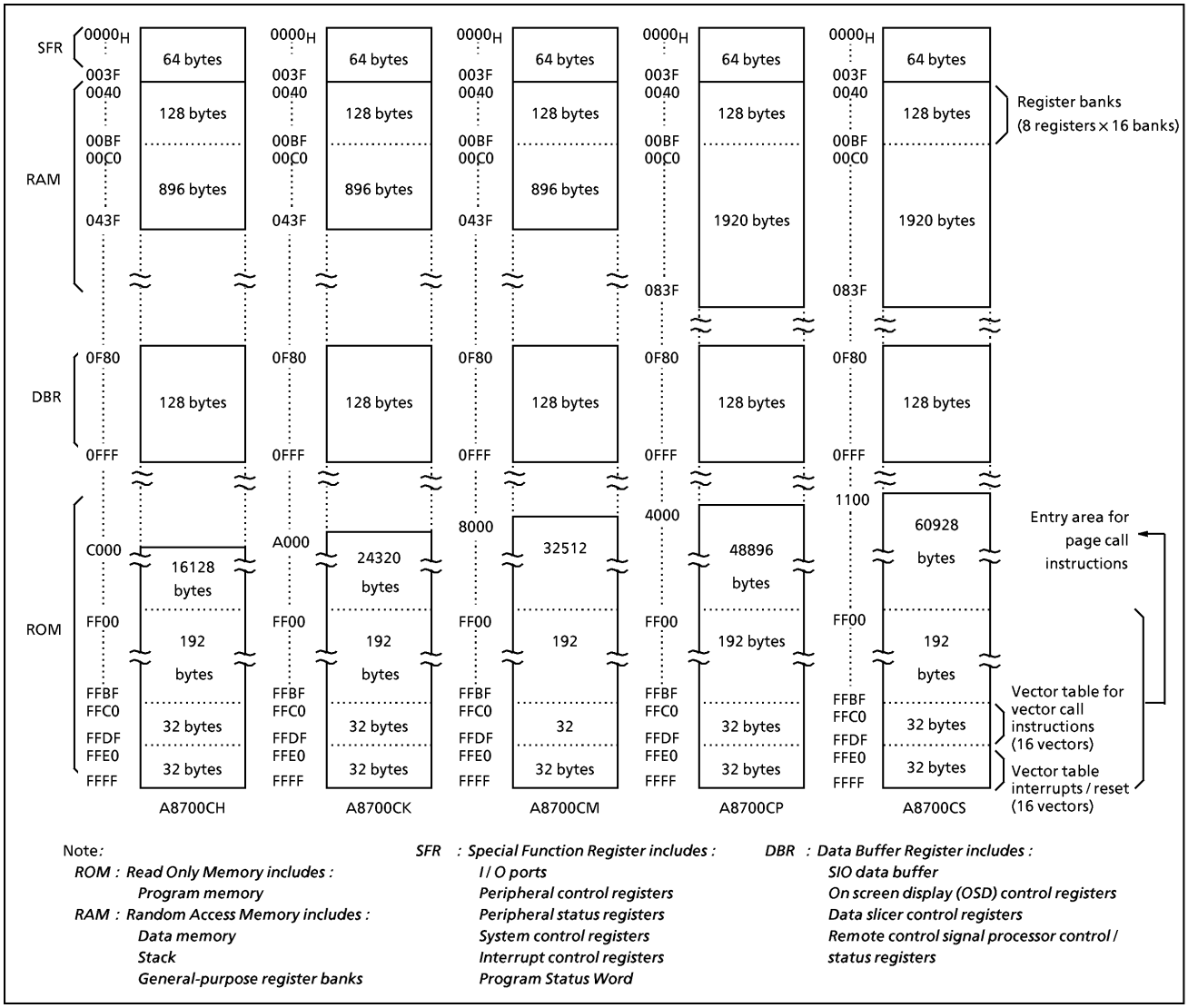
1. CPU Core Functions

The CPU core consists of a CPU, a system clock controller, an interrupt controller, a watchdog timer, and ROM corrective function.

This section provides a description of the CPU core, the program memory (ROM), the data memory (RAM), and the reset circuit.

1.1 Memory Address Map

The TLCS-870 Series is capable of addressing 64 Kbytes of memory. Figure 1-1. shows the memory address maps of the A8700CH / CK / CM / CP / CS. In the TLCS-870 Series, the memory is organized 4 address spaces (ROM, RAM, SFR, and DBR). It uses a memory mapped I / O system, and all I / O registers are mapped in the SFR / DBR address spaces. There are 16 banks of general-purpose registers. The register banks are also assigned to the first 128 bytes of the RAM address space.



Note:

ROM : Read Only Memory includes :
Program memory

RAM : Random Access Memory includes :
Data memory
Stack
General-purpose register banks

SFR : Special Function Register includes :
I / O ports
Peripheral control registers
Peripheral status registers
System control registers
Interrupt control registers
Program Status Word

DBR : Data Buffer Register includes :
SIO data buffer
On screen display (OSD) control registers
Data slicer control registers
Remote control signal processor control / status registers

Figure 1-1. Memory Address Map

Electrical Characteristics

Absolute Maximum Ratings (V_{SS} = 0 V)

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage	V_{DD}	—	– 0.3 to 6.5	V
Input Voltage	V_{IN}	—	– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT1}	—	– 0.3 to V_{DD} + 0.3	V
Output Current (Per 1pin)	I_{OUT1}	Ports P2, P3, P4, P5, P64 to P67, P7	3.2	mA
	I_{OUT2}	P60 to P63	30	
Output Current (Total)	ΣI_{OUT1}	Ports P2, P3, P4, P5, P64 to P67, P7	120	mA
	ΣI_{OUT2}	P60 to P63	120	
Power Dissipation [T_{opr} = 70°C]	P_D	—	600	mW
Soldering Temperature (time)	T_{sld}	—	260 (10 s)	°C
Storage Temperature	T_{stg}	—	– 55 to 125	°C
Operating Temperature	T_{opr}	—	– 30 to 70	°C

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded

Recommended Operating Conditions (V_{SS} = 0 V, T_{opr} = − 30 to 70°C)

Parameter	Symbol	Pins	Test Condition		Min	Max	Unit
Supply Voltage	V_{DD}	—	fc = 8 MHz	NORMAL mode	4.5	5.5	V
				IDLE mode			
				STOP mode	2.0		
Input High Voltage	V_{IH1}	Except hysteresis input	$V_{DD} \geqq 4.5$ V		$V_{DD} \times 0.70$	V_{DD}	V
	V_{IH2}	Hysteresis input			$V_{DD} \times 0.75$		
	V_{IH3}	—	$V_{DD} < 4.5$ V		$V_{DD} \times 0.90$		
Input Low Voltage	V_{IL1}	Except hysteresis input	$V_{DD} \geqq 4.5$ V		0	$V_{DD} \times 0.30$	V
	V_{IL2}	Hysteresis input				$V_{DD} \times 0.25$	
	V_{IL3}	—	$V_{DD} < 4.5$ V			$V_{DD} \times 0.10$	
Clock Frequency	fc	XIN, XOUT	V_{DD} = 4.5 to 5.5 V		—	8.0	MHz
	f_{OSD}	OSC1, OSC2	V_{DD} = 4.5 to 5.5 V	Double frequency mode (FORS = 1)	2	6	
				Normal freguency mode (FORS = 0)	2	12	

Note 1: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

Note 2: fc : The condition of power supply voltage is limited to NORMAL and IDLE mode.
Furthermore, since the CPU clock serves dual purposes as a clock for the CCD slier, always be sure to use an 8 MHz oscillator.

Electrical Characteristics

D.C. Characteristics (V_{SS} = 0 V, T_{opr} = − 30 to 70°C)

Parameter	Symbol	Pins	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Hysteresis Voltage	V_{HS}	Hysteresis inputs	—	—	—	0.9	—	V
Input Current	I_{IN1}	TEST	—	V_{DD} = 5.5 V, V_{IN} = 5.5 V / 0V	—	—	± 2	μA
	I_{IN2}	Open drain ports	—	V_{DD} = 5.5 V, V_{IN} = 5.5 V / 0 V	—	—	± 2	
	I_{IN3}	Tri-state ports	—	V_{DD} = 5.5 V, V_{IN} = 5.5 V / 0 V	—	—	± 2	
	I_{IN4}	$\overline{RESET}$, $\overline{STOP}$						
Input Resistance	R_{IN2}	$\overline{RESET}$	—	—	100	220	450	kΩ
Output Leakage Current	I_{LO}	Open drain ports and tri-state ports	—	V_{DD} = 5.5 V, V_{OUT} = 5.5 V	—	—	2	μA
Output High Voltage	V_{OH2}	Tri-state ports	—	V_{DD} = 4.5 V, I_{OH} = − 0.7 mA	4.1	—	—	V
Output Low Voltage	V_{OL}	Except XOUT, OSC2, P60 to 63	—	V_{DD} = 4.5 V, I_{OL} = 1.6 mA	—	—	0.4	V
Output Low Current	I_{OL3}	P60 to P63	—	V_{DD} = 4.5 V, V_{OL} = 1.0 V	—	20	—	mA
Supply Current in NORMAL Mode	I_{DD}	—	—	V_{DD} = 5.5 V (Note 3) fc = 8 MHz V_{IN} = 5.3 V / 0.2 V	—	13	25	mA
Supply Current in IDLE Mode					—	8	18	mA
Supply Current in STOP Mode				V_{DD} = 5.5 V V_{IN} = 5.3 V / 0.2 V	—	0.5	10	μA

Note 1: Typical values show those at Topr = 25°C, VDD = 5 V.

Note 2: Input Current : The current through pull-up or pull-down resistor is not included.

Note 3: Typical current consumption during A / D conversion is 1.2 mA.

A/D Conversion Characteristics (V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, T_{opr} = − 30 to 70°C)

Parameter	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Analog Reference Voltage	V_{AREF}	—	—	—	V_{DD}	—	V
	V_{ASS}		—	—	0	—	
Analog Reference Voltage Range	ΔV_{AREF}	—	= V_{DD} − V_{SS}	—	V_{DD}	—	V
Analog Input Voltage	V_{AIN}	—	—	V_{SS}	—	V_{DD}	V
Nonlinearity Error	—	—	V_{DD} = 4.5 to 5.5 V	—	—	± 1	LSB
Zero Point Error	—	—		—	—	± 2	LSB
Full Scale Error	—	—		—	—	± 2	LSB
Total Error	—	—		—	—	± 3	LSB

Note: Total error does not include quantization error.

A.C. Chracteristics

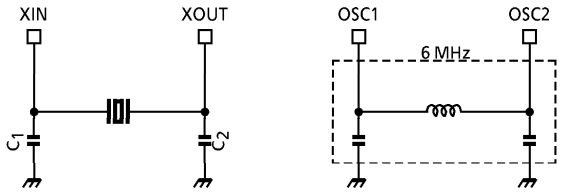
(V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, T_{opr} = – 30 to 70°C)

Parameter	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Machine Cycle Time	tcy	—	In NORMAL mode	—	0.5	—	μs
			In IDLE mode				
High Level Clock Pulse Width	t_{WCH}	—	For external clock operation (XIN input), fc = 8 MHz	62.5	—	—	ns
Low Level Clock Pulse Width	t_{WCL}						

Recommended Oscillating

(V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, T_{opr} = – 30 to 70°C)

Parameter	Oscillator	Frequency	Recommended Oscillator	Recommended Conditions	
				C_1	C_2
High-frequency	Ceramic Resonator	8 MHz	KYOCERA KBR8.0M	30 pF	30 pF
	Crystal Oscillator	8 MHz	TOYOCOM 210B 8.0000	20 pF	20 pF
OSD	LC Resonator	6 MHz	TOKO A285HCIS-13319 (5 mm)	—	—
		12 MHz	TOKO TA285HCIS-13306 (5 mm)		



(1) High-frequency (2) LC Resonator for OSD

Note: An electrical shield by metal shield plate on the surface of the IC package should be recommendable in order to prevent the device from the high electric fieldstress applied from CRT (Cathode Ray Tube) for continuous reliable operation.