NEC

MOS INTEGRATED CIRCUIT

μPD75328

4-BIT SINGLE-CHIP MICROCOMPUTER

DESCRIPTION

The μPD75328 is one of the 75X Series 4-bit single-chip microcomputer, and has a data processing capability comparable to that of an 8-bit microcomputer.

In addition to high-speed operation with 0.95 μs minimum instruction execution time for the CPU, the μPD75328 can also process data in 1-, 4-, and 8-bit units. Therefore, as a 4-bit single-chip microcomputer chip having a built-in LCD controller/driver and A/D converter, its data processing capability is the highest in its class in the world.

The μPD75P328 with one-time PROM, which is replaced with the internal mask ROM for a μPD75328, is applicable for evaluating systems under development, or for small-scale production of developed systems.

"Detailed functions are described in the following user's manual. Be sure to read it for designing."
"μPD75328 User's Manual: IEM-5045"

FEATURES

- Capable of high-speed operation and variable instruction execution time to power save
  - 0.95 μs, 1.91 μs, 15.3 μs (Main system clock: operating at 4.19 MHz)
  - 122 μs (Subsystem clock: operating at 32.768 kHz)
- 75X architecture comparable to that for an 8-bit microcomputer is employed
- Built-in programmable LCD controller/driver
- Built-in 8-bit resolution A/D converter: 6 channels
- Clock operation at reduced power dissipation: 5 μA TYP. (operating at 3 V)
- Timer function: 3 channels
- Interrupt functions especially enhanced for applications, such as remote control receiver
- Pull-up resistors can be provided for 35 I/O lines
- Built-in NEC standard serial bus interface (SBI)

APPLICATIONS

Cameras, blood pressure gauges, airconditioners, etc.

ORDERING INFORMATION

Part Number	Package	Quality Grade
μPD75328GC-xxx-3B9	80-pin plastic QFP (□14mm)	Standard

Remarks: xxx is ROM code number.

Please refer to "Quality Grade on NEC Semiconductor Devices" (Document Number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

The information in this document is subject to change without notice.

Document No. IC-2763B
(O. D. No. IC-7628D)
Date Published November 1993 P
Printed in Japan

The mark ★ shows the major revised points.

FUNCTIONAL OUTLINE (1/2)

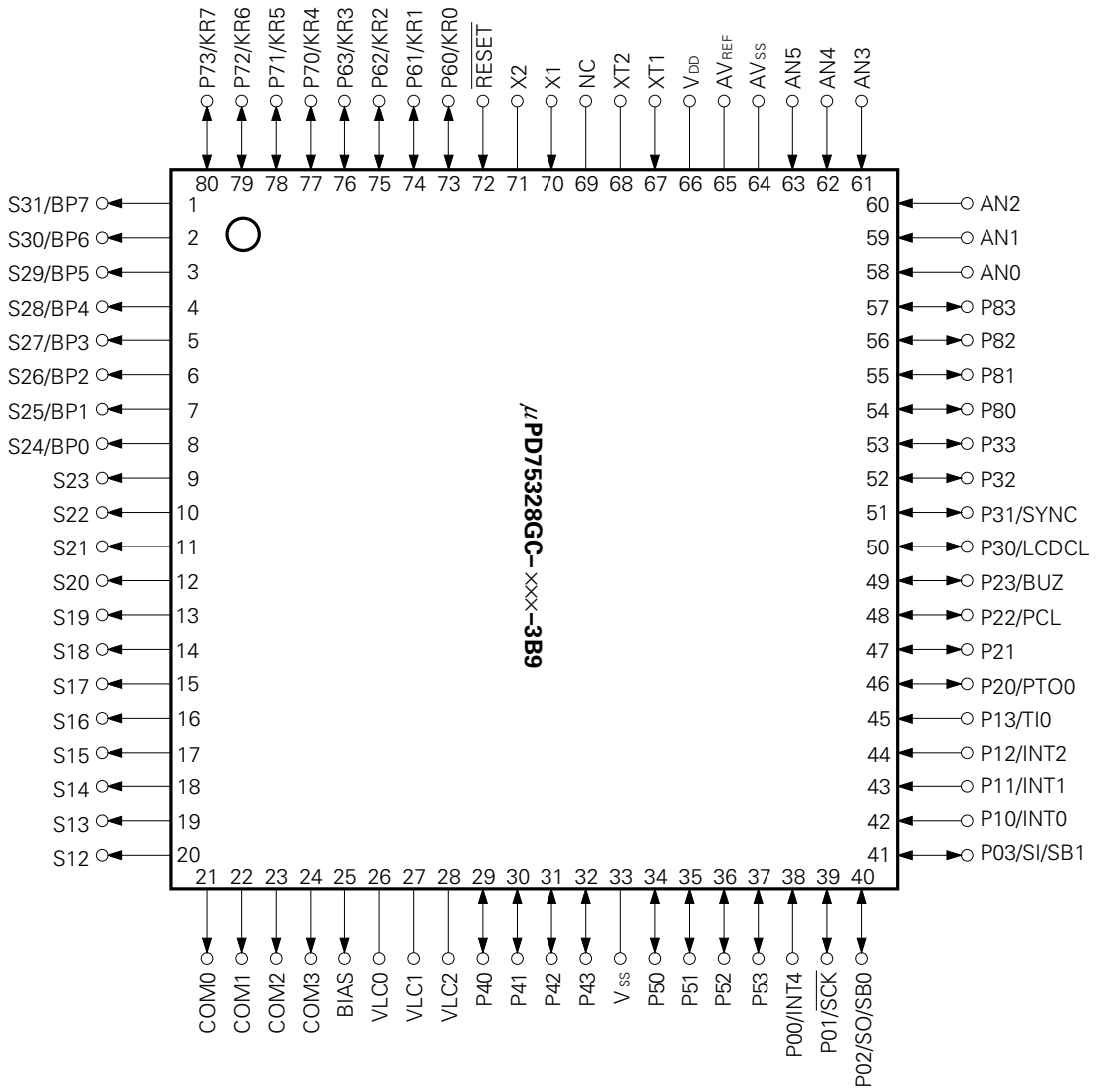
Item		Function			
Number of Basic Instructions		41			
Instruction Execution Time		0.95, 1.91, and 15.3 μs, (Main system clock: operating at 4.19 MHz) 122 μs (Subsystem clock: operating at 32.768 kHz)			
Internal Memory	ROM	8064 × 8-bit			
	RAM	512 × 4-bit			
General-Purpose Registers		4-bit manipulation: 8×4 banks, 8-bit manipulation: 4×4 banks			
I/O Line (Including the pins which also serve as LCD drive pins. Excluding the pins which is specifically provided for driving LCD.)		44	8	CMOS Input pins	Internal pull-up resistor specification by software is possible (except P00).
			20	CMOS input/output pins	
			8	CMOS output pins	Also serve as segment pins
			8	N-ch open-drain input/output	Withstand voltage: 10V Internal pull-up resistor specification by mask option is possible.
LCD Controller/ Driver		• LCD drive output pins • Segment output pins: 20 (CMOS output pins: 8) • Common output pins: 4 • Capable of driving up to 20 × 4 segments • Display output mode: Static, 1/2, 1/3, 1/4 duty			
A/D Converter		8-bit resolution x 6 channels (successive approximation type) • Operating voltage V_{DD} = 3.5 to 6.0 V • A/D conversion speed 40.1 μs (operating at 4.19 MHz)			
Timer MHz)		3 chs	8-bit timer/event counter • Clock source: 4 steps • Event count is possible		
			8-bit basic interval timer • Reference time generation (1.95, 7.82, 31.3, 250 ms: operating at 4.19 • Can be used as watchdog timer		
			Clock timer • 0.5 second interval generation • Count clock source slectable (4.19 MHz/32.768 kHz) • Clock advance mode (3.9 ms time interval generation) • Buzzer output (2 kHz)		
Serial Interface		Clock synchronized serial interface • Internal NEC standard serial bus interface (SBI mode) • 3-line serial I/O mode ... MSB/LSB first selectable • 2-line serial I/O mode			
Bit Sequential Buffer		Special bit manipulation memory: 16 bits			
Clock Output (PCL)		Φ, 524, 262, 65.5 kHz (Main system clock: 4.19 MHz)			
Buzzer Output (BUZ)		2 kHz (with main system clock or subsystem clock operated)			
Vector Interrupt		• External: 3 • Internal: 3			
Test Input		• External: 1 • Internal: 1			

FUNCTIONAL OUTLINE (2/2)

Item	Function
System Clock Generator	• Main system clock generation ceramic/crystal oscillator; 4.194304 MHz • Subsystem clock generation crysal oscillator: 32.768 kHz
Standby	STOP/HALT mode
Operating Temperature Range	–40 to +85°C
Operating Supply Voltage	V_{DD} = 2.7 to 6.0 V
Package	80-pin plastic QFP (□14 mm)

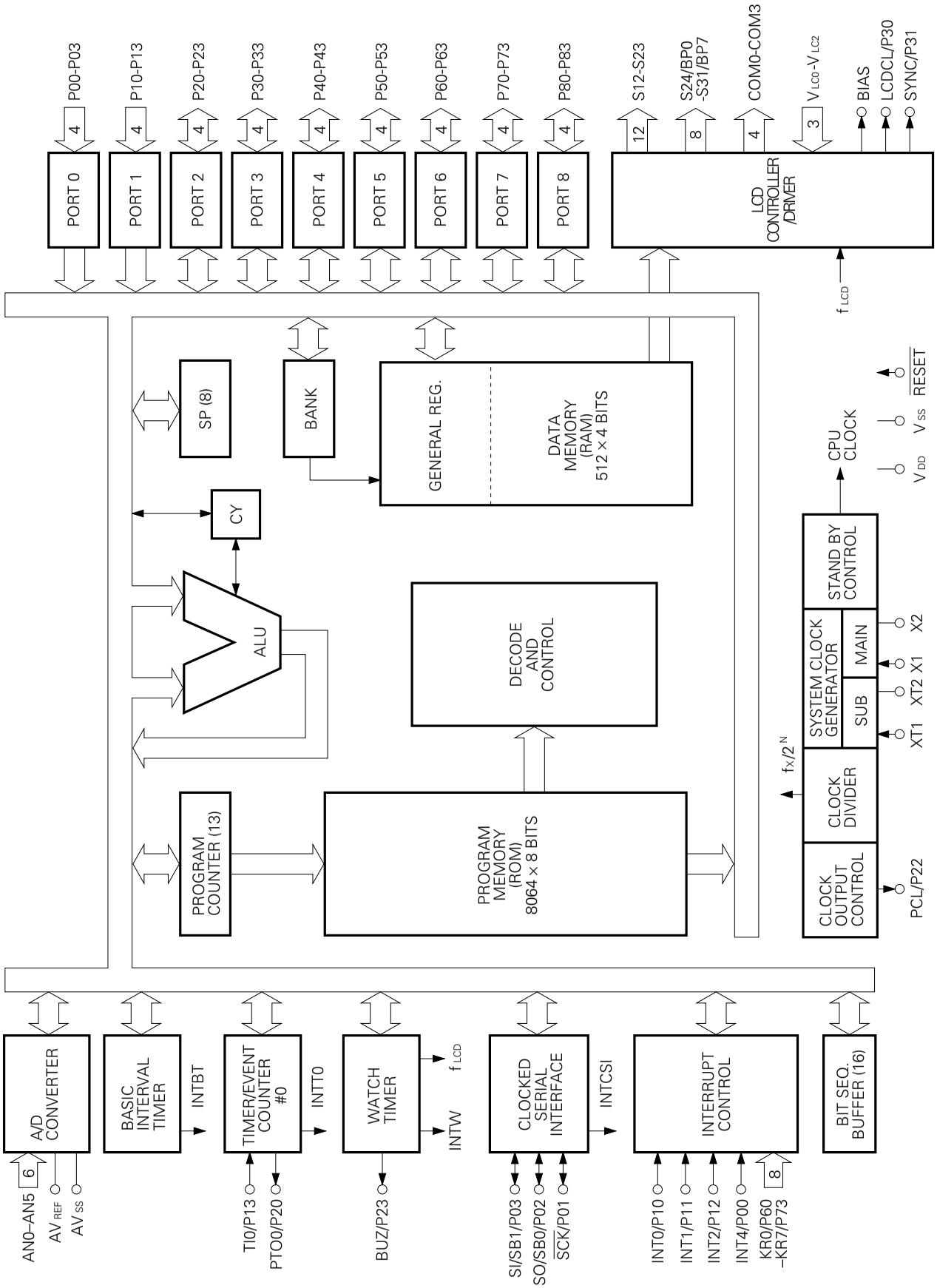
CONTENTS

1. PIN CONFIGURATION (Top View)



P00-P03	: Port 0	AVSS	: Analog Ground
P10-P13	: Port 1	AN0-AN5	: Analog Input 0-5
P20-P23	: Port 2	S12-S31	: Segment Output 12-31
P30-P33	: Port 3	COM0-COM3	: Command Output 0-3
P40-P43	: Port 4	VLC0-VLC2	: LCD Power Supply 0-2
P50-P53	: Port 5	BIAS	: LCD Power Supply Bias Control
P60-P63	: Port 6	LCDCL	: LCD Clock
P70-P73	: Port 7	SYNC	: LCD Synchronization
P80-P83	: Port 8	TI0	: Timer Input 0
BP0-BP7	: Bit Port	PTO0	: Programmable Timer Output 0
KR0-KR7	: Key Return	BUZ	: Buzzer Clock
$\overline{SCK}$	: Serial Clock	PCL	: Programmable Clock
SI	: Serial Input	INT0,INT1,INT4	: External Vectored Interrupt 0,1,4
SO	: Serial Output	INT2	: External Test Input 2
SB0,SB1	: Serial Bus 0,1	X1,X2	: Main System Clock Oscillation 1,2
$\overline{RESET}$	: Reset Input	XT1,XT2	: Subsystem Clock Oscillation 1,2
AVREF	: Analog Reference	NC	: No Connection

2. BLOCK DIAGRAM



3. PIN FUNCTIONS

3.1 PORT PINS (1/2)

Pin Name	Input/Output	Also Served As	Function	8-Bit I/O	When Reset	Input/ Output Circuit TYPE*1
P00	Input	INT4	4-bit input port (PORT0) Pull-up resistors can be specified in 3-bit units for the P01 to P03 pins by software.	X	Input	(B)
P01	Input/ Output	$\overline{SCK}$				(F)-A
P02	Input/ Output	SO/SB0				(F)-B
P03	Input/ Output	SO/SB1				(M)-C
P10	Input	INT0	With noise elimination function	X	Input	(B)-C
P11		INT1	4-bit input port (PORT1) Internal pull-up resistors can be specified in 4-bit units by software.			
P12		INT2				
P13		TI0				
P20	Input/ Output	PTO0	4-bit input/output port (PORT2) Internal pull-up resistors can be specified in 4-bit units by software.	X	Input	E-B
P21		—				
P22		PCL				
P23		BUZ				
P30*2	Input/ Output	LCDCL	Programmable 4-bit input/output port (PORT3) This port can be specified for input/ output in bit units. Internal pull-up resistors can be specified in 4-bit units by software.	X	Input	E-B
P31*2		SYNC				
P32*2		—				
P33*2		—				
P40-43*2	Input/ Output	—	N-ch open-drain 4-bit input/output port (PORT4) Internal pull-up resistors can be specified in bit units. (mask option) Resistive voltage is 10 V in the open-drain mode.	○	High level (with internal pull-up resistor) or high impedance	M
P50-53*2	Input/ Output	—	N-ch open-drain 4-bit input/output port (PORT5) Internal pull-up resistors can be specified in bit units. (mask option) Resistive voltage is 10 V in the open-drain mode.		High level (with internal pull-up resistor) or high impedance	M

*1: Circles indicate Schmitt trigger inputs.

2: Can directly drive LED.

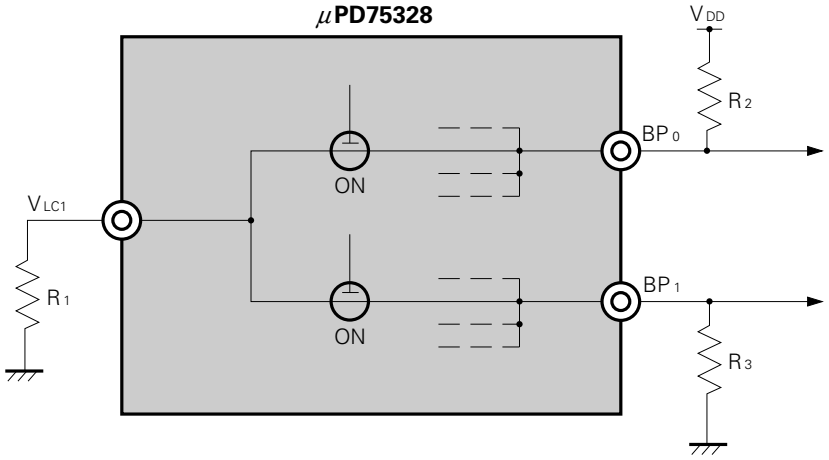
3.1 PORT PINS (2/2)

Pin Name	Input/Output	Also Served As	Function	8-Bit I/O	When Reset	Input/ Output Circuit TYPE*1
P60	Input/ Output	KR0	Programmable 4-bit input/output port (PORT6) This port can be specified for input/ output in bit units. Internal pull-up resistors can be specified in 4-bit units by software.	○	Input	(F)-A
P61		KR1				
P62		KR2				
P63		KR3				
P70	Input/ Output	KR4	4-bit input/output port (PORT7) Internal pull-up resistors can be specified in 4-bit units by software.		Input	(F)-A
P71		KR5				
P72		KR6				
P73		KR7				
P80	Input/ Output	—	4-bit input/output port (PORT8) Internal pull-up resistors can be specified in 4-bit units by software.	X	Input	E-B
P81						
P82						
P83						
BP0	Output	S24	1-bit output port (BIT PORT) Shared with a segment output pin.	X	*2	G-C
BP1		S25				
BP2		S26				
BP3		S27				
BP4	Output	S28				
BP5		S29				
BP6		S30				
BP7		S31				

*1: Circles indicate schmidt trigger inputs.

2: For BP0-7, V_{LC1} indicated below are selected as the input source. However, the output level is changed depending on BP0-7 and the V_{LC1} external circuits.

Example: Since BP0-7 are connected to each other within the μPD75328 as shown in the diagram below, the output level of BP0-7 depends on the sizes of R_1, R_2 and R_3.



3.2 NON PORT PINS

Pin Name	Input/Output	Also Served As	Functon		When Reset	Input/ Output Circuit TYPE*1
TI0	Input	P13	Timer/event counter external event pulse Input		Input	Ⓑ-C
PTO0	Output	P20	Timer/event counter output		Input	E-B
PCL	Input/ Output	P22	Clock output		Input	E-B
BUZ	Input/ Output	P23	Fixed frequency output (for buzzer or for trimming the system clock)		Input	E-B
$\overline{SCK}$	Input/ Output	P01	Serial clock input/output		Input	Ⓕ-A
SO/SB0	Input/ Output	P02	Serial data output Serial bus input/output		Input	Ⓕ-B
SI/SB1	Input/ Output	P03	Serial data input Serial bus input/output		Input	Ⓜ-C
INT4	Input	P00	Edge detection vector interrupt input (both rising and falling edge detection are effective)		Input	Ⓑ
INT0	Input	P10	Edge detection vector interrupt input (detection edge can be selected)	Clock synchronous	Input	Ⓑ-C
INT1		P11		Asynchronous		
INT2	Input	P12	Edge detection testable input (rising edge detection)	Asynchronous	Input	Ⓑ-C
KR0-KR3	Input/ Output	P60-P63	Parallel falling edge detection testable input/output		Input	Ⓕ-A
KR4-KR7	Input/ Output	P70-P73	Parallel falling edge detection testable input/output		Input	Ⓕ-A
S12-S23	Output	—	Segment signal output		*4	G-A
S24-S31	Output	BP0-7	Segment signal output		*4	G-C
COM0-COM3	Output	—	Common signal output		*4	G-B
V_{LC0}-V_{LC2}	—	—	LCD drive power Step-down resistor network (mask option)		—	—
BIAS	Output	—	External expanded driver for disconnect output		*5	
LCDCL*3	Input/ Output	P30	Externally expanded driver for clock output		Input	E-B
SYNC*3	Input/ Output	P31	Externally expanded driver sync clock output		Input	E-B
AN0-AN5	Input	—	6-bit analog input for A/D converter		Input	Y
AV_{REF}	Input	—	A/D converter reference voltage input		Input	Z
AV_{SS}	—	—	GND potential for A/D converter reference voltage input. Connected to V_{SS}.		—	—

(cont'd)

Pin Name	Input/Output	Also Served As	Function	When Reset	Input/ Output Circuit TYPE*1
X1, X2	—	—	To connect the crystal/ceramic oscillator to the main system clock generator. When inputting the external clock, input the external clock to pin X1, and the reverse phase of the external clock to pin X2.	—	—
XT1, XT2	—	—	To connect the crystal oscillator to the subsystem clock generator. When the external clock is used, pin XT1 inputs the external clock. In this case, pin XT2 must be left open. Pin XT1 can be used as a 1-bit input pin.	—	—
$\overline{\text{RESET}}$	Input	—	System reset input	—	(B)
NC *2	—	—	No connection	—	—
V_{DD}	—	—	Positive power supply	—	—
V_{SS}	—	—	GND	—	—

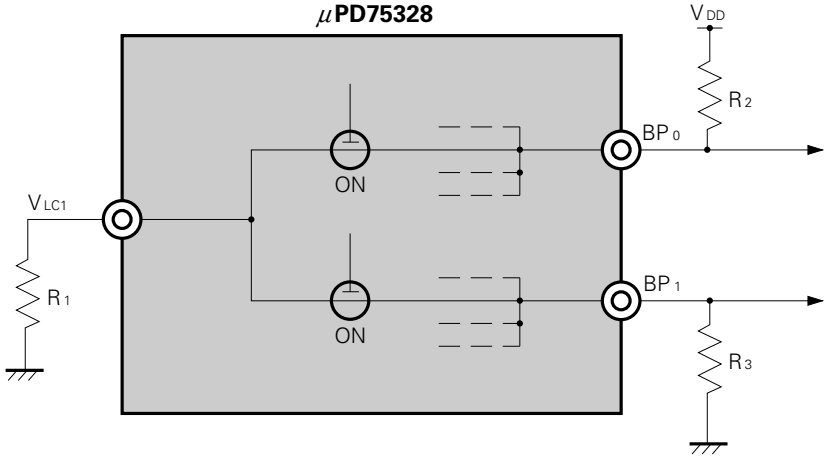
*1: Circles indicate schmidt trigger inputs.

2: When sharing the printed circut board with the μPD75P328, the NC pin must be connected to V_{DD}.

3: These pins are provided for future system expansion. At present, these pins are used only as pins P30 and P31.

4: For these display output, V_{LCX} indicated below are selected as the input source.
S12 to S31: V_{LC1}, COM0 to COM2: V_{LC2}, COM3: V_{LC0}
However, display output level varies depending on the particular display output and V_{LCX} external circuit.

Example: Since BP0-7 are connected to each other within the μPD75328 as shown in the diagram below, the output level of BP0-7 depends on the size of R_1, R_2 and R_3.

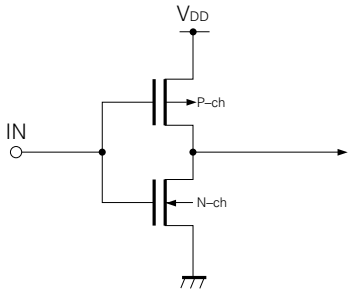


5: Step-down resistor network provided : Low level
Step-down resistor network not provided : High impedance

3.3 PIN INPUT/OUTPUT CIRCUITS

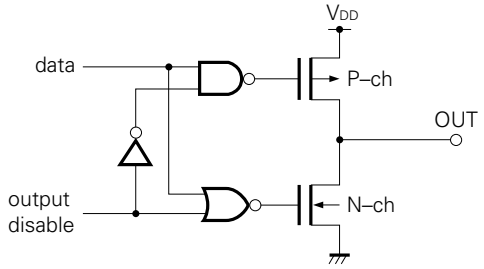
The following shows a simplified input/output circuit diagram for each pin of the μPD75328.

TYPE A (for TYPE E–B)



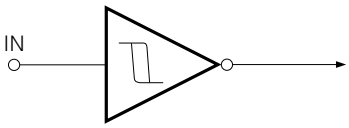
Input buffer of CMOS standard

TYPE D (for TYPE E–B, F–A)



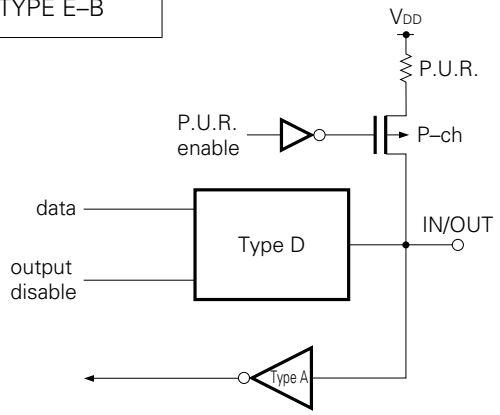
Push–pull output that can be set in a output high–impedance state (both P–ch and N–ch are off)

TYPE B



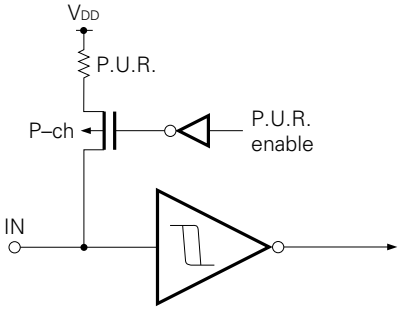
Schmitt trigger input with hysteresis characteristics

TYPE E–B



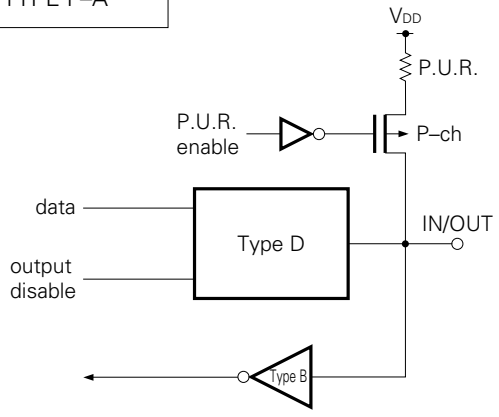
P.U.R. : Pull–Up Resistor

TYPE B–C



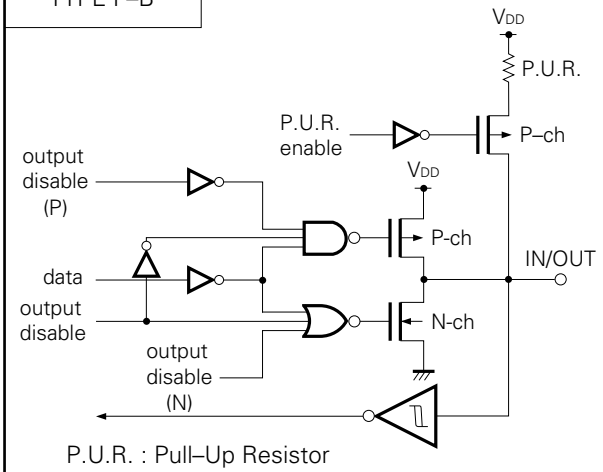
P.U.R. : Pull–Up Resistor
Schmitt trigger input with hysteresis characteristics

TYPE F–A



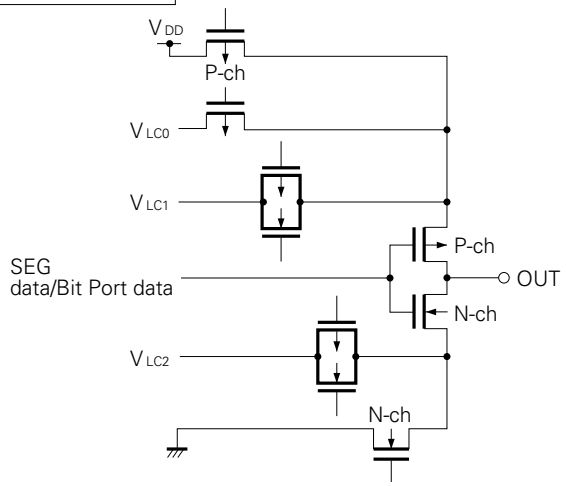
P.U.R. : Pull–Up Resistor

TYPE F–B

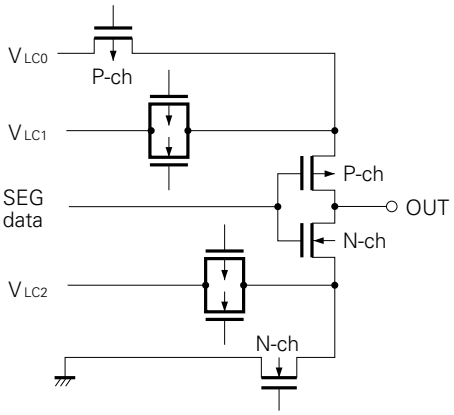


P.U.R. : Pull–Up Resistor

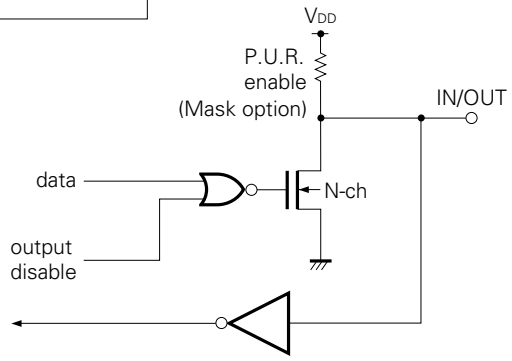
TYPE G–C



TYPE G–A



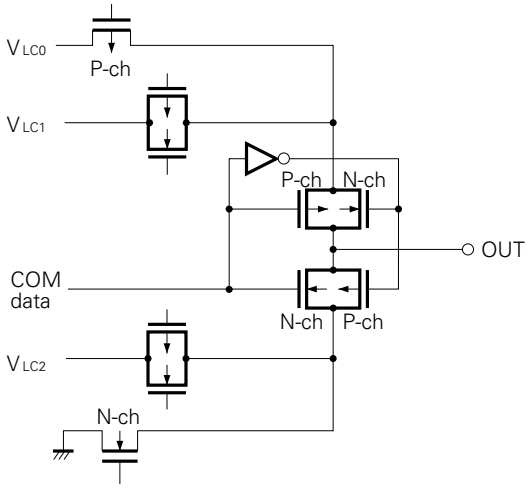
TYPE M



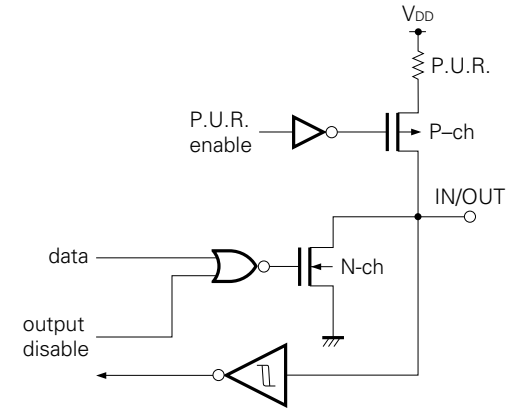
Middle voltage input buffer
(resistive voltage: +10 V)

P.U.R. : Pull–Up Resistor

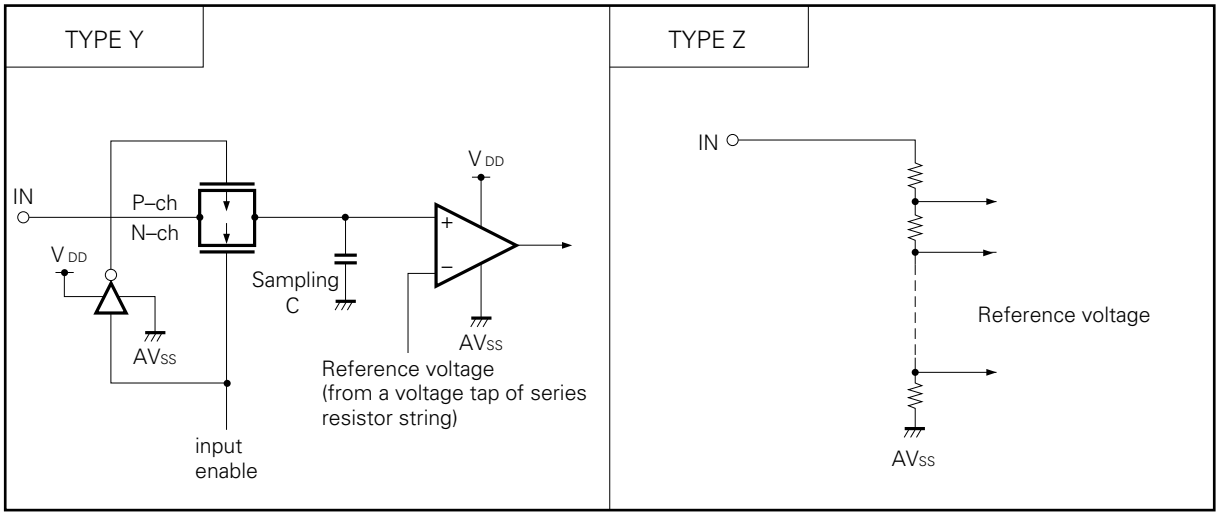
TYPE G–B



TYPE M–C



P.U.R. : Pull–Up Resistor



3.4 RECOMMENDED PROCESSING OF UNUSED PINS

Pin	Recommended Connections
P00/INT4	Connect to V_{SS}
P01/$\overline{SCK}$	Connect to V_{SS} or V_{DD}
P02/SO/SB0	
P03/SI/SB1	
P10/INT0-P12/INT2	Connect to V_{SS}
P13/TI0	
P20/PTO0	Input : Connect to V_{SS} or V_{DD} Output: Open
P21	
P22/PCL	
P23/BUZ	
P30-P33	
P40-P43	
P50-P53	
P60-P63	
P70-P73	
P80-P83	
S12-S23	Open
S24/BP0-S31/BP7	
COM0-COM3	
V_{LC0}-V_{LC2}	Connect to V_{SS}
BIAS	Connect to V_{SS} only when All of the V_{LC0}-V_{LC2} pins are unused, otherwise, open.
XT1	Connect to V_{SS} or V_{DD}
XT2	Open
AV_{REF}	Connect to V_{SS}
AV_{SS}	Connect to V_{SS}
AN0-AN5	Connect to V_{SS} or V_{DD}

3.5 SELECTION OF MASK OPTION

The following mask operations are available and can be specified for each pin.

Table 3-1 Mask Option Selection

Pin	Mask Option		Remarks
P40-P43, P50-P53	With pull-up resistor	Without pull-up resistor	Specification in bit units
V_{LC0}-V_{LC2} BIAS	With voltage dividing resistor for LCD drive power source	Without voltage dividing resistor for LCD drive power source	Specification in 4-bit units
XT1, XT2	With feed back resistor (when using the subsystem clock)	Without feed back resistor (when using the subsystem clock)	

3.6 NOTES ON USING THE P00/INT4, AND $\overline{\text{RESET}}$ PINS ★

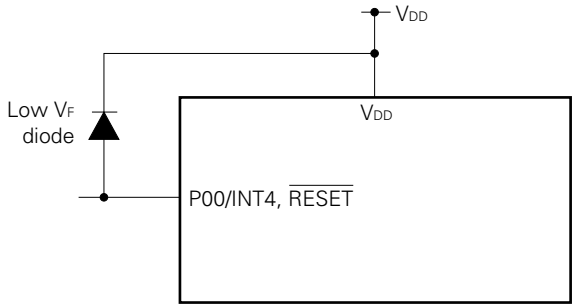
In addition to the functions described in Sections 3.1 and 3.2, an exclusive function for setting the test mode, in which the internal fuctions of the μPD75328 are tested, is provided to the P00/INT4 and $\overline{\text{RESET}}$ pins.

If a voltage exceeding V_{DD} is applied to either of these pins, the μPD75328 is put into test mode. Therefore, even when the μPD75328 is in normal operation, if noise exceeding the V_{DD} is input into any of these pins, the μPD75328 will enter the test mode, and this will cause problems for normal operation.

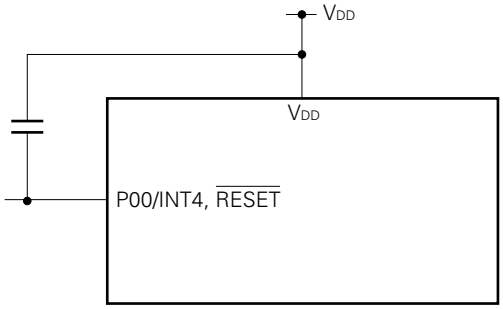
As an example, if the wiring to the P00/INT4 pin or the $\overline{\text{RESET}}$ pin is long, stray noise may be picked up and the above montioned problem may occur.

Therefore, all wiring to these pins must be made short enough to not pick up stray noise. If noise cannot be avoided, suppress the noise using a capacitor or diode as shown in the figure below.

- Connect a diode having a low V_F across P00/INT4 and $\overline{\text{RESET}}$, and V_{DD}.



- Connect a capacitor across P00/INT4 and $\overline{\text{RESET}}$, and V_{DD}.



4. MEMORY CONFIGURATION

- Program memory (ROM) ... 8064 words × 8 bits
  - 0000H, 0001H : Vector table to which address from which program is started is written after reset
  - 0002H-000BH : Vector table to which address from which program is started is written after interrupt
  - 0020H-007FH : Table area referenced by GETI instruction

- Data memory
  - Data area .... 512 words × 4 bits (000H–1FFH)
  - Peripheral hardware area .... 128 words × 4 bits (F80H–FFFH)

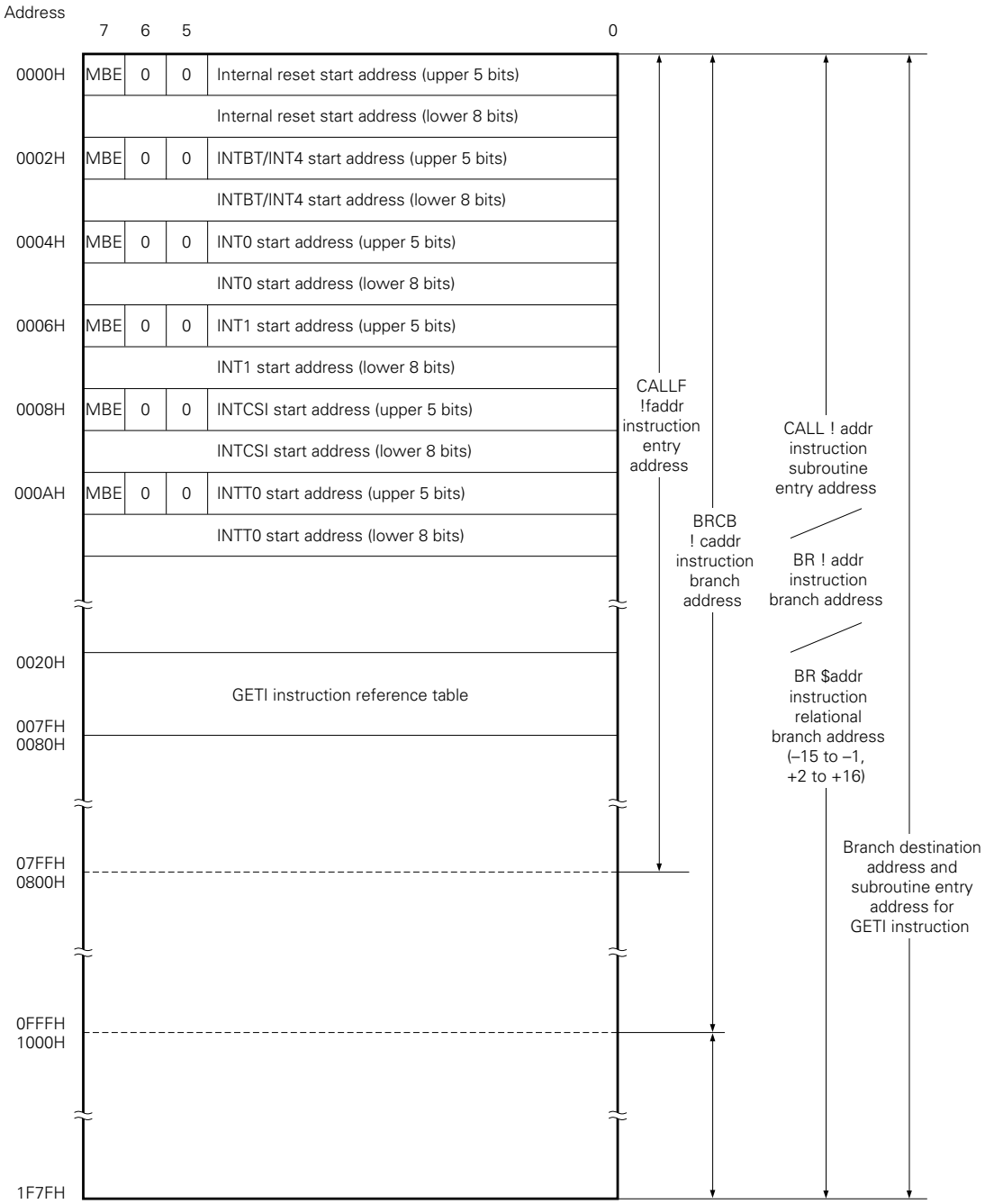


Fig. 4-1 Program Memory Map

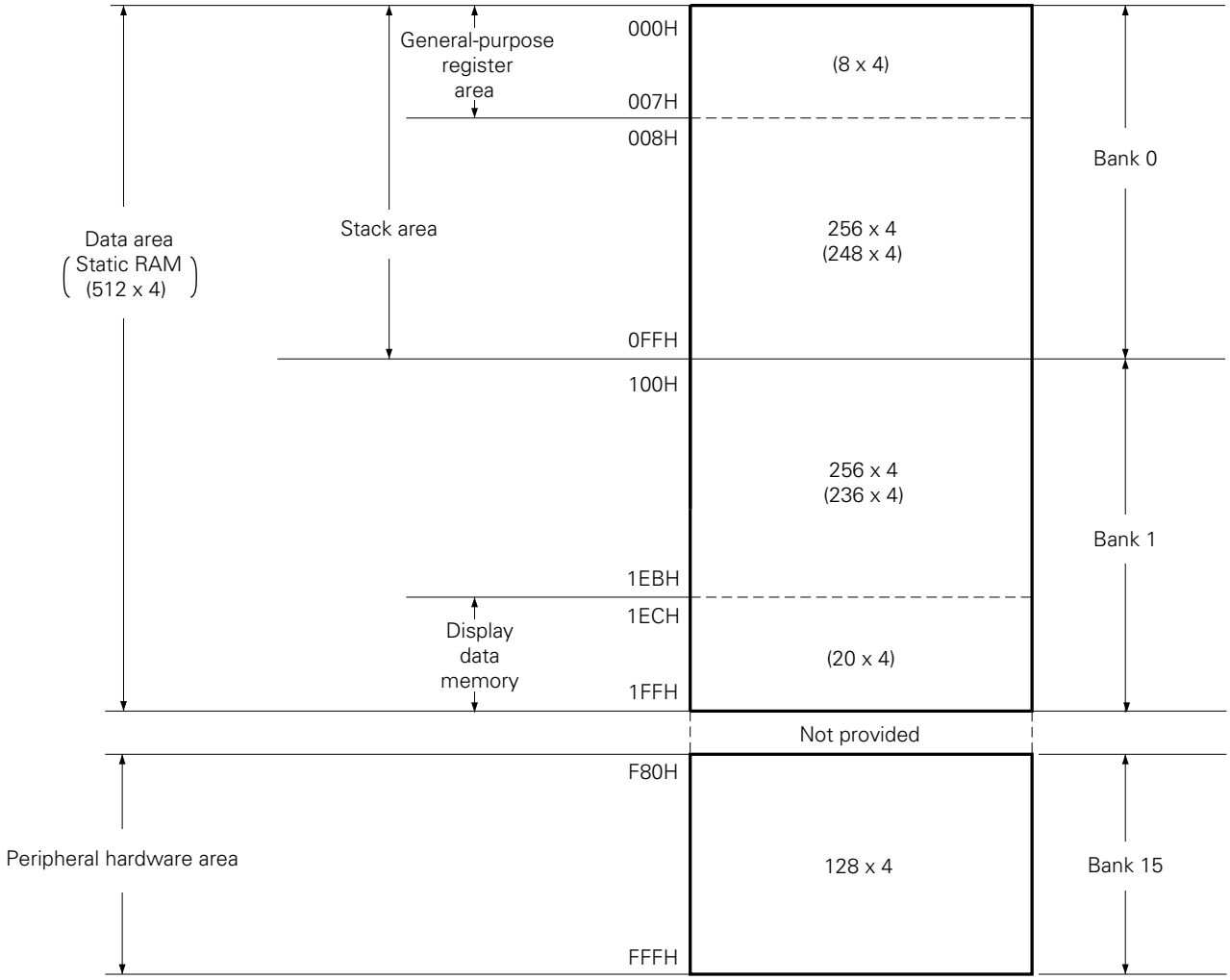


Fig. 4-2 Data Memory Map

5. PERIPHERAL HARDWARE FUNCTIONS

5.1 PORTS

I/O ports are classified into the following 4 kinds:

- CMOS input (PORT0, 1) : 8
- CMOS input/output (PORT2, 3, 6, 7, and 8) : 20
- CMOS output (BP0-BP7) : 8
- N-ch open-drain input/output (PORT4, 5) : 8

Total : 44

Table 5-1 Port Function

Port Name	Function	Operation and Feature	Remarks
PORT0	4-bit input	Can be always read or tested regardless of operation mode of multiplexed pin.	Multiplexed with INT4, $\overline{SCK}$, SO/SB0, and SI/SB1
PORT1			Multiplexed with INT0-INT2 and TI0
PORT2	4-bit Input/Output	Can be set in input or output mode in 4-bit units. Ports 6 and 7 are used in pairs to input/output data in 8-bit units.	Multiplexed with PTO0, PCL, and BUZ
PORT7			Multiplexed with KR4-KR7
PORT8			—
PORT3		Can be set in input or output mode in 1-bit units.	Multiplexed with LCDCL and SYNC
PORT6			Multiplexed with KR0-KR3
PORT4 * PORT5 *	4-bit Input/Output (N-ch open-drain, 10 V)	Can be set in input or output mode in 4-bit units. Ports 4 and 5 are used in pairs to input/output data in 8-bit units.	Can be connected to a pull-up resistor in 1-bit units by using mask option.
BP0-BP7	1-bit output	Output data in 1-bit units. Can be used as LCD drive segment output pins S24-S31 through software.	—

*: Can directly drive LED.

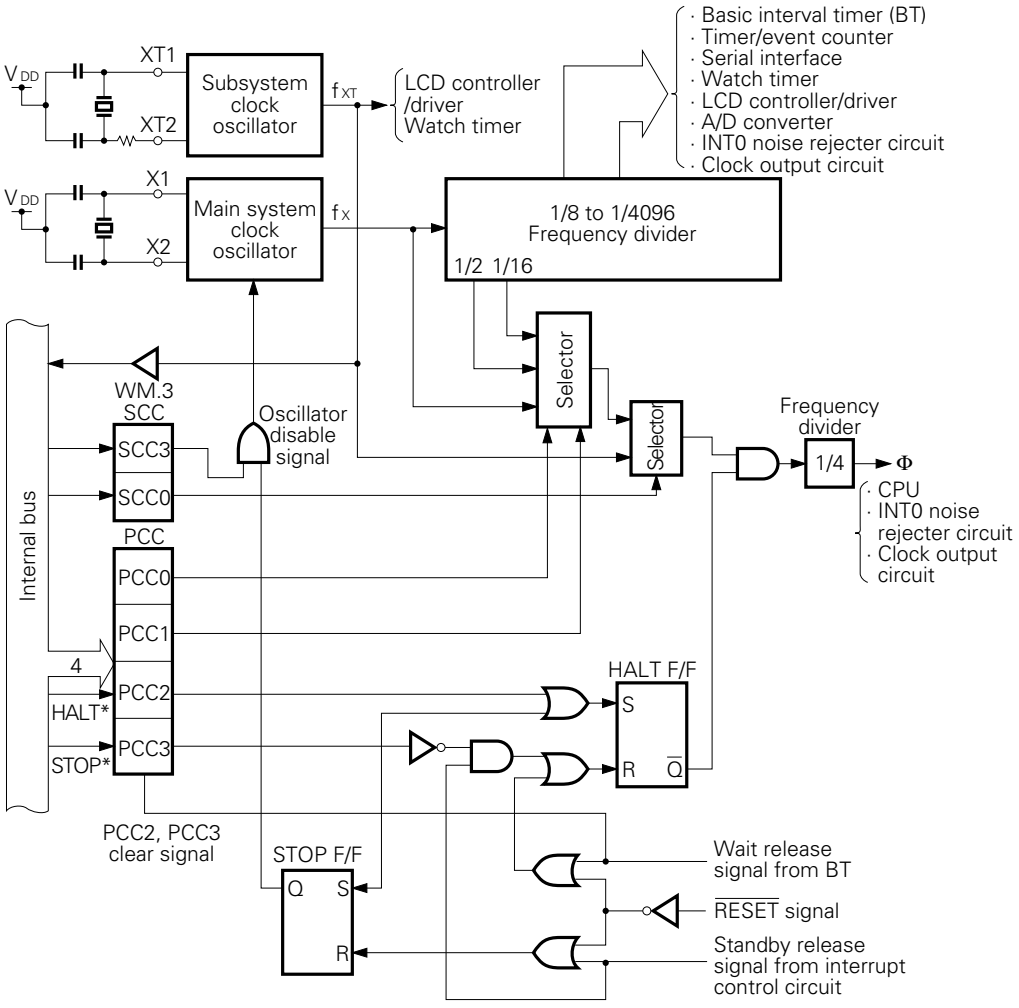
5.2 CLOCK GENERATOR CIRCUIT

The operation of the clock generator circuit is determined by the processor clock control regiser (PPC) and system clock control register (SCC).

This circuit can generate two types of clocks: main system clock and subsystem clock.

In addition, it can also change the instruction execution time.

- 0.95 μs, 1.91 μs, 15.3 μs (main system clock: 4.19 MHz)
- 122 μs (subsystem clock: 32.768 kHz)



*: instruction execution.

Remarks 1: f_X = Main system clock frequency

2: f_{XT} = Subsystem clock frequency

3: Φ = CPU clock

4: PCC: Processor clock control register

5: SCC: System clock control register

6: One clock cysle (t_{CY}) of Φ is one machine cycle of an instruction. For t_{CY}, refer to AC characteristics in 10. ELECTRICAL SPECIFICATIONS. ★

Fig. 5-1 Clock Generator Block Diagram

5.3 CLOCK OUTPUT CIRCUIT

The clock output circuit outputs clock pulse from the P22/PCL pin. This clock pulse is used for the remote control output, peripheral LSIs, etc.

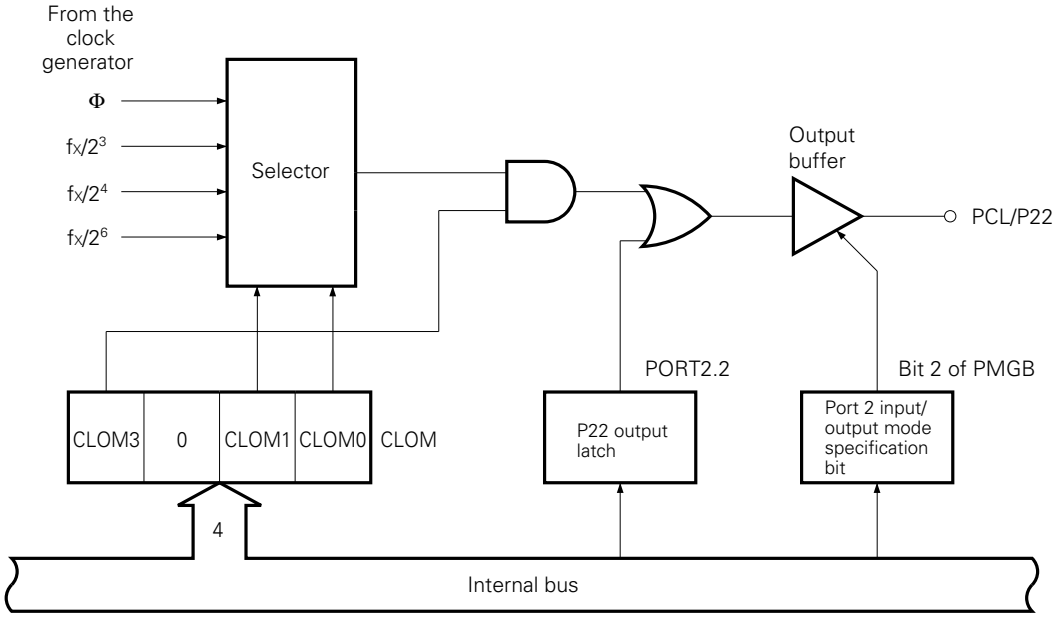


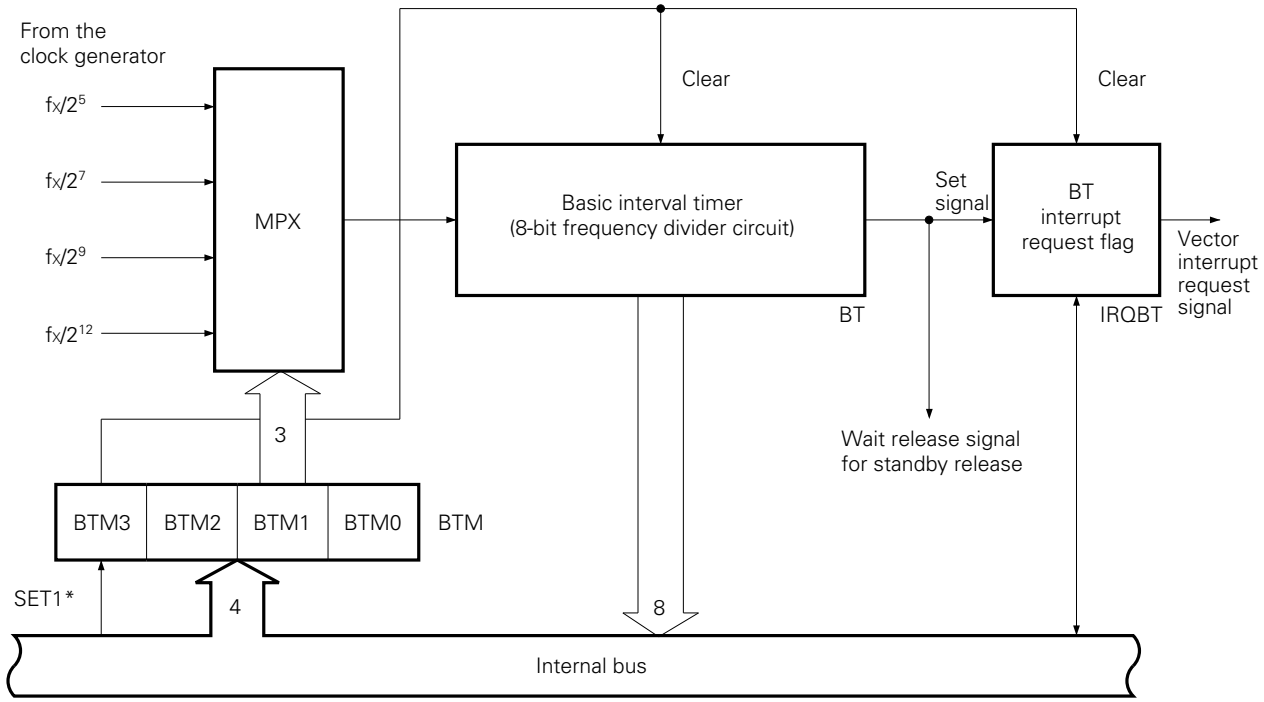
Fig. 5-2 Clock Output Circuit Configuration

Remarks: A measures to prevent outputting narrow width pulse when selecting clock output enable/disable is taken.

5.4 BASIC INTERVAL TIMER

The μPD75328 is provided with the 8-bit basic interval timer. The basic interval timer has these functions:

- Interval timer operation which generates a reference time interrupt
- Watchdog timer application which detects a program runaway
- Selects the wait time for releasing the standby mode and counts the wait time
- Reads out the count value



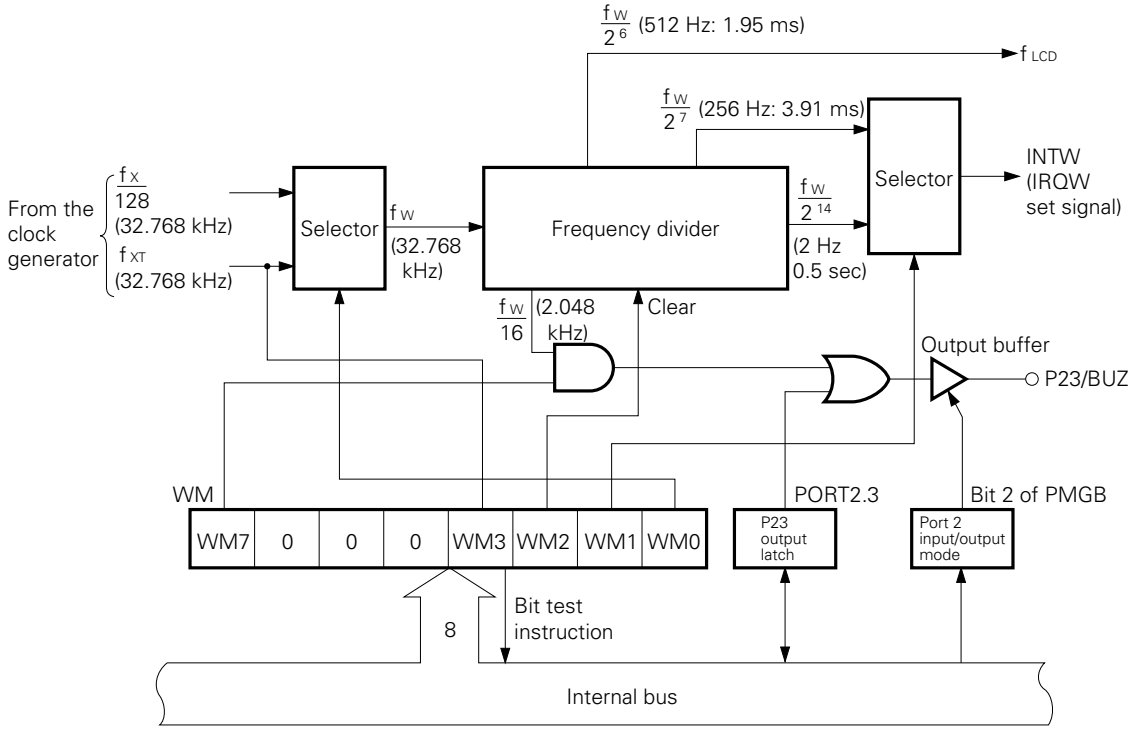
Remarks : *: Instruction execution

Fig. 5-3 Basic Interval Timer Configuration

5.5 WATCH TIMER

The μPD75328 has a built-in 1-ch watch timer. The watch timer is configured as shown in Fig. 5-4.

- Sets the test flag (IRQW) with 0.5 sec interval.
  The standby mode can be released by IRQW.
- 0.5 second interval can be generated either from the main system clock or subsystem clock.
- Time interval can be advanced to 128 times faster (3.91 ms) by setting the fast mode. This is convenient for program debugging, test, etc.
- Fixed frequency (2.048 kHz) can be output to the P23/BUZ pin. This can be used for beep and system clock frequency trimming.
- The frequency divider circuit can be cleared so that zero second watch start is possible.



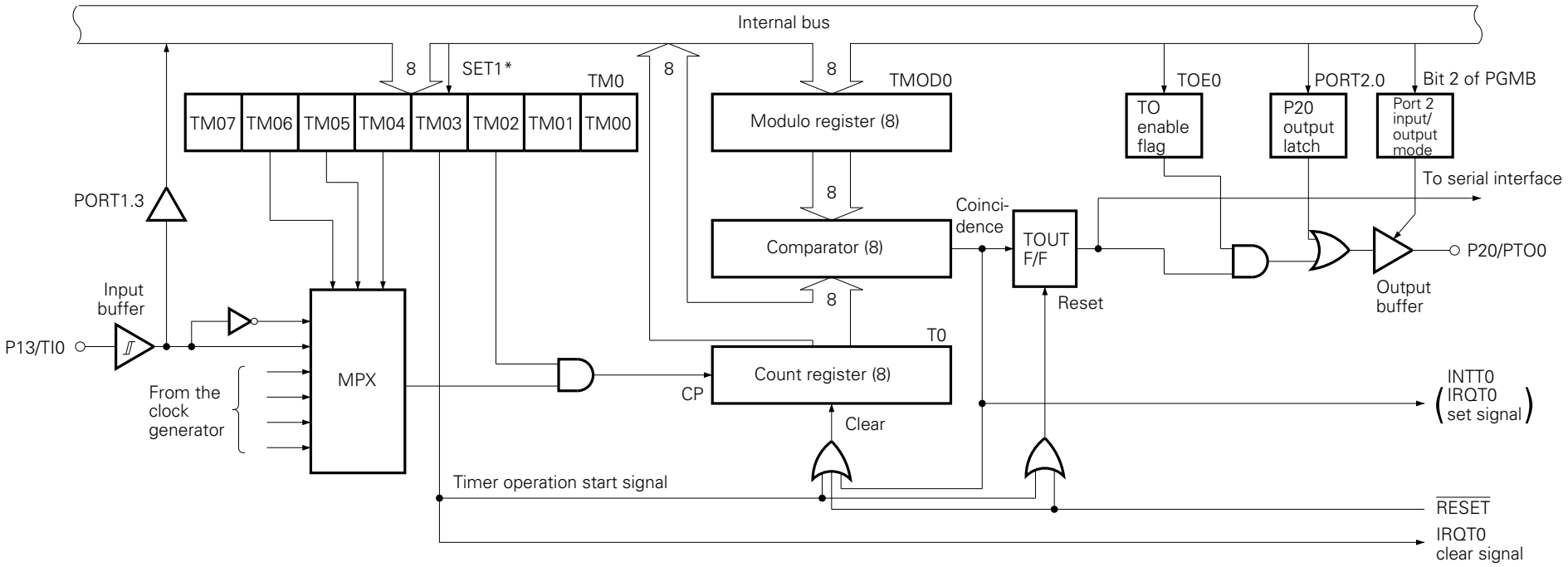
( ) is for fx = 4.194304 MHz, fxT = 32.768 kHz.

Fig. 5-4 Watch Timer Block Diagram

5.6 TIMER/EVENT COUNTER

The μPD75328 has a built-in 1-ch timer/event counter. The timer/even counter has these functions:

- Programmable interval timer operation
- Outputs square-wave signal of an arbitrary frequency to the PTO0 pin.
- Event counter operation
- Divides the TI0 pin input in N and outputs to the PTO0 pin (frequency divider operation).
- Supplies serial shift clock to the serial interface circuit.
- Count condition read out function



*:Instruction execution

Fig. 5-5 Timer/Event Counter Block Diagram

5.7 SERIAL INTERFACE

The μPD75328 is equipped with an 8-bit clocked serial interface that operates in the following four modes:

- Operation stop mode
- Three-line serial I/O mode
- Two-line serial I/O mode
- SBI mode (serial bus interface mode)

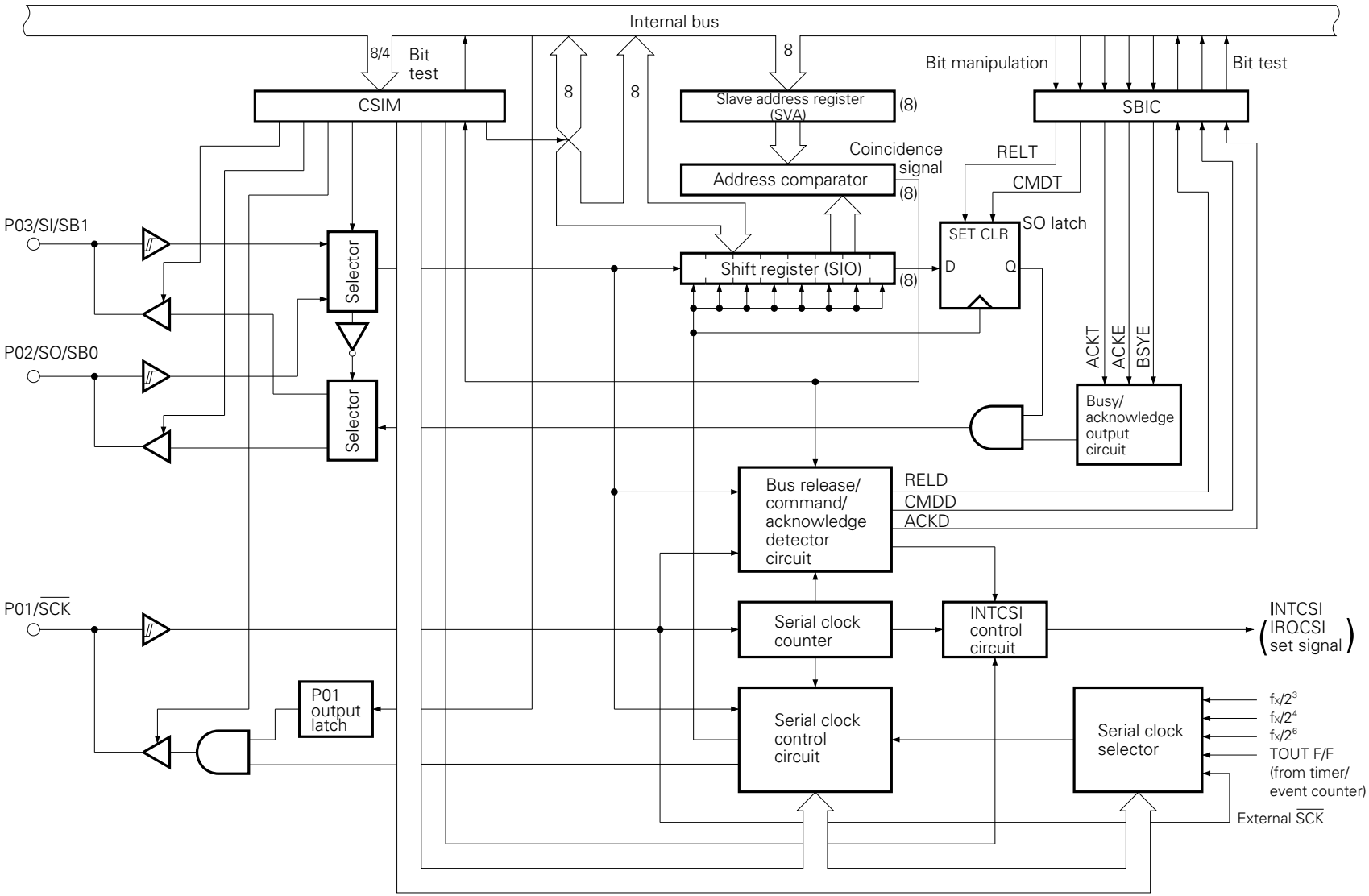


Fig. 5-6 Serial Interface Block Diagram

5.8 LCD CONTROLLER/DRIVER

The μPD75328 is provided with a display controller that generates segment and common signals and a segment driver and a common driver that can directly drive an LCD panel. These LCD controller and drivers have the following functions:

- Generate segment and common signals by automatically reading the display data memory by means of DMA
- Five display modes selectable
  - Static
  - 1/2 duty (divided by 2), 1/2 bias
  - 1/3 duty (divided by 3), 1/2 bias
  - 1/3 duty (divided by 3), 1/3 bias
  - 1/4 duty (divided by 4), 1/3 bias
- Four types of frame frequencies selectable in each display mode
- Up to 20 segment signals (S12-S31) and four common signals (COM0-COM3) can be output.
- Four segment signal output pins (S24-S27, S28-S31) can be used as an output port (BP0-BP3, BP4-BP7).
- Dividing resistor for LCD driving power source can be provided (by mask option).
  - All bias modes and LCD drive voltages can be used.
  - Current flowing to dividing resistor can be cut when display is off.
- Display data memory not used for display can be used as ordinary data memory.
- Can also operate on subsystem clock.

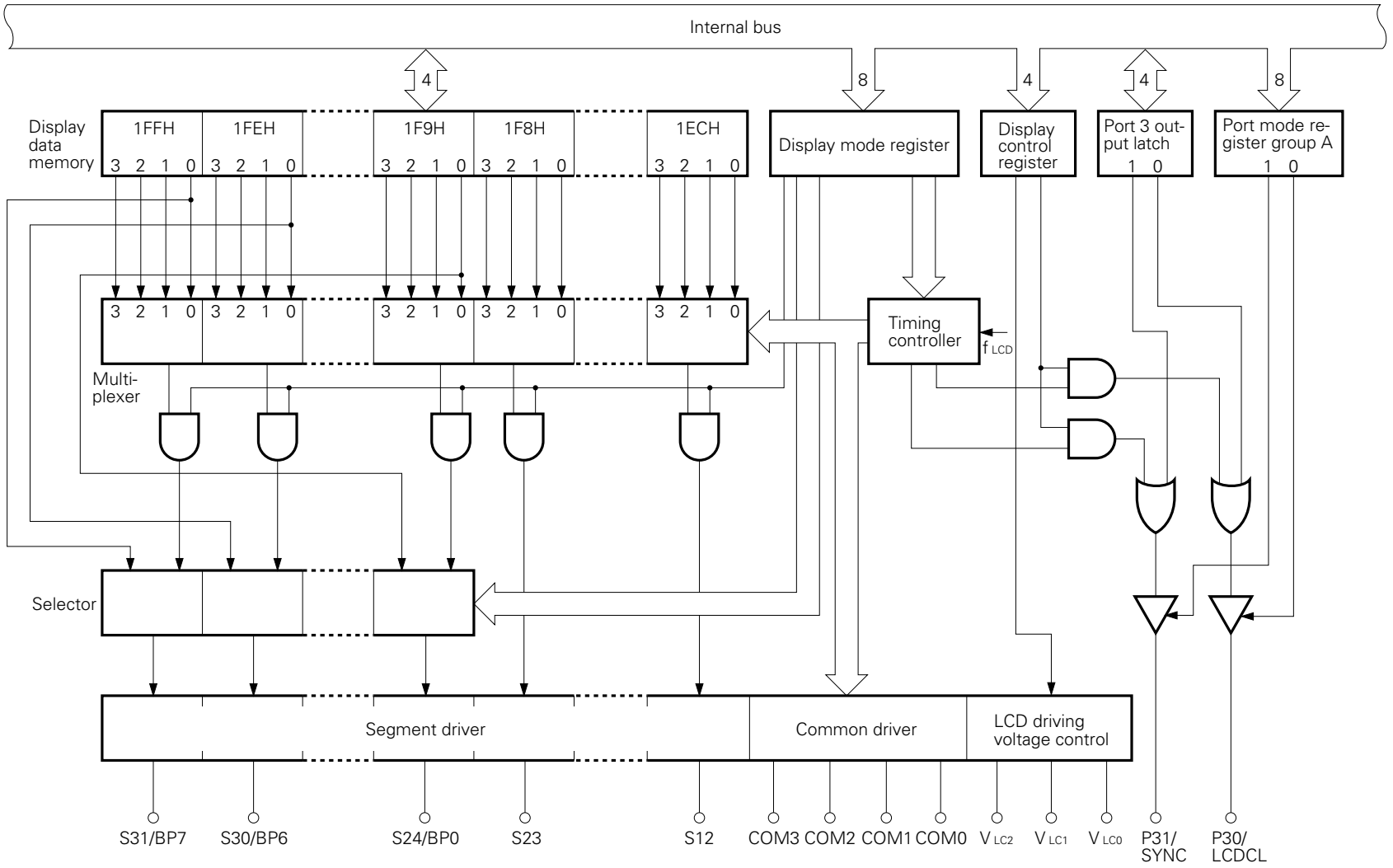


Fig. 5-7 LCD Controller/Driver Block Diagram

5.9 A/D CONVERTER

The μPD75328 is provided with an 8-bit resolution analog-to-digital (A/D) converter with six channels of analog inputs (AN0-AN5).

This A/D converter is of a successive approximation type.

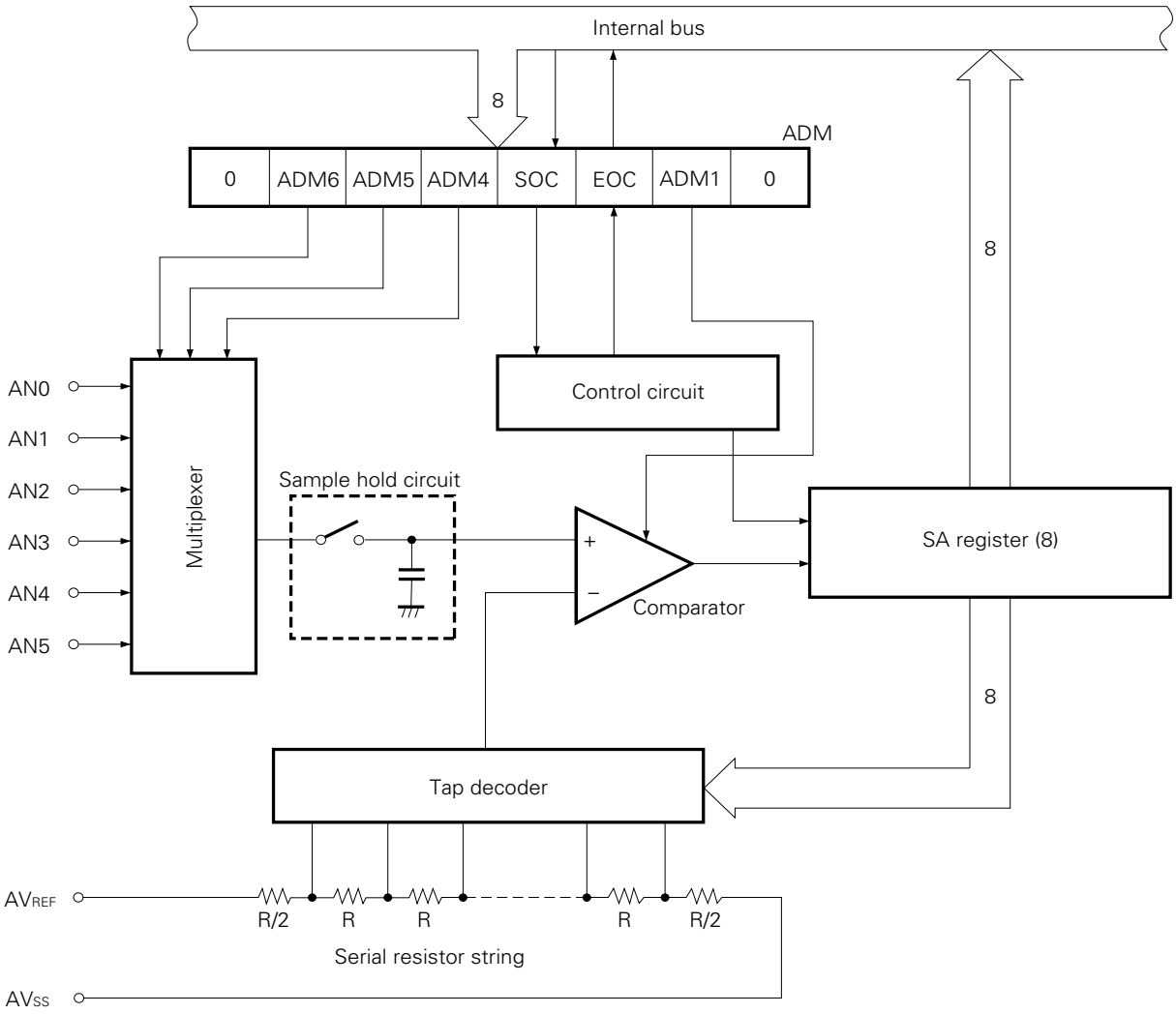
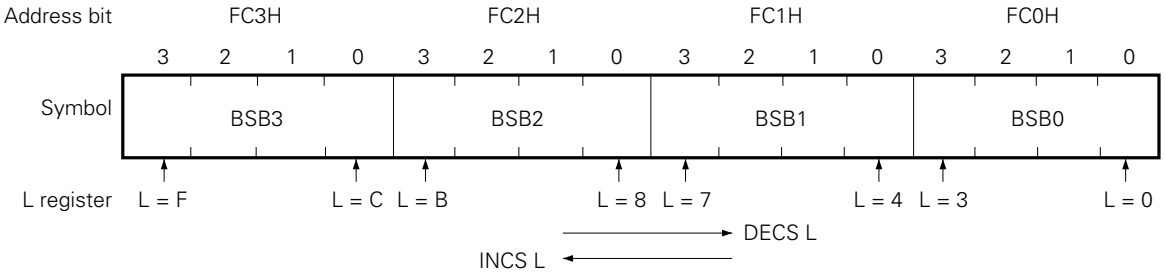


Fig. 5-8 Block Diagram of A/D Converter

5.10 BIT SEQUENTIAL BUFFER .... 16 BITS

The bit sequential buffer is a data memory specifically provided for bit manipulation. With this buffer, addresses and bit specifications can be sequentially up-dated in bit manipulation operation. Therefore, this buffer is very useful for processing long data in bit units.



Remarks: For the pmem.@L addressing, the specification bit is shifted according to the L register.

Fig. 5-9 Bit Sequential Buffer Format

6. INTERRUPT FUNCTIONS

The μPD75328 has 6 different interrupt sources and multiplexed interrupt with priority order.

In addition to that, the μPD75328 is also provided with two types of test sources, of which INT2 has two types of edge detection testable inputs.

The interrupt control circuit of the μPD75328 has these functions:

- Hardware controlled vector interrupt function which can control whether or not to accept an interrupt by using the interrupt flag (IExxx) and interrupt master enable flag (IME).
- The interrupt start address can be arbitrarily set.
- Interrupt request flag (IRQxxx) test function (an interrupt generation can be confirmed by means of software).
- Standby mode release (Interrupts to be released can be selected by the interrupt enable flag).

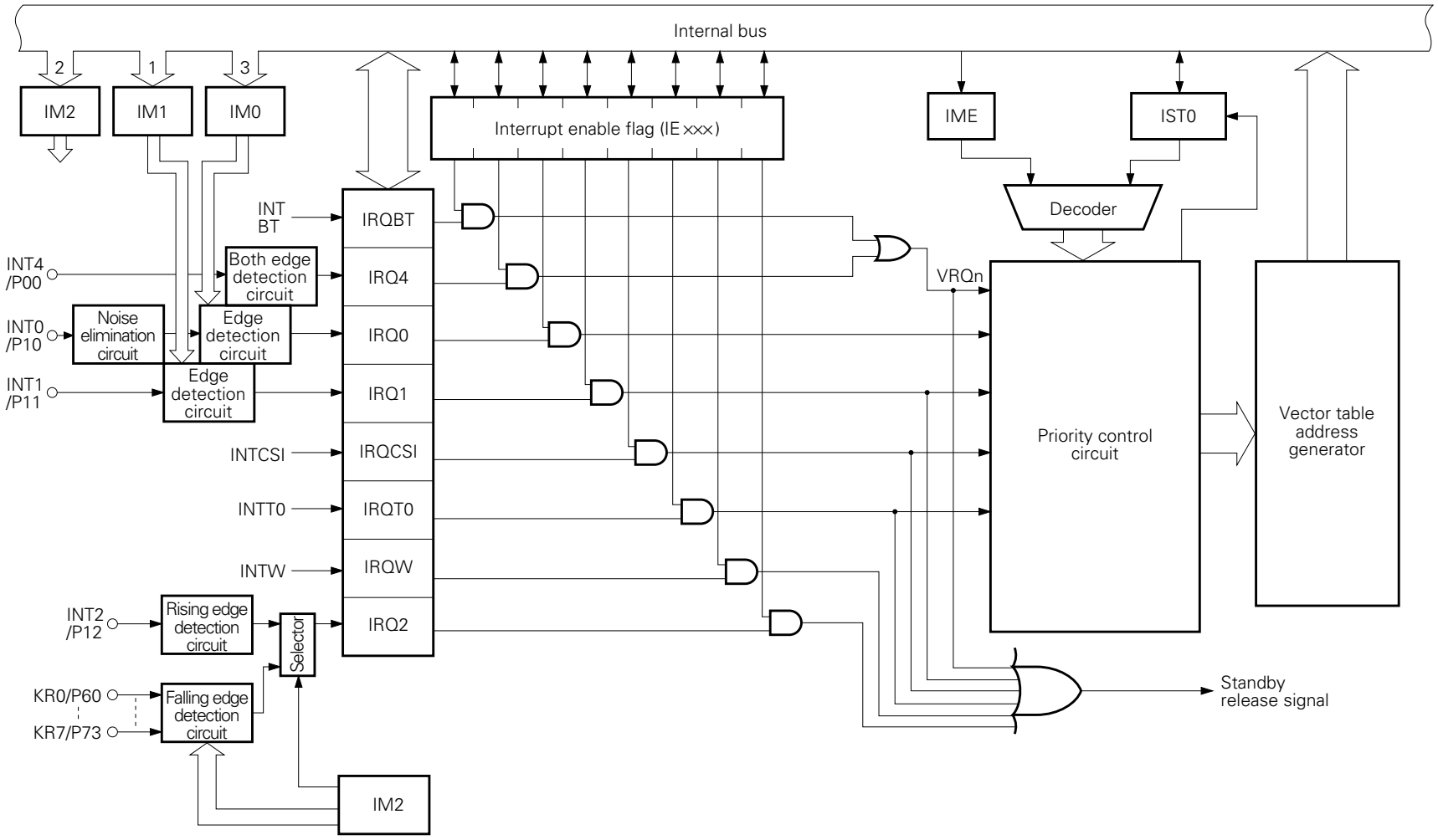


Fig. 6-1 Interrupt Control Block Diagram

7. STANDBY FUNCTIONS

The μPD75328 has two different standby modes (STOP mode and HALT mode) to reduce the power consumption while waiting for program execution.

Table 7-1 Each Status in Standby Mode

Item \ Mode		STOP Mode	HALT Mode
Setting Instruction		STOP instrtuction	HALT instruction
System Clock for Setting		Can be set only when operating on the main system clock	Can be set either with the main system clock or the subsystem clock
Operation Status	Clock Generator	Only the main system clock stops its operation.	Only the CPU clock Φ stops its operation. (oscillation continues)
	Basic Interval Timer	No operation	Can operate only when main system clock oscillates (Sets IRQBT at reference time interval)
	Serial Interface	Can operate only when the external $\overline{SCK}$ input is selected for the serial clock	Can operate only when main system clock oscillates, or when external $\overline{SCK}$ input is selected as serial clock
	Timer/Event Counter	Can operate only when the TI0 pin input is selected for the count clock	Can operate only when main system clock oscillates, or when TI0 pin input is selected as count clock
	Watch Timer	Can operate when f_{XT} is selected as the count clock	Can operate
	LCD controller	Can operate only when f_{XT} is selected as LCDCL	Can operate
	A/D Convertor	No operation	Can operate only when the main system clock is operating.
	External Interrupt	INT1, INT2, and INT4 can operate. Only INT0 can not operate.	
	CPU	No operation	
Release Signal		An interrupt request signal from a hardware whose operation is enabled by the interrupt enable flag or the $\overline{RESET}$ signal input	An interrupt request signal from a hardware whose operation is enabled by the interrupt enable flag or the $\overline{RESET}$ signal input

8. RESET FUNCTION

When the $\overline{\text{RESET}}$ signal is input, the μPD75328 is reset and each hardware is initialized as indicated in Table 8-1. Fig. 8-1 shows the reset operation timing.

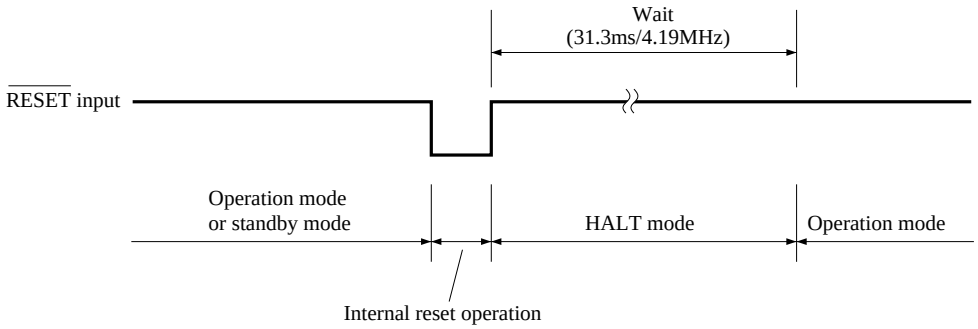


Fig. 8-1 Reset Operation by $\overline{\text{RESET}}$ Input

Table 8-1 Status of Each Hardware after Reset (1/2)

Hardware		$\overline{\text{RESET}}$ Input in Standby Mode	$\overline{\text{RESET}}$ Input during Operation
Program Counter (PC)		The contents of the lower 5 bits of address 0000H of the program memory are set to PC12-8, and the contents of address 0001H are set to PC7-0.	The contents of the lower 5 bits of address 0000H of the program memory are set to PC12-8, and the contents of address 0001H are set to PC7-0.
PSW	Carry Flag (CY)	Retained	Undefined
	Skip Flag (SK0-2)	0	0
	Interrupt Status Flag (IST0)	0	0
	Bank Enable Flag (MBE)	The contents of bit 7 of address 0000H of the program memory are set to MBE.	The contents of bit 7 of address 0000H of the program memory are set to MBE.
Stack Pointer (SP)		Undefined	Undefined
Data Memory (RAM)		Retained *1	Undefined
General-Purpose Register (X, A, H, L, D, E, B, C)		Retained	Undefined
Bank Selection Register (MBS)		0	0
Basic Interval Timer	Counter (BT)	Undefined	Undefined
	Mode Register (BTM)	0	0
Timer/Event Counter	Counter (T0)	0	0
	Module Register (TMOD0)	FFH	FFH
	Mode Register (TM0)	0	0
	TOE0, TOUT F/F	0, 0	0, 0
Watch Timer	Mode Register (WM)	0	0

Table 8-1 Status of Each Hardware after Reset (2/2)

Hardware		$\overline{\text{RESET}}$ Input in Standby Mode	$\overline{\text{RESET}}$ Input during Operation
Serial Interface	Shift Register (SIO)	Retained	Undefined
	Operation Mode Register (CSIM)	0	0
	SBI Control Register (SBIC)	0	0
	Slave Address Register (SVA)	Retained	Undefined
Clock Generator, Clock Output Circuit	Processor Clock Control Register (PCC)	0	0
	System Clock Control Register (SCC)	0	0
	Clock Output Mode Register (CLOM)	0	0
LCD Controller	Display Mode Register (LCMD)	0	0
	Display Control Register (LCDC)	0	0
A/D Converter	Mode Regiseter (ADM), EOC	04H (EOC = 1)	04H (EOC = 1)
	SA Register	7FH	7FH
Interrupt Function	Interrupt Request Flag (IRQxxx)	Reset (0)	Reset (0)
	Interrupt Enable Flag (IExxx)	0	0
	Interrupt Master Enable Flag (IME)	0	0
	INT0, INT1, INT2 Mode Registers (IM0, 1, 2)	0, 0, 0	0, 0, 0
Digital Port	Output Buffer	Off	Off
	Output Latch	Clear (0)	Clear (0)
	Input/Output Mode Register (PMGA, B, C)	0	0
	Pull-Up Resistor Specification Register (POGA, B)	0	0
Pin States	P00-P03, P10-P13, P20-P23, P30-P33, P60-P63, P70-P73, P80-P83	Input	Input
	P40-P43, P50-P53	• Internal pull-up resistors ... High level • Open drain ... High impedance	Same as at left
	S12-S23, COM0-COM3	*2	*2
	BIAS	• Internal step-down resistors ... Low level • External step-down resistors ... High impedance	Same as at left
Bit Sequential Buffer (BSB0-3)		Retained	Specified

***1:** Data of address 0F8H to 0FDH of the data memory becomes undefined when a $\overline{\text{RESET}}$ signal is input.

2: Select V_{LCX} as shown below as the input source for each display output.

S12-31 : V_{LC1}

COM0-2 : V_{LC2}

COM3 : V_{LC0}

However, the level of each display output varies according to the display output and the external circuit for V_{LCX}.

9. INSTRUCTION SET

(1) Operand representation and description

Describe one or more operands in the operand field of each instruction according to the operand representation and description methods of the instruction (for details, refer to RA75X Assembler Package User's Manual - Language (EEU-730)). With some instructions, only one operand should be selected from several operands. The uppercase characters, +, and – are keywords and must be described as is.

Describe an appropriate numeric value or label as immediate data.

Representation	Description
reg reg1	X, A, B, C, D, E, H, L X, B, C, D, E, H, L
rp rp1 rp2	XA, BC, DE, HL BC, DE, HL BC, DE
rpa rpa1	HL, DE, DL DE, DL
n4 n8	4-bit immediate data or label 8-bit immediate data or label
mem bit	8-bit immediate data or label 2-bit immediate data or label
fmem pmem	FB0H to FBFH,FF0H to FFFH immediate data or label FC0H to FFFH immediate data or label
addr caddr faddr	0000H to 1F7FH immediate data or label 12-bit immediate data or label 11-bit immediate data or label
taddr	20H to 7FH immediate data (where bit0 = 0) or label
PORTn IExxx MBn	PORT0 to PORT8 IEBT, IECSI, IET0, IE0, IE1, IE2, IE4, IEW MB0, MB1, MB15

(2) Legend of operation field

A	:	A register; 4-bit accumulator
B	:	B register; 4-bit accumulator
C	:	C register; 4-bit accumulator
D	:	D register; 4-bit accumulator
E	:	E register; 4-bit accumulator
H	:	H register; 4-bit accumulator
L	:	L register; 4-bit accumulator
X	:	X register; 4-bit accumulator
XA	:	Register pair (XA); 8-bit accumulator
BC	:	Register pair (BC); 8-bit accumulator
DE	:	Register pair (DE); 8-bit accumulator
HL	:	Register pair (HL); 8-bit accumulator
PC	:	Program counter
SP	:	Stack pointer
CY	:	Carry flag; or bit accumulator
PSW	:	Program status word
MBE	:	Memory bank enable flag
PORTn	:	Port n (n = 0 to 8)
IME	:	Interrupt mask enable flag
IExxx	:	Interrupt enable flag
MBS	:	Memory bank selector register
PCC	:	Processor clock control register
·	:	Delimiter of address and bit
(xx)	:	Contents addressed by xx
xxH	:	Hexadecimal data

(3) Symbols in addressing area field

*1	MB = MBE · MBS (MBS = 0, 1, 15)	Data memory addressing
*2	MB = 0	
*3	MBE = 0 : MB = 0 (00H-7FH) MB = 15 (80H-FFH) MBE = 1 : MB = MBS (MBS = 0, 1, 15)	
*4	MB = 15, fmem = FB0H-FBFH, FF0H-FFFH	
*5	MB = 15, pmem = FC0H-FFFH	
*6	addr = 000H-1F7FH	Program memory addressing
*7	addr = (Current PC) – 15 to (Current PC) – 1 (Current PC) + 2 to (Current PC) + 16	
*8	caddr = 0000H-0FFFH (PC_{12} = 0) or 1000H-1F7FH (PC_{12} = 1)	
*9	faddr = 0000H-07FFH	
*10	taddr = 0020H-007FH	

Remarks 1: MB indicates memory bank that can be accessed.

2: In *2, MB = 0 regardless of MBE and MBS.

3: In *4 and *5, MB = 15 regardless of MBE and MBS.

4: *6 to *10 indicate areas that can be addressed.

(4) Machine cycle field

In this field, S indicates the number of machine cycles required when an instruction having a skip function skips. The value of S varies as follows:

- When no instruction is skipped ..... S = 0
- When 1-byte or 2-byte instruction is skipped ..... S = 1
- When 3-byte instruction (BR ! addr or CALL ! addr) is skipped ..... S = 2

Note : The GETI instruction is skipped in one machine cycle.

One machine cycle equals to one cycle of the CPU clock Φ, ($=t_{CY}$), and can be changed in three steps depending on the setting of the processor clock control register (PCC).

Instructions	Mnemonics	Operand	Bytes	Machine Cycles	Operation	Addressing Area	Skip Conditions
Transfer	MOV	A, #n4	1	1	A ← n4		String effect A
		reg1, #n4	2	2	reg1 ← n4		
		XA, #n8	2	2	XA ← n8		String effect A
		HL, #n8	2	2	HL ← n8		String effect B
		rp2, #n8	2	2	rp2 ← n8		
		A, @HL	1	1	A ← (HL)	*1	
		A, @rpa1	1	1	A ← (rpa1)	*2	
		XA, @HL	2	2	XA ← (HL)	*1	
		@HL, A	1	1	(HL) ← A	*1	
		@HL, XA	2	2	(HL) ← XA	*1	
		A,mem	2	2	A ← (mem)	*3	
		XA, mem	2	2	XA ← (mem)	*3	
		mem, A	2	2	(mem) ← A	*3	
		mem, XA	2	2	(mem) ← XA	*3	
		A, reg	2	2	A ← reg		
		XA, rp	2	2	XA ← rp		
		reg1, A	2	2	reg1 ← A		
		rp1, XA	2	2	rp1 ← XA		
	XCH	A, @HL	1	1	A ↔ (HL)	*1	
		A, @rpa1	1	1	A ↔ (rpa1)	*2	
		XA, @HL	2	2	XA ↔ (HL)	*1	
		A, mem	2	2	A ↔ (mem)	*3	
		XA, mem	2	2	XA ↔ (mem)	*3	
		A, reg1	1	1	A ↔ reg1		
		XA, rp	2	2	XA ↔ rp		
	MOVT	XA, @PCDE	1	3	XA ← $(PC_{12-8}+DE)_{ROM}$		
		XA, @PCXA	1	3	XA ← $(PC_{12-8}+XA)_{ROM}$		
Arithmetic Operation	ADDS	A, #n4	1	1+S	A ← A+n4		carry
		A, @HL	1	1+S	A ← A+(HL)	*1	carry
	ADDC	A, @HL	1	1	A, CY ← A+(HL)+CY	*1	
	SUBS	A, @HL	1	1+S	A ← A-(HL)	*1	borrow
	SUBC	A, @HL	1	1	A, CY ← A-(HL)-CY	*1	
	AND	A, #n4	2	2	A ← A ∧ n4		
		A, @HL	1	1	A ← A ∧ (HL)	*1	
	OR	A, #n4	2	2	A ← A ∨ n4		
		A, @HL	1	1	A ← A ∨ (HL)	*1	
	XOR	A, #n4	2	2	A ← A ∨̄ n4		
		A, @HL	1	1	A ← A ∨̄ (HL)	*1	
Accumulator Manipulation	RORC	A	1	1	CY ← A_0, A_3 ← CY, A_{n-1} ← A_n		
	NOT	A	2	2	A ← $\overline{A}$		

Instructions	Mnemonics	Operand	Bytes	Machine Cycles	Operation	Addressing Area	Skip Conditions
Increment/ Decrement	INCS	reg	1	1+S	reg ← reg+1		reg = 0
		@HL	2	2+S	(HL) ← (HL)+1	*1	(HL) = 0
		mem	2	2+S	(mem) ← (mem)+1	*3	(mem) = 0
	DECS	reg	1	1+S	reg ← reg-1		reg = FH
Compare	SKE	reg, #n4	2	2+S	Skip if reg = n4		reg = n4
		@HL, #n4	2	2+S	Skip if (HL) = n4		*1(HL) = n4
		A, @HL	1	1+S	Skip if A = (HL)	*1	A = (HL)
		A, reg	2	2+S	Skip if A = reg		A = reg
Carry flag Manipulation	SET1	CY	1	1	CY ← 1		
	CLR1	CY	1	1	CY ← 0		
	SKT	CY	1	1+S	Skip if CY = 1		CY = 1
	NOT1	CY	1	1	CY ← $\overline{CY}$		
Memory/ Bit Manipulation	SET1	mem.bit	2	2	(mem.bit) ← 1	*3	
		fmem.bit	2	2	(fmem.bit) ← 1	*4	
		pmem.@L	2	2	($pmem_{7-2}$ + L_{3-2}.bit(L_{1-0})) ← 1	*5	
		@H+mem.bit	2	2	(H + mem_{3-0}.bit) ← 1	*1	
	CLR1	mem.bit	2	2	(mem.bit) ← 0	*3	
		fmem.bit	2	2	(fmem.bit) ← 0	*4	
		pmem.@L	2	2	($pmem_{7-2}$ + L_{3-2}.bit(L_{1-0})) ← 0	*5	
		@H+mem.bit	2	2	(H+mem_{3-0}.bit) ← 0	*1	
	SKT	mem.bit	2	2+S	Skip if (mem.bit) = 1	*3	(mem.bit) = 1
		fmem.bit	2	2+S	Skip if (fmem.bit) = 1	*4	(fmem.bit) = 1
		pmem.@L	2	2+S	Skip if ($pmem_{7-2}$+L_{3-2}.bit (L_{1-0})) = 1	*5	(pmem.@L) = 1
		@H+mem.bit	2	2+S	Skip if (H + mem_{3-0}.bit) = 1	*1	(@H+mem.bit) = 1
	SKF	mem.bit	2	2+S	Skip if (mem.bit) = 0	*3	(mem.bit) = 0
		fmem.bit	2	2+S	Skip if (fmem.bit) = 0	*4	(fmem.bit) = 0
		pmem.@L	2	2+S	Skip if ($pmem_{7-2}$ +L_{3-2}.bit (L_{1-0})) = 0	*5	(pmem.@L) = 0
		@H+mem.bit	2	2+S	Skip if (H + mem_{3-0}.bit) = 0	*1	(@H+mem.bit) = 0
	SKTCLR	fmem.bit	2	2+S	Skip if (fmem.bit) = 1 and clear	*4	(fmem.bit) = 1
		pmem.@L	2	2+S	Skip if ($pmem_{7-2}$+L_{3-2}.bit (L_{1-0})) = 1 and clear	*5	(pmem.@L) = 1
		@H+mem.bit	2	2+S	Skip if (H+mem3-0.bit) = 1 and clear	*1	(@H+mem.bit) = 1
	AND1	CY,fmem.bit	2	2	CY ← CY ∧ (fmem.bit)	*4	
		CY,pmem.@L	2	2	CY ← CY ∧ ($pmem_{7-2}$+L_{3-2}.bit(L_{1-0}))	*5	
		CY,@H+mem.bit	2	2	CY ← CY ∧ (H+mem_{3-0}.bit)	*1	
	OR1	CY,fmem.bit	2	2	CY ← CY ∨ (fmem.bit)	*4	
		CY,pmem.@L	2	2	CY ← CY ∨ ($pmem_{7-2}$+L_{3-2}.bit (L_{1-0}))	*5	
		CY,@H+mem.bit	2	2	CY ← CY ∨ (H+mem_{3-0}.bit)	*1	
	XOR1	CY,fmem.bit	2	2	CY ← CY ⊻ (fmem.bit)	*4	
		CY,pmem.@L	2	2	CY ← CY ⊻ ($pmem_{7-2}$+L_{3-2}.bit (L_{1-0}))	*5	
		CY,@H+mem.bit	2	2	CY ← CY ⊻ (H+mem_{3-0}.bit)	*1	

Instructions	Mnemonics	Operand	Bytes	Machine Cycles	Operation	Addressing Area	Skip Conditions
Branch	BR	addr	—	—	$PC_{12-0} \leftarrow$ addr (The most suitable instruction is selectable from among BR !addr, BRCB !caddr, and BR $addr depending on the assembler.)	*6	
		!addr	3	3	$PC_{12-0} \leftarrow$ addr	*6	
		$addr	1	2	$PC_{12-0} \leftarrow$ addr	*7	
	BRCB	!caddr	2	2	$PC_{11-0} \leftarrow caddr_{11-0}$	*8	
Subroutine/ Stack Control	CALL	!addr	3	3	(SP-4)(SP-1)(SP-2) $\leftarrow PC_{11-0}$ (SP-3) $\leftarrow$ MBE, 0, 0, PC_{12} $PC_{12-0} \leftarrow$ addr, SP $\leftarrow$ SP-4	*6	
	CALLF	!faddr	2	2	(SP-4)(SP-1)(SP-2) $\leftarrow PC_{11-0}$ (SP-3) $\leftarrow$ MBE, 0, 0, PC_{12} $PC_{12-0} \leftarrow$ 00, faddr, SP $\leftarrow$ SP-4	*9	
	RET		1	3	MBE, x, x, $PC_{12} \leftarrow$ (SP+1) $PC_{11-0} \leftarrow$ (SP)(SP+3)(SP+2) SP $\leftarrow$ SP+4		
	RETS		1	3+S	MBE, x, x, $PC_{12} \leftarrow$ (SP+1) $PC_{11-0} \leftarrow$ (SP)(SP+3)(SP+2) SP $\leftarrow$ SP+4, then skip unconditionally		Undefined
	RET1		1	3	MBE, x, x, $PC_{12} \leftarrow$ (SP+1) $PC_{11-0} \leftarrow$ (SP)(SP+3)(SP+2) PSW $\leftarrow$ (SP+4)(SP+5), SP $\leftarrow$ SP+6		
	PUSH	rp	1	1	(SP-1)(SP-2) $\leftarrow$ rp, SP $\leftarrow$ SP-2		
		BS	2	2	(SP-1) $\leftarrow$ MBS, (SP-2) $\leftarrow$ 0, SP $\leftarrow$ SP-2		
	POP	rp	1	1	rp $\leftarrow$ (SP+1)(SP), SP $\leftarrow$ SP+2		
		BS	2	2	MBS $\leftarrow$ (SP+1), SP $\leftarrow$ SP+2		
Interrupt Control	EI		2	2	IME $\leftarrow$ 1		
		IExxx	2	2	IExxx $\leftarrow$ 1		
	DI		2	2	IME $\leftarrow$ 0		
		IExxx	2	2	IExxx $\leftarrow$ 0		
I/O	IN *1	A,PORTn	2	2	A $\leftarrow PORT_n$ (n = 0-8)		
		XA,PORTn	2	2	XA $\leftarrow PORT_{n+1}, PORT_n$ (n = 4, 6)		
	OUT *1	PORTn,A	2	2	$PORT_n \leftarrow$ A (n = 2-8)		
		PORTn,XA	2	2	$PORT_{n+1}, PORT_n \leftarrow$ XA (n = 4, 6)		
CPU Control	HALT		2	2	Set HALT Mode (PCC.2 $\leftarrow$ 1)		
	STOP		2	2	Set STOP Mode (PCC.3 $\leftarrow$ 1)		
	NOP		1	1	No Operation		
Special	SEL	MBn	2	2	MBS $\leftarrow$ n (n = 0, 1, 15)		
	GETI *2	taddr	1	3	· Where TBR instruction, $PC_{12-0} \leftarrow (taddr)_{4-0}+(taddr+1)$	*10	
					· Where TCALL instruction, (SP-4)(SP-1)(SP-2) $\leftarrow PC_{11-0}$ (SP-3) $\leftarrow$ MBE, 0, 0, PC_{12} $PC_{12-0} \leftarrow (taddr)_{4-0}+(taddr+1)$ SP $\leftarrow$ SP-4		
					· Except for TBR and TCALL instructions, Instruction execution of (taddr)(taddr+1)		Depends on referenced instruction

*1: When executing the IN/OUT instruction, MBE = 0, or MBE = 1, and MBS = 15.

2: The TBR, and TCALL instructions are the assembler pseudo-instructions for the table definition of GETI instruction.

10. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Parameter	Symbol	Conditions		Ratings	Unit
Supply Voltage	V_{DD}			-0.3 to +7.0	V
Input Voltage	V_{I1}	Other than ports 4, 5		-0.3 to V_{DD}+0.3	V
	V_{I2}	Ports 4, 5	w/pull-up resistor	-0.3 to V_{DD}+0.3	V
			Open drain	-0.3 to +11	V
Output Voltage	V_O			-0.3 to V_{DD}+0.3	V
High-Level Output Current	I_{OH}	1 pin		-15	mA
		All pins		-30	mA
Low-Level Output Current	I_{OL}*	1 pin	Peak	30	mA
			rms	15	mA
		Other than ports 0, 2, 3, 5, 8	Peak	100	mA
			rms	60	mA
		Total of ports 4, 6, 7	Peak	100	mA
			rms	60	mA
Operating Temperature	T_{opt}			-40 to +85	°C
Storage Temperature	T_{stg}			-65 to +150	°C

*: rms = Peak value x $\sqrt{Duty}$

CAPACITANCE (T_a = 25°C, V_{DD} = 0 V)

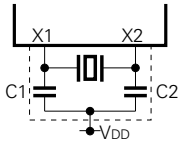
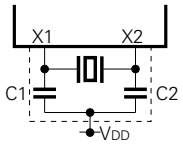
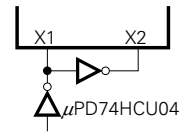
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input Capacitance	C_{IN}	f = 1 MHz			15	pF
Output Capacitance	C_{OUT}	Pins other than thosemeasured are at 0 V			15	pF
Input/Output Capacitance	C_{IO}				15	pF

OPERATING SUPPLY VOLTAGE

Parameter		Symbol	Conditions	MIN.	MAX.	Unit
A/D Converter	Supply voltage	V_{DD}		3.5	6.0	V
	Ambient temperature	T_a		-10	+70	°C
Other Circuits	Supply voltage	V_{DD}		2.7	6.0	V
	Ambient temperatuare	T_a		-40	+85	°C

MAIN SYSTEM CLOCK OSCILLATOR CIRCUIT CHARACTERISTICS

(T_a = -40 to +85°C, V_{DD} = 2.7 to 6.0 V)

Oscillator	Recommended Constants	Item	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic *3		Oscillation frequency(f_{XX})*1		1.0		5.0*4	MHz
		Oscillation stabilization time*2	After V_{DD} came to MIN. of oscillation voltage range			4	ms
Crystal *3		Oscillation frequency (f_{XX})*1		1.0	4.19	5.0*4	MHz
		Oscillation stabilization time*2	V_{DD} = 4.5 to 6.0 V			10	ms
						30	ms
External Clock		X1 input frequency (f_X)*1		1.0		5.0*4	MHz
		X1 input high-, low-level widths (t_{XH}, t_{XL})		100		500	ns

*1: The oscillation frequency and X1 input frequency are indicated only to express the characteristics of the oscillator circuit.
For instruction execution time, refer to AC Characteristics.

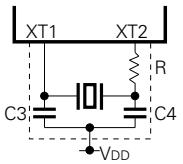
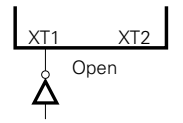
2: Time required for oscillation to stabilize after V_{DD} reaches the minimum value of the oscillation voltage range or the STOP mode has been released.

3: The oscillators on the next page are recommended.

4: When the oscillation frequency is 4.19 MHz < fx ≤ 5.0 MHz, do not select PCC = 0011 as the instruction execution time: otherwise, one machine cycle is set to less than 0.95 μs, falling short of the rated minimum value of 0.95 μs. ★

SUBSYSTEM CLOCK OSCILLATOR CIRCUIT CHARACTERISTICS

(T_a = -40 to +85°C, V_{DD} = 2.7 to 6.0 V)

Oscillator	Recommended Constants	Item	Conditions	MIN.	TYP.	MAX.	Unit
Crystal		Oscillation frequency (f_{XT})		32	32.768	35	kHz
		Oscillation stabilization time*	V_{DD} = 4.5 to 6.0 V		1.0	2	s
						10	s
External Clock		XT1 input frequency (f_{XT})*		32		100	kHz
		XT1 input high-, low-level widths (t_{XTH}, t_{XTL})		5		15	μs

*: Time required for oscillation to stabilize after V_{DD} reaches the minimum value of the oscillation voltage range.

Note: When using the oscillation circuit of the main system clock and subsystem clock, wire the portion enclosed in dotted line in the figures as follows to avoid adverse influences on the wiring capacity:

- Keep the wiring length as short as possible.
- Do not cross the wiring over the other signal lines. Do not route the wiring in the vicinity of lines through which a high alternating current flows.
- Always keep the ground point of the capacitor of the oscillator circuit at the same potential as V_{DD}. Do not connect the power source pattern through which a high current flows.
- Do not extract signals from the oscillation circuit.

The amplification factor of the subsystem clock oscillation circuit is designed to be low to reduce the current dissipation and therefore, the subsystem clock oscillation circuit is influenced by noise more easily than the main system clock oscillation circuit. When using the subsystem clock, therefore, exercise utmost care in wiring the circuit.

RECOMMENDED OSCILLATION CIRCUIT CONSTANTS

MAIN SYSTEM CLOCK: CERAMIC OSCILLATOR (T_a = -40 to +85°C)

Manufacturer	Product Name	Frequency (MHz)	Recommended Circuit Constants		Operating Voltage Range	
			C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)
Murata Mfg. Co., Ltd.	CSAx.xxMG093	2.00 to 2.44	30	30	2.7	6.0
	CSTx.xxMG093		Unnecessary	Unnecessary	2.7	
	CSAx.xxMGU	2.45 to 5.00	30	30	2.7	
	CSTx.xxMGU		Unnecessary	Unnecessary	2.7	
	CSAx.xxMG	2.00 to 5.00	30	30	3.0	
	CSTx.xxMG		Unnecessary	Unnecessary	3.0	
Kyoto Ceramic Co., Ltd.	KBR-2.0MS	2.00	47	47	2.7	6.0
	KBR-4.0MS	4.00	33	33	2.7	
	KBR-5.0M	5.00	33	33	3.0	

MAIN SYSTEM CLOCK: CRYSTAL OSCILLATOR (T_a = -20 to +70°C)

Manufacturer	Product Name	Frequency (MHz)	Recommended Circuit Constants		Operating Voltage Range	
			C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)
Kinseki	HC-18U HC-43U, 49/U	2.0 to 5.0	22 *	22	2.7	6.0

*: Adjust the oscillation frequency in a range of C1 = 15 to 33 pF.

SUBSYSTEM CLOCK: CRYSTAL OSCILLATOR (T_a = -10 to +60°C)

Manufacturer	Product Name	Frequency (MHz)	Recommended Circuit Constants			Operating Voltage Range	
			C3 (pF)	C4 (pF)	R (kΩ)	MIN. (V)	MAX. (V)
Kinseki	P3	32.768	22 *	22	330	2.7	6.0

*: Adjust the oscillation frequency in a range of C3 = 3 to 30 pF.

DC CHARACTERISTICS (T_a = -40 to +85°C, V_{DD} = 2.7 to 6.0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
High-Level Input Voltage	V_{IH1}	Ports 2, 3, 8		0.7V_{DD}		V_{DD}	V
	V_{IH2}	Ports 0, 1, 6, 7, $\overline{RESET}$		0.8V_{DD}		V_{DD}	V
	V_{IH3}	Ports 4, 5	w/pull-up resistor	0.7V_{DD}		V_{DD}	V
			Open-drain	0.7V_{DD}		10	V
	V_{IH4}	X1, X2, XT1		V_{DD}-0.5		V_{DD}	V
Low-level Input Voltage	V_{IL1}	Ports 2, 3, 4, 5, 8		0		0.3V_{DD}	V
	V_{IL2}	Ports 0, 1, 6, 7, $\overline{RESET}$		0		0.2V_{DD}	V
	V_{IL3}	X1, X2, XT1		0		0.4	V
High-Level Output Voltage	V_{OH1}	Ports 0, 2, 3, 6, 7, 8, and BIAS	V_{DD} = 4.5 to 6.0 V I_{OH} = -1 mA	V_{DD}-1.0			V
			I_{OH} = -100 μA	V_{DD}-0.5			V
	V_{OH2}	BP0-7 (with two I_{OH} outputs)	V_{DD} = 4.5 to 6.0 V I_{OH} = -100 μA	V_{DD}-2.0			V
			I_{OH} = -50 μA	V_{DD}-1.0			V
Low-Level Output Voltage	V_{OL1}	Ports 0, 2, 3, 4, 5, 6, 7, and 8	Ports 3, 4, and 5 V_{DD} = 4.5 to 6.0 V I_{OL} = -15 mA		0.4	2.0	V
			V_{DD} = 4.5 to 6.0 V I_{OL} = 1.6 mA			0.4	V
			I_{OL} = 400 μA			0.5	V
		SB0, 1	Open-drain Pull-up resistor ≥ 1 kΩ			0.2V_{DD}	V
	V_{OL2}	BP0-7 (with two I_{OL} outputs)	V_{DD} = 4.5 to 6.0 V I_{OL} = 100 μA			1.0	V
			I_{OL} = 50 μA			1.0	V
High-Level Input Leakage Current	I_{LIH1}	V_{IN} = V_{DD}	Other than below			3	μA
	I_{LIH2}		X1, X2, XT1			20	μA
	I_{LIH3}	V_{IN} = 10 V	Ports 4, 5 (open-drain)			20	μA
Low-Level Input Leakage Current	I_{LIL1}	V_{IN} = 0 V	Other than below			-3	μA
	I_{LIL2}		X1, X2, XT1			-20	μA
High-Level Output Leakage Current	I_{LOH1}	V_{OUT} = V_{DD}	Other than below			3	μA
	I_{LOH2}	V_{OUT} = 10 V	Ports 4, 5 (open-drain)			20	μA
Low-Level Output Leakage Current	I_{LOL}	V_{OUT} = 0 V				-3	μA
Internal Pull-Up Resistor	R_{L1}	Ports 0, 1, 2, 3, 6, 7, 8 (except P00) V_{IN} = 0V	V_{DD} = 5.0 V±10%	15	40	80	kΩ
			V_{DD} = 3.0 V±10%	30		300	kΩ
	R_{L2}	Ports 4, 5 V_{OUT} = V_{DD}-2.0 V	V_{DD} = 5.0 V±10%	15	40	70	kΩ
			V_{DD} = 3.0 V±10%	10		60	kΩ
LCD Drive Voltage	V_{LCD}			2.5		V_{DD}	V
LCD Step-down Resistor	R_{LCD}			60	100	140	kΩ
LCD Output Voltage Deviation (Common) *1	V_{ODC}	I_O = ±5 μA	V_{LCD0} = V_{LCD} V_{LCD1} = V_{LCD}×2/3 V_{LCD2} = V_{LCD}×1/3 2.7 V ≤ V_{LCD} ≤ V_{DD}	0		±0.2 V	V
LCD Output Voltage Deviation (Segment) *1	V_{ODS}	I_O = ±1 μA		0		±0.2 V	V

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Supply Current *2	I_{DD1}	4.19 MHz*3 crystal oscillator C1 = C2 = 22pF	V_{DD} = 5 V±10%*4			2.5	8	mA
			V_{DD} = 3 V±10%*5			0.35	1.2	mA
	I_{DD2}		HALT mode	V_{DD} = 5 V±10%		500	1500	μA
				V_{DD} = 3 V±10%		150	450	μA
	I_{DD3}	32 kHz*6 crystal oscillator	Operation mode	V_{DD} = 3 V±10%		30	90	μA
	I_{DD4}		HALT mode	V_{DD} = 3 V±10%		5	15	μA
	I_{DD5}	XT1 = 0 V STOP mode	V_{DD} = 5 V±10%			0.5	20	μA
			V_{DD} = 3 V±10%			0.1	10	μA
				T_a = 25°C		0.1	5	μA

*1: "Voltage deviation" means the difference between the ideal segment or common output value (V_{LCDn}: n = 0, 1, 2) and output voltage.

2: Currents for the built-in pull-up resistor and the LCD step-down resistor are not included.

3: Including when the subsystem clock is operated.

4: When operand in the high-speed mode with the processor clock control register (PCC) set to 0011.

5: When operated in the low-speed mode with the PCC set to 0000.

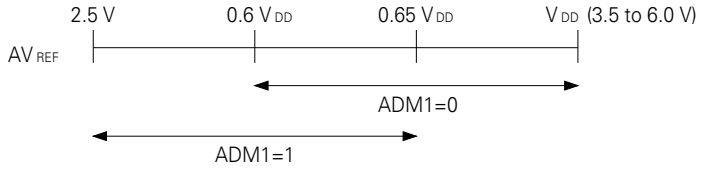
6: When operated with the subsystem clock by setting the system clock control register (SCC) to 1011 to stop the main system clock operation.

A/D CONVERTER (T_a = -10 to +85°C, V_{DD} = 3.5 to 6.0 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Absolute Accuracy*1		2.5 V ≤ AV_{REF} ≤ V_{DD}*2			±1.5	LSB
Conversion Time	t_{CONV}	*3			168/f_X	S
Sampling Time	t_{SAMP}	*4			44/f_X	S
Analog Input Voltage	V_{IAN}		AV_{SS}		AV_{REF}	V
Analog Input Impedance	R_{AN}			1000		MΩ
AV_{REF} Current	I_{REF}			0.25	2.0	mA

*1: Absolute accuracy excluding quantization error ($\pm\frac{1}{2}$LSB)

2: Set ADM1 as follows, in respect to the reference voltage of the AD converter (AV_{REF}).



ADM1 can be set to either 0 or 1 when 0.6V_{DD} ≤ AV_{REF} ≤ 0.65V_{DD}

3: Time since execution of conversion start instruction until EOC = 1 (f_X = 4.19 MHz: 40.1 μs)

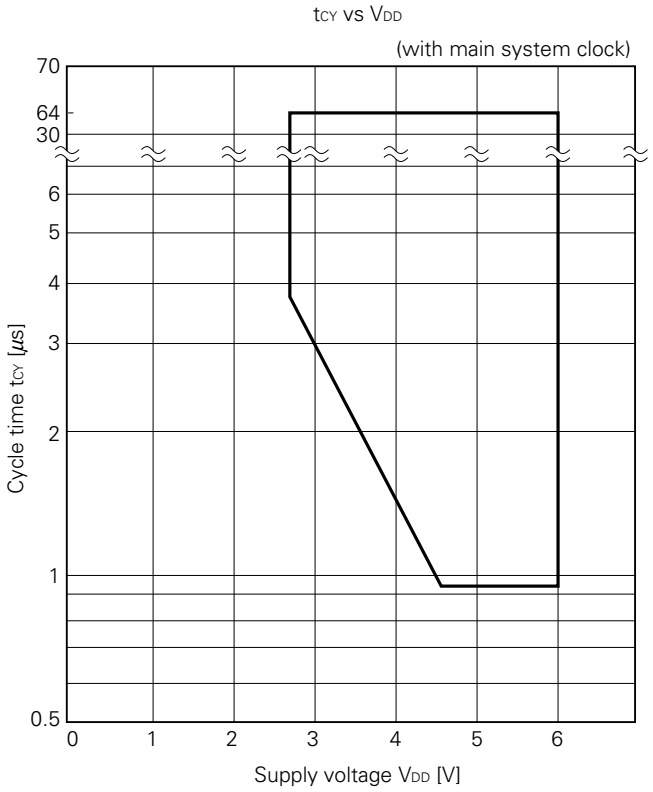
4: Time since execution of conversion start instruction until end of sampling (f_X = 4.19 MHz: 10.5 μs)

AC CHARACTERISTICS (T_a = -40 to +85°C, V_{DD} = 2.7 to 6.0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
CPU Clock Cycle Time (Minimum Instruction Execution Time = 1 Machine Cycle)*1	t_{CY}	w/main system clock	V_{DD} = 4.5 to 6.0 V	0.95		64	μs
				3.8		64	μs
		w/sub-system clock		114	122	125	μs
TI0 Input Frequency	f_{TI}	V_{DD} = 4.5 to 6.0 V		0		1	MHz
				0		275	kHz
TI0 Input High-, Low-Level Widths	t_{TIH}, t_{TIL}	V_{DD} = 4.5 to 6.0 V		0.48			μs
				1.8			μs
Interrupt Input High-, Low-Level Widths	t_{INTH}, t_{INTL}	INT0		*2			μs
		INT1, 2, 4		10			μs
		KR0-7		10			μs
$\overline{\text{RESET}}$ Low-Level Width	t_{RSL}			10			μs

*1: The CPU clock (Φ) cycle time is determined by the oscillation frequency of the connected oscillator, system clock control register (SCC), and processor clock control register (PCC).
The figure on the right is cycle time t_{CY} vs. supply voltage V_{DD} characteristics at the main system clock.

2: $2t_{CY}$ or $128/f_X$ depending on the setting of the interrupt mode register (IM0).



SERIAL TRANSFER OPERATION

Two-Line and Three-Line Serial I/O Modes ($\overline{SCK}$: internal clock output)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ Cycle Time	t_{KCY1}	V_{DD} = 4.5 to 6.0 V		1600			ns
				3800			ns
$\overline{SCK}$ High-, Low-Level Widths	t_{KL1}	V_{DD} = 4.5 to 6.0 V		t_{KCY1}/2-50			ns
	t_{KH1}			t_{KCY1}/2-150			ns
SI Set-Up Time (vs. $\overline{SCK}$ ↑)	t_{SIK1}			150			ns
SI Hold Time (vs. $\overline{SCK}$ ↑)	t_{KSI1}			400			ns
$\overline{SCK}$ ↓→ SO Output Delay Time	t_{KSO1}	R_L = 1 kΩ, C_L = 100 pF*	V_{DD} = 4.5 to 6.0 V			250	ns
						1000	ns

*: R_L and C_L are load resistance and load capacitance of the SO output line.

TWO-LINE AND THREE-LINE SERIAL I/O MODES ($\overline{SCK}$: external clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ Cycle Time	t_{KCY2}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK}$ High-, Low-Level Widths	t_{KL2}	V_{DD} = 4.5 to 6.0 V		400			ns
	t_{KH2}			1600			ns
SI Set-Up Time (vs. $\overline{SCK}$ ↑)	t_{SIK2}			100			ns
SI Hold Time (vs. $\overline{SCK}$ ↑)	t_{KSI2}			400			ns
$\overline{SCK}$ ↓→ SO Output Delay Time	t_{KSO2}	R_L = 1 kΩ, C_L = 100 pF*	V_{DD} = 4.5 to 6.0 V			300	ns
						1000	ns

*: R_L and C_L are load resistance and load capacitance of the SO output line.

SBI MODE ($\overline{SCK}$: internal clock output (master))

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ Cycle Time	t_{KCY3}	V_{DD} = 4.5 to 6.0 V		1600			ns
				3800			ns
$\overline{SCK}$ High-, Low-Level Widths	t_{KL3} t_{KH3}	V_{DD} = 4.5 to 6.0 V		t_{KCY3}/2-50			ns
				t_{KCY3}/2-150			ns
SB0, 1 Set-Up Time (vs. $\overline{SCK}$ ↑)	t_{SIK3}			150			ns
SB0, 1 Hold Time (vs. $\overline{SCK}$ ↑)	t_{KSI3}			t_{KCY3}/2			ns
$\overline{SCK}$ ↓← SB0, 1 Output Delay Time	t_{KSO3}	R_L = 1 kΩ, C_L = 100 pF*	V_{DD} = 4.5 to 6.0 V	0		250	ns
				0		1000	ns
$\overline{SCK}$ ↑→ SB0, 1 ↓	t_{KSB}			t_{KCY3}			ns
SB0,1 ↓→ $\overline{SCK}$	t_{SBK}			t_{KCY3}			ns
SB0, 1 Low-Level Width	t_{SBL}			t_{KCY3}			ns
SB0, 1 High-Level Width	t_{SBH}			t_{KCY3}			ns

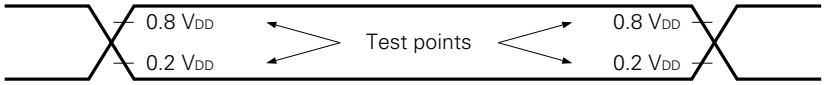
*: R_L and C_L are load resistance and load capacitance of the SO output line.

SBI MODE ($\overline{SCK}$: external clock input (slave))

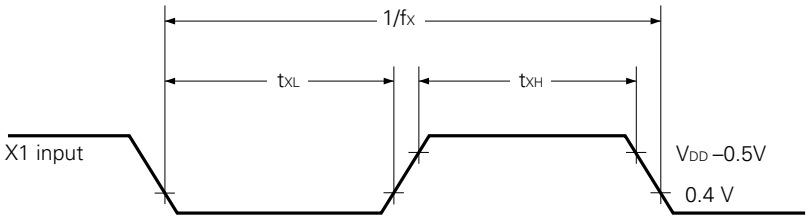
Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ Cycle Time	t_{KCY4}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK}$ High-, Low-Level Widths	t_{KL4} t_{KH4}	V_{DD} = 4.5 to 6.0 V		400			ns
				1600			ns
SB0, 1 Set-Up Time (vs. $\overline{SCK}$ ↑)	t_{SIK4}			100			ns
SB0, 1 Hold Time (vs. $\overline{SCK}$ ↑)	t_{KSI4}			t_{KCY4}/2			ns
$\overline{SCK}$ ↓← SB0, 1 Output Delay Time	t_{KSO4}	R_L = 1 kΩ, C_L = 100 pF*	V_{DD} = 4.5 to 6.0 V	0		300	ns
				0		1000	ns
$\overline{SCK}$ ↑→ SB0, 1 ↓	t_{KSB}			t_{KCY4}			ns
SB0,1 ↓→ $\overline{SCK}$ ↓	t_{SBK}			t_{KCY4}			ns
SB0, 1 Low-Level Width	t_{SBL}			t_{KCY4}			ns
SB0, 1 High-Level Width	t_{SBH}			t_{KCY4}			ns

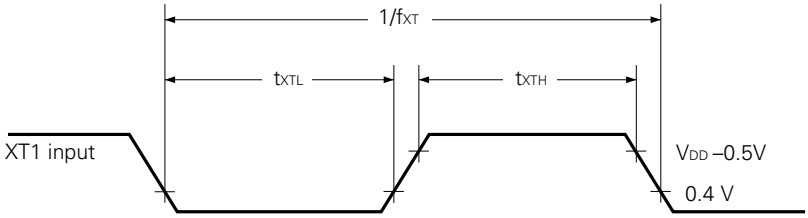
*: R_L and C_L are load resistance and load capacitance of the SO output line.

AC TIMING TEST POINT (excluding X1 and XT1 inputs)

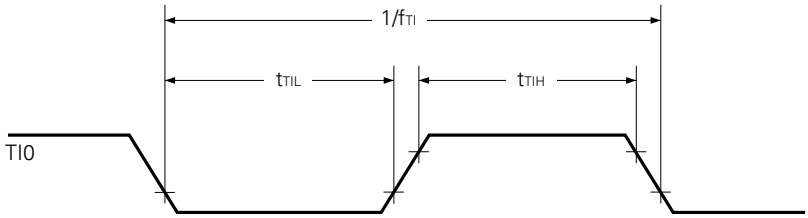


CLOCK TIMING



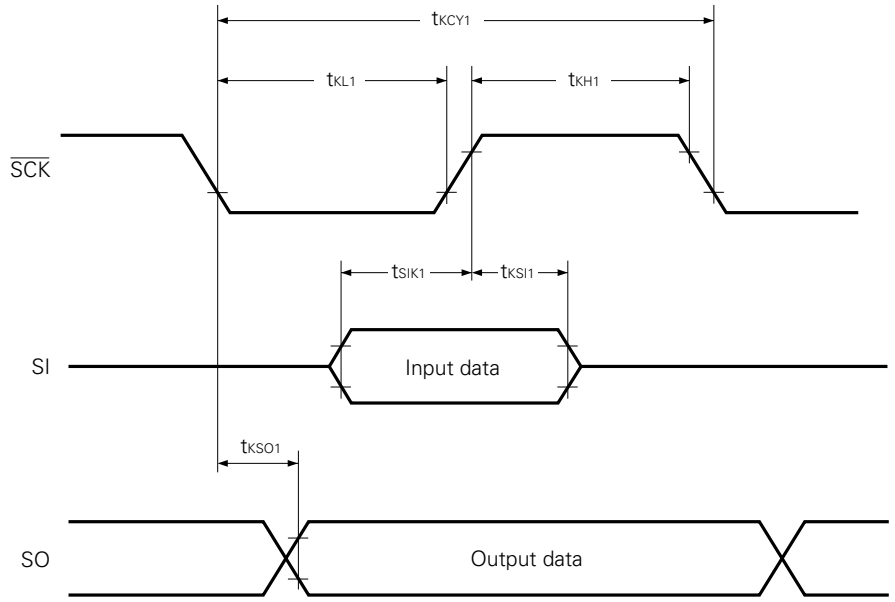


TI0 TIMING

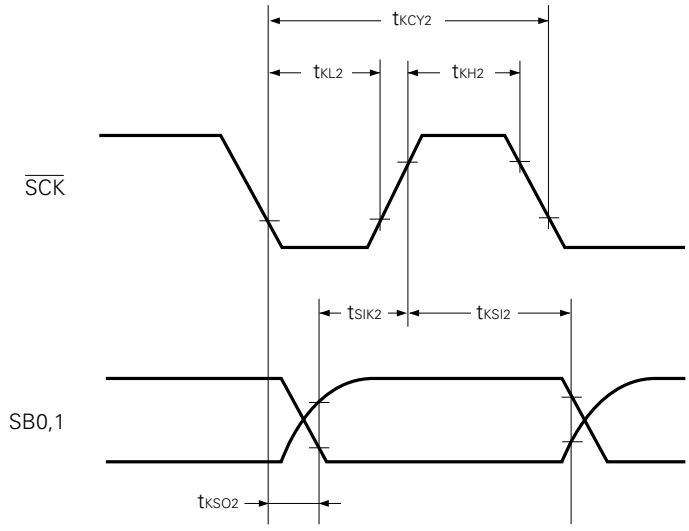


SERIAL TRANSFER TIMING

THREE-LINE SERIAL I/O MODE:

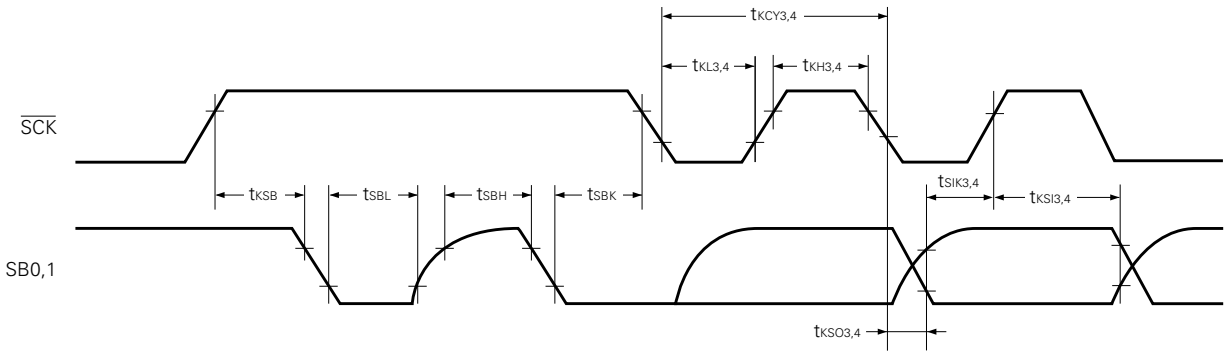


TWO-LINE SERIAL I/O MODE:

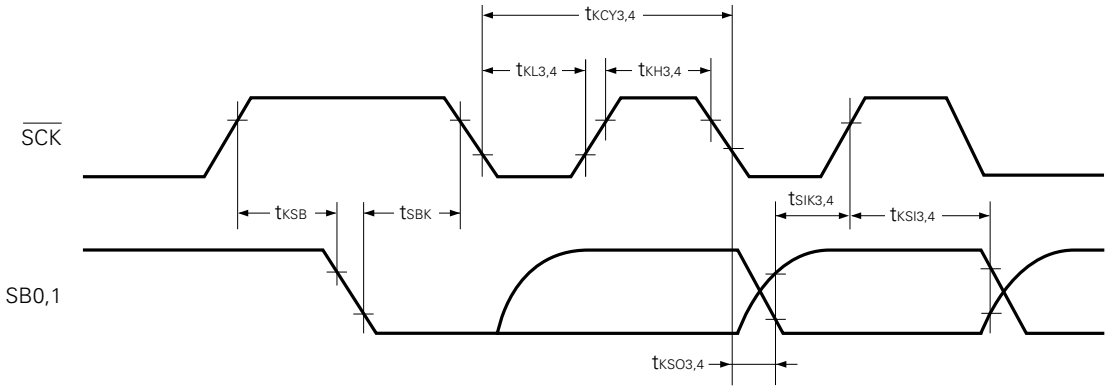


SERIAL TRANSFER TIMING

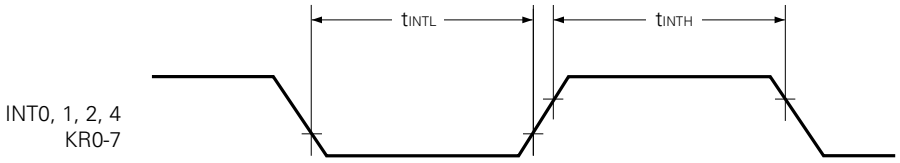
BUS RELEASE SIGNAL TRANSFER:



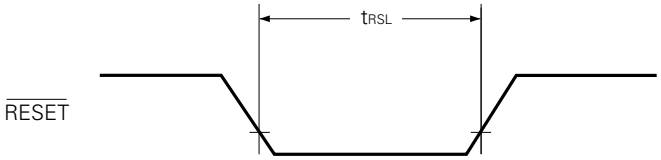
COMMAND SIGNAL TRANSFER:



INTERRUPT INPUT TIMING:



RESET INPUT TIMING:



LOW-VOLTAGE DATA RETENTION CHARACTERISTICS OF DATA MEMORY IN STOP MODE

(T_a = –40 to +85 °C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data Retention Supply Voltage	V_{DDDR}		2.0		6.0	V
Data Retention Supply Current*1	I_{DDDR}	V_{DDDR} = 2.0 V		0.1	10	μA
Release Signal Set Time	t_{SREL}		0			μs
Oscillation Stabilization Wait Time*2	t_{WAIT}	Released by $\overline{RESET}$		$2^{17}/f_x$		ms
		Released by interrupt		*3		ms

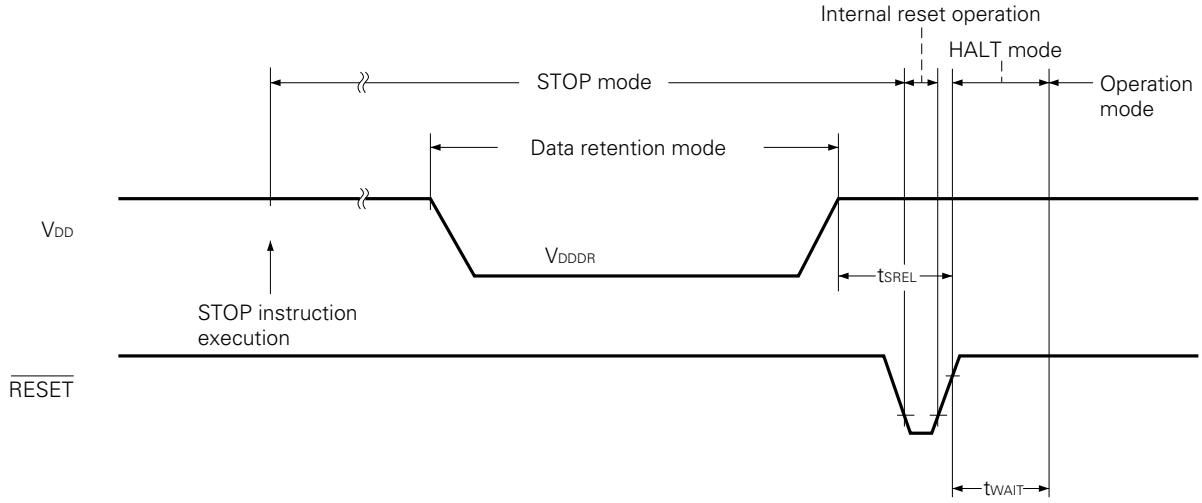
*1: Does not include current flowing through internal pull-up resistor

2: The oscillation stabilization wait time is the time during which the CPU is stopped to prevent unstable operation when oscillation is started.

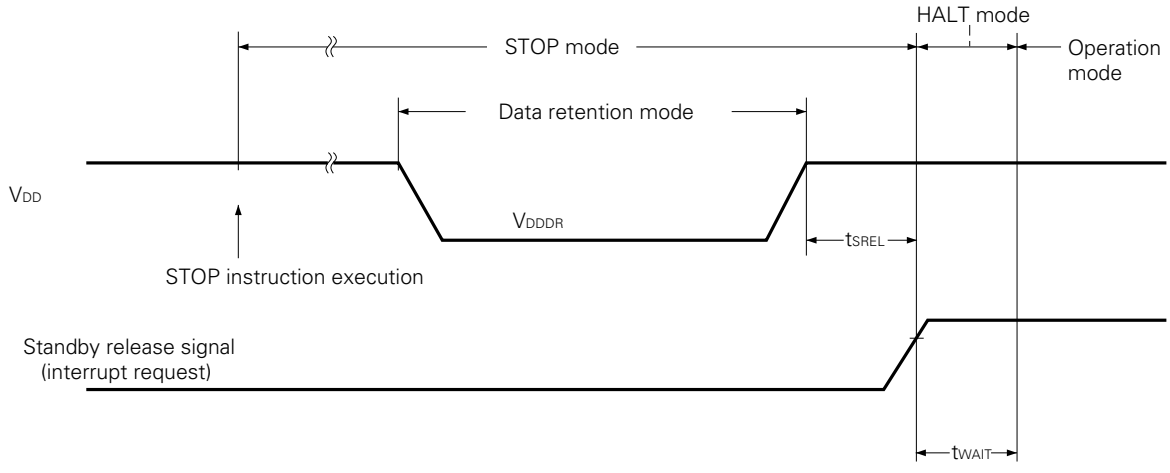
3: Depends on the setting of the basic interval timer mode register (BTM) as follows:

BTM3	BTM2	BTM1	BTM0	WAIT time ( ): f_{XX} = 4.19 MHz
–	0	0	0	$2^{20}/f_{XX}$ (approx. 250 ms)
–	0	1	1	$2^{17}/f_{XX}$ (approx. 31.3 ms)
–	1	0	1	$2^{15}/f_{XX}$ (approx. 7.82 ms)
–	1	1	1	$2^{13}/f_{XX}$ (approx. 1.95 ms)

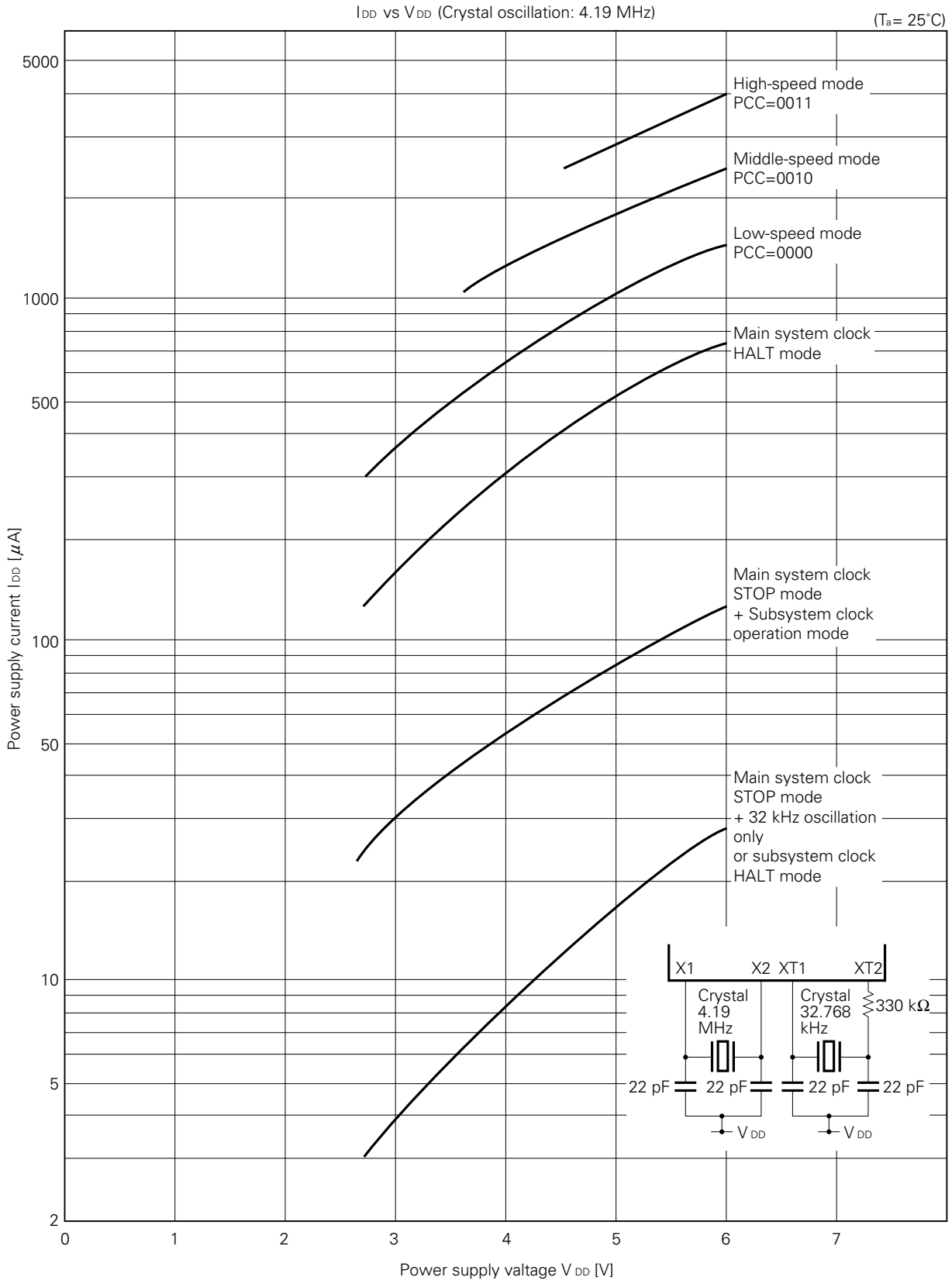
DATA RETENTION TIMING (releasing STOP mode by $\overline{RESET}$)

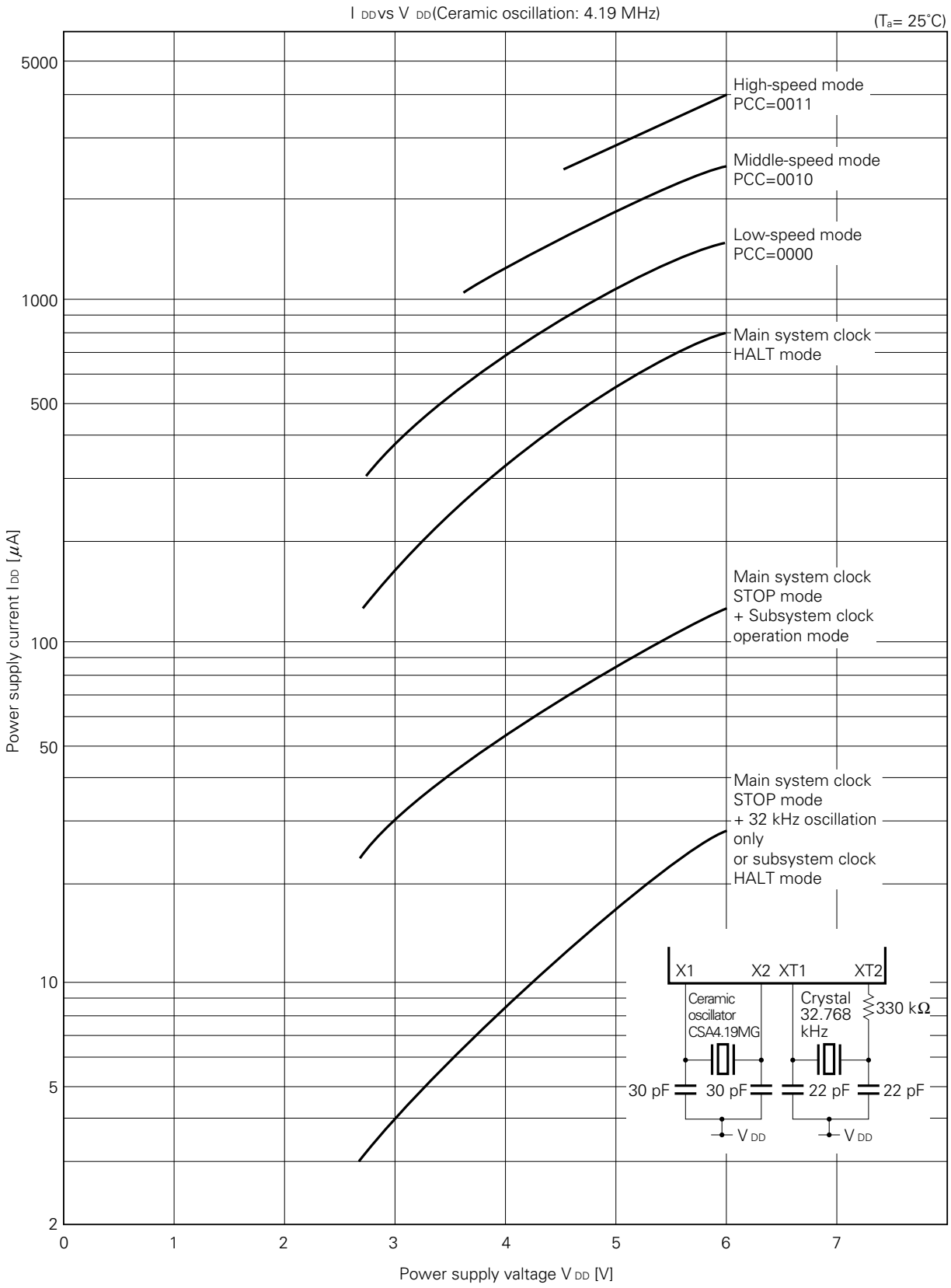


DATA RETENTION TIMING (standby release signal: releasing STOP mode by interrupt)



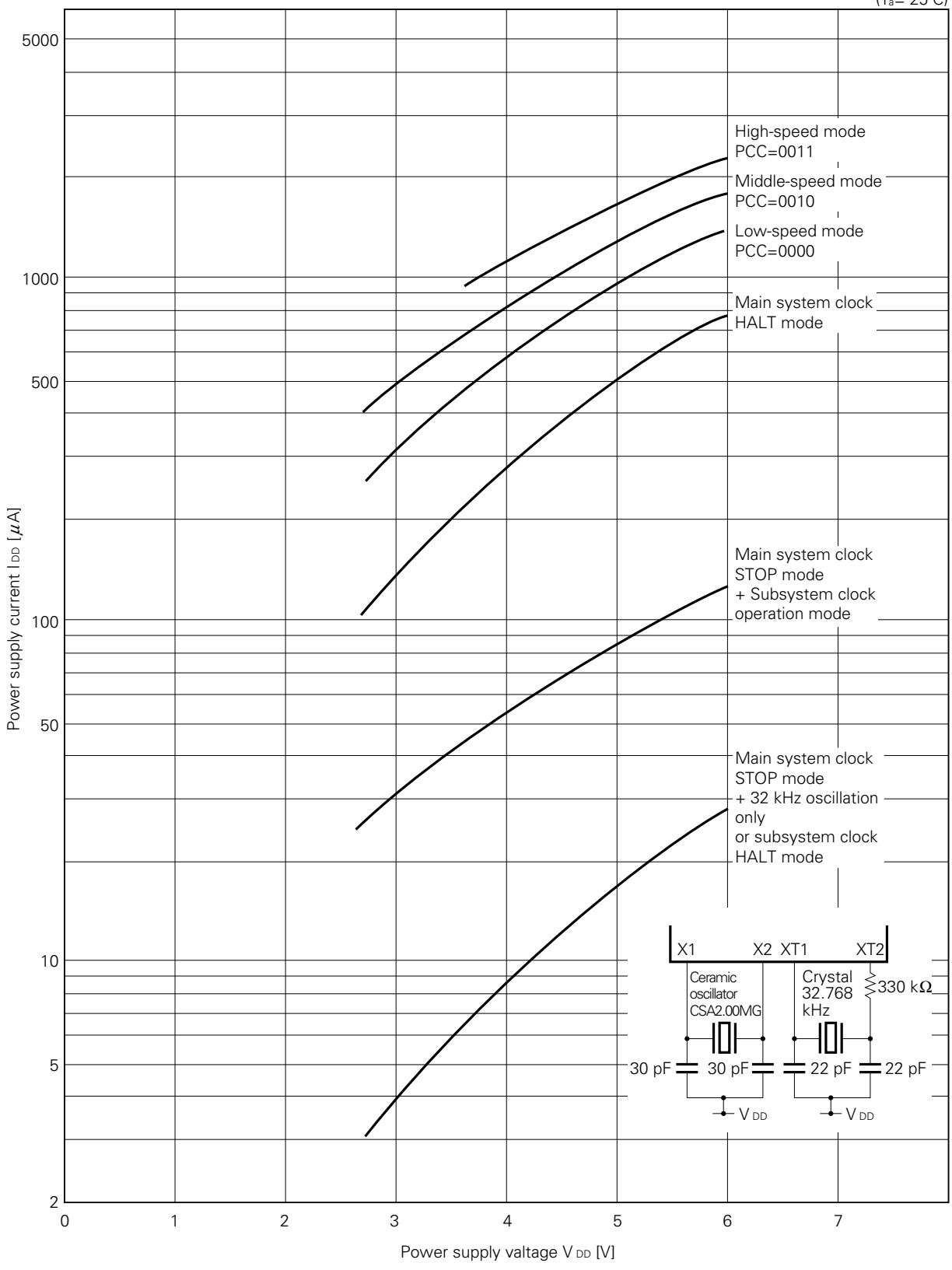
11. CHARACTERISTIC CURVES (REFERENCE VALUE)



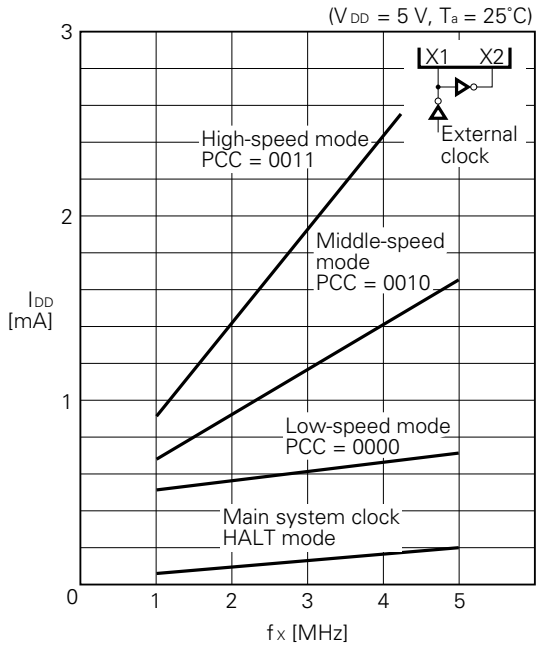

I DD vs V DD (Ceramic oscillation: 4.19 MHz)
(Ta= 25°C)
High-speed mode
PCC=0011
Middle-speed mode
PCC=0010
Low-speed mode
PCC=0000
Main system clock
HALT mode
Main system clock
STOP mode
+ Subsystem clock
operation mode
Main system clock
STOP mode
+ 32 kHz oscillation
only
or subsystem clock
HALT mode
X1
X2
XT1
XT2
Ceramic
oscillator
CSA4.19MG
Crystal
32.768
kHz
330 kΩ
30 pF
30 pF
22 pF
22 pF
V DD
V DD
Power supply current I DD [μA]
Power supply valtage V DD [V]
5000
1000
500
100
50
10
5
2
0
1
2
3
4
5
6
7

I_{DD} vs V_{DD} (Ceramic oscillation: 2.00 MHz)

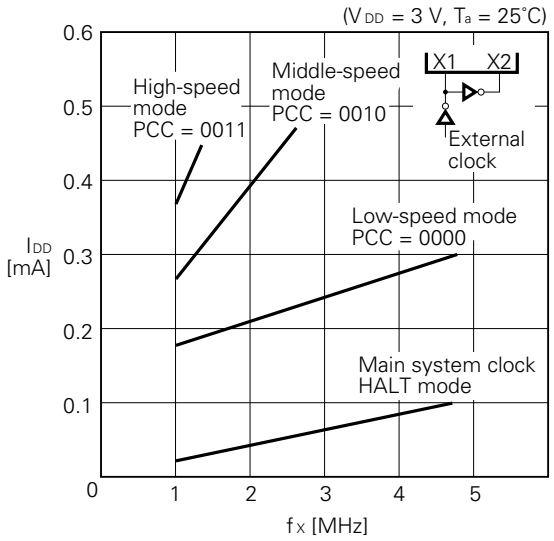
(T_a= 25°C)



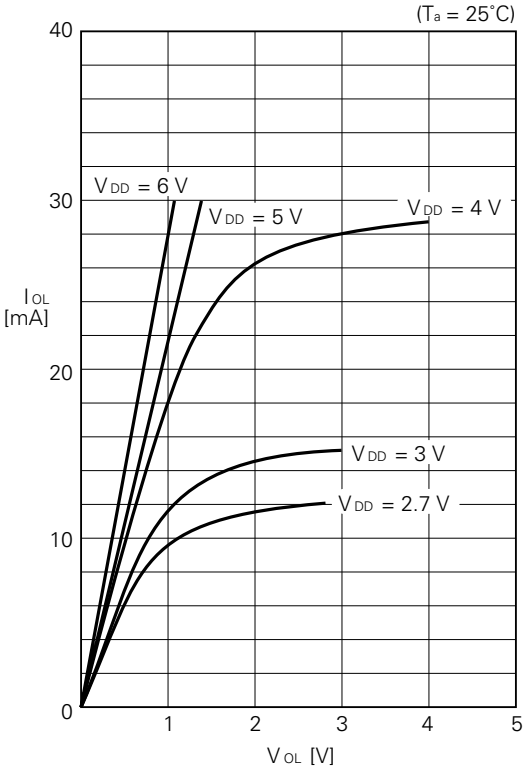
I_{DD} vs f_X



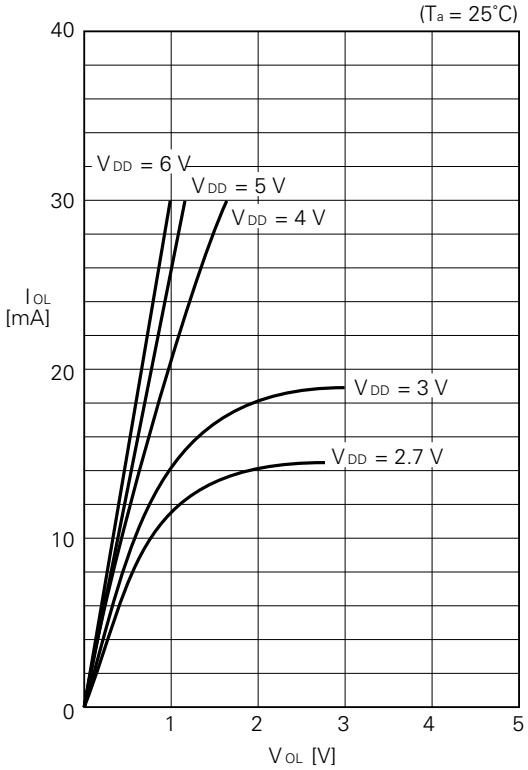
I_{DD} vs f_X



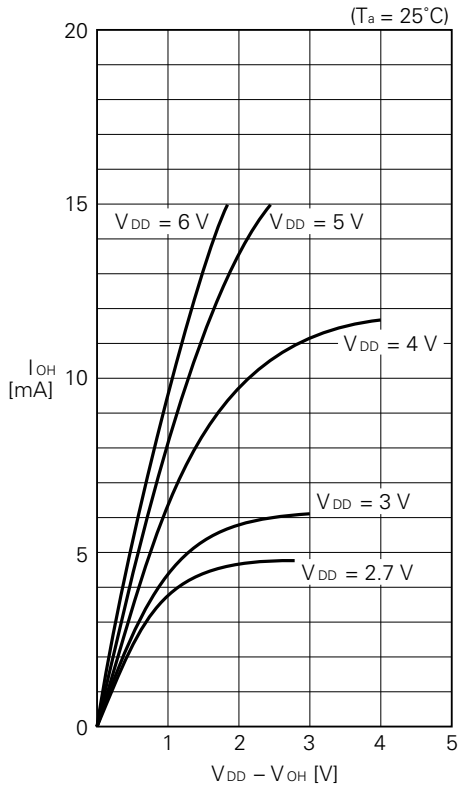
V_{OL} vs I_{OL} (PORT 0, 2, 6, 7, 8)



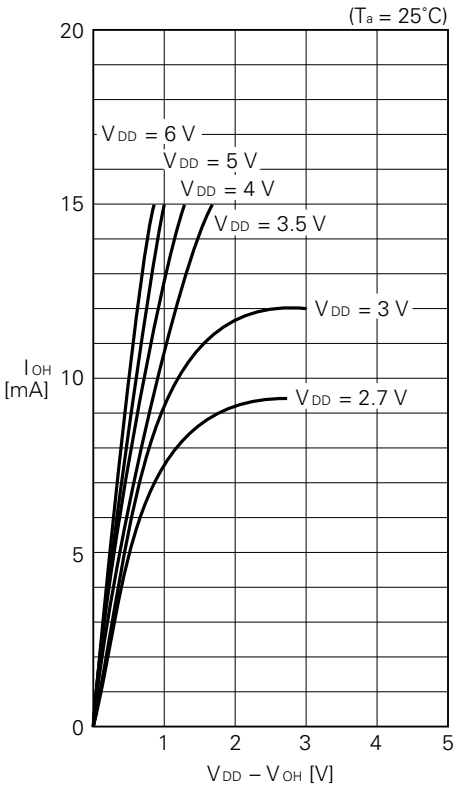
V_{OL} vs I_{OL} (PORT 3, 4, 5)



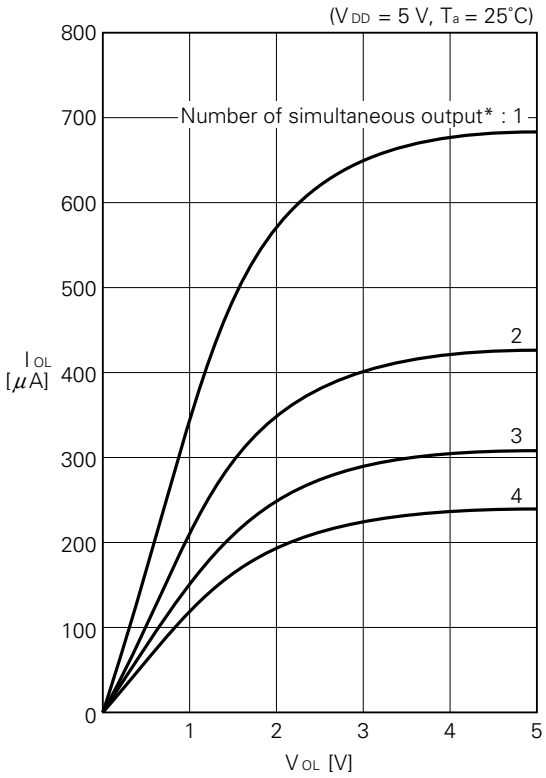
VOH vs IOH (Except for P83)



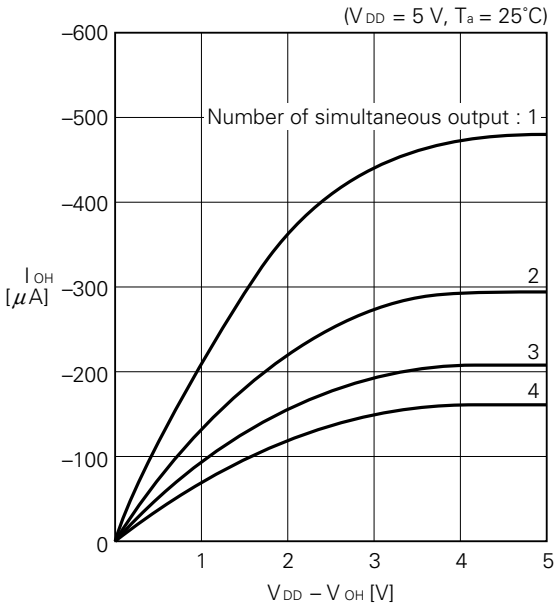
VOH vs IOH (P83)



V_{OL} vs I_{OL} (BP0-3, BP4-7)

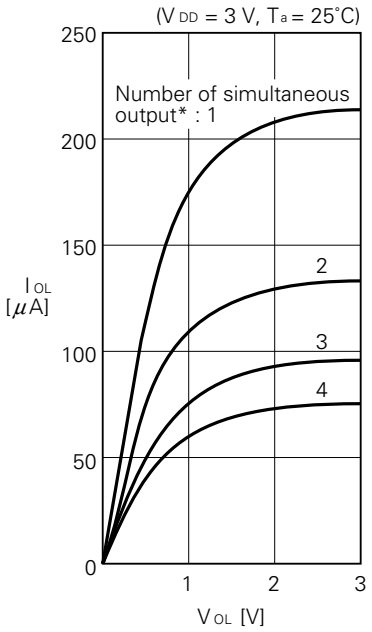


V_{OH} vs I_{OH} (BP0-3, BP4-7)

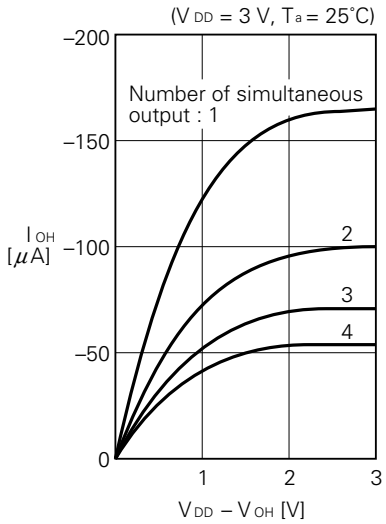


* Of pins BP0-BP3 and BP4-BP7, for each, the number of pins simultaneously outputting the same level.

V_{OL} vs I_{OL} (BP0-3, BP4-7)

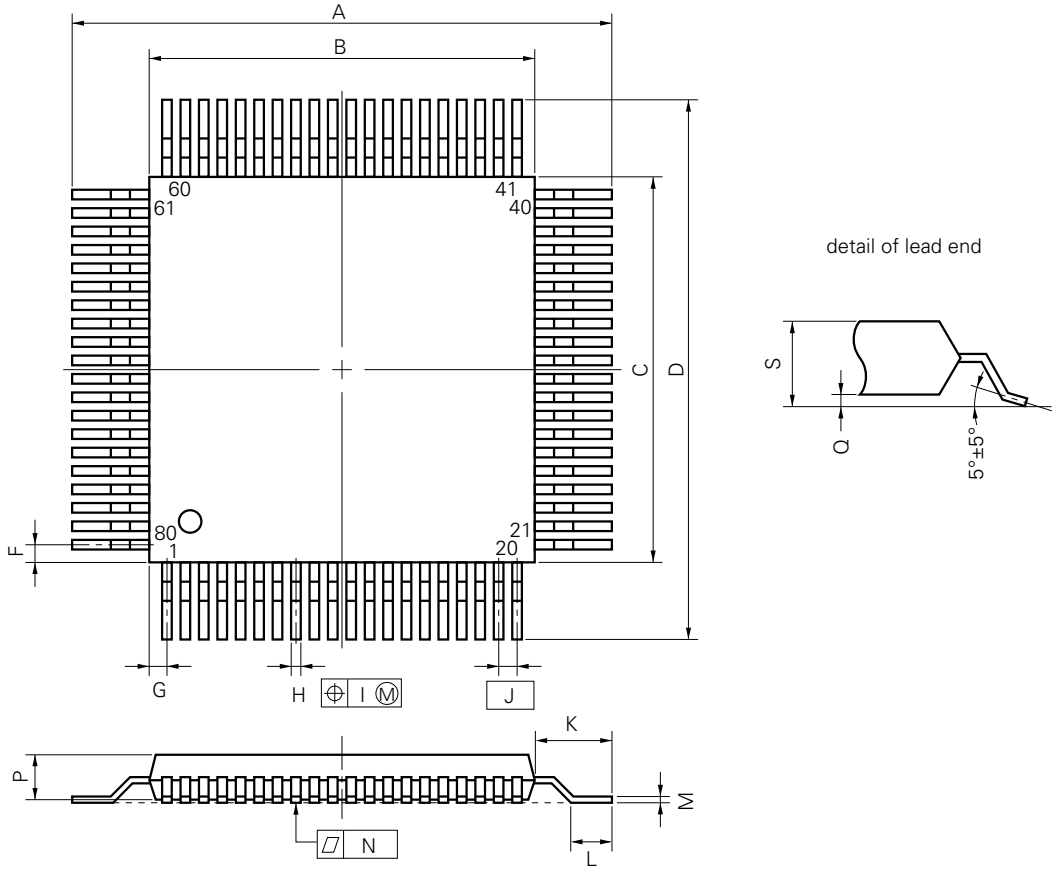


V_{OH} vs I_{OH} (BP0-3, BP4-7)



12. PACKAGE DRAWINGS

80 PIN PLASTIC QFP (□14)



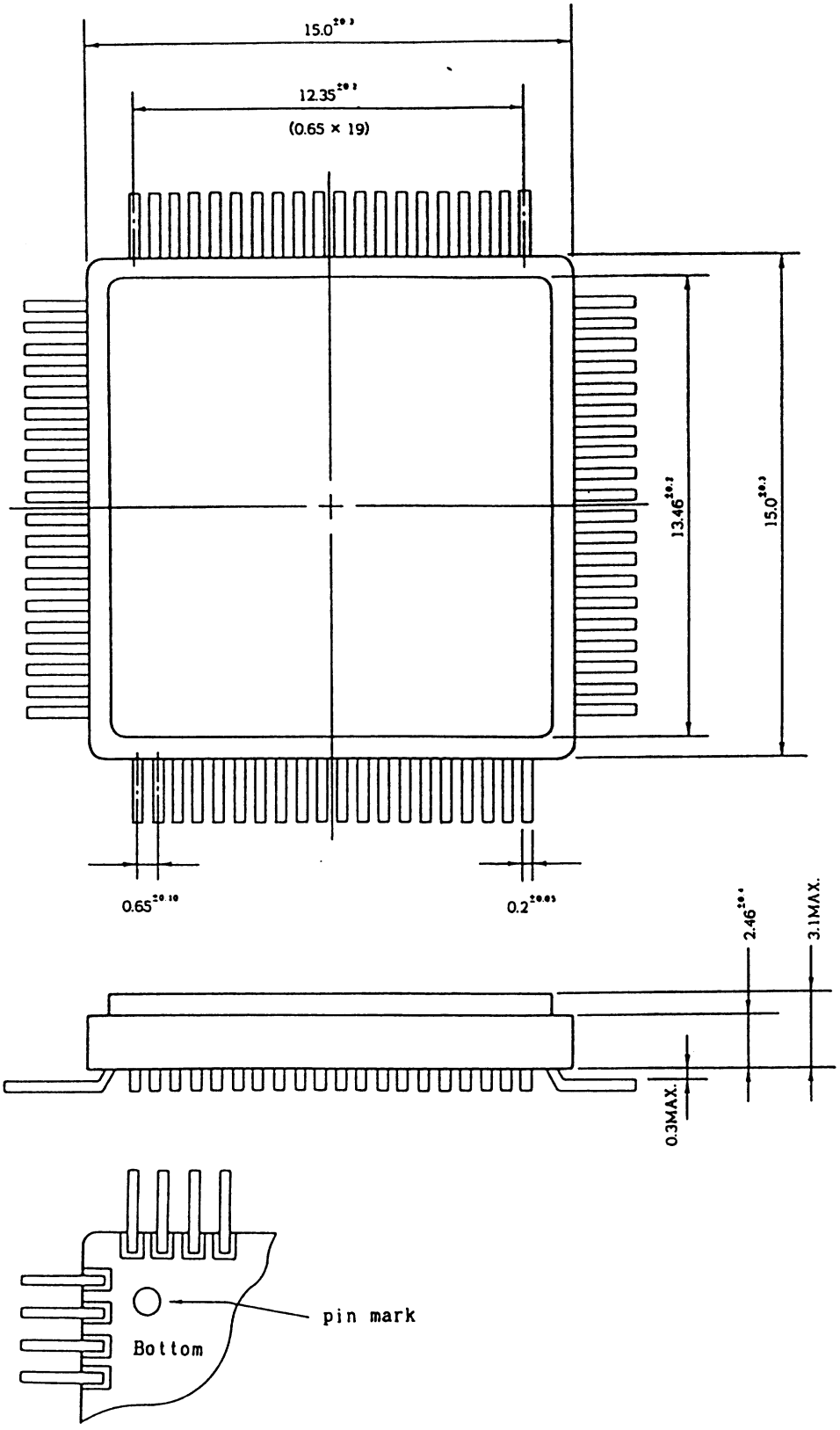
S80GC-65-3B9-3

NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.2±0.4	0.677±0.016
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.2±0.4	0.677±0.016
F	0.8	0.031
G	0.8	0.031
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

80-PIN CERAMIC QFP FOR ES (UNITS IN mm)



Notes: Lead edge cutoff process is not under the process control; therefore the lead length is not specified.

13. RECOMMENDED SOLDERING CONDITIONS ★

It is recommended that μPD75328 be soldered under the following conditions.

For details on the recommended soldering conditions, refer to Information Document "Semiconductor Devices Mounting Manual" (IEI-616).

The soldering methods and conditions are not listed here, consult NEC.

Table 13-1 Soldering Conditions

μPD75328GC - xxx - 3B9: 80-pin plastic QFP (□14 mm)

Soldering Method	Soldering Conditions	Symbol for Recommended Condition
Wave Soldering	Soldering bath temperature: 260°C max., time: 10 seconds max., number of times: 1, pre-heating temperature: 120°C max. (package surface temperature), maximum number of days: 2 days*, (beyond this period, 16 hours of pre-baking is required at 125°C).	WS60-162-1
Infrared Reflow	Package peak temperature: 230°C, time: 30 seconds max. (210°C min.), number of times: 1, maximum number of days: 2 days* (beyond this period, 16 hours of pre-baking is required at 125°C)	IR30-162-1
VPS Reflow	Package peak temperature: 215°C, time: 40 seconds max. (200°C min.), number of times: 1, maximum number of days: 2 days* (beyond this period, 16 hours of pre-baking is required at 125°C)	VP15-162-1
Pin Partial Heating	Pin temperature: 300°C max., time: 3 seconds max. (per side)	—

*: Number of days after unpacking the dry pack. Storage conditions are 25°C and 65%RH max.

Caution: Do not use two or more soldering methods in combination (except the pin partial heating method).

Notice

A model that can be soldered under the more stringent conditions (infrared reflow peak temperature: 235°C, number of times: 2, and an extended number of days) is also available. For details, consult NEC.

APPENDIX A. COMPARISON OF FEATURES BETWEEN μPD75328 AND μPD75308

Item \ Name		μPD75328			μPD75308		
ROM (Bytes)		8064					
RAM (× 4 Bits)		512					
General-Purpose Register		• 4-bit manipulation: 8 × 4 banks • 8-bit manipulation: 4 × 4 banks					
Instruction Cycle		Selectable from 0.95 μs, 1.91 μs, 15.3 ms (main system clock: operating at 4.19 MHz) and 122 μs (subsystem clock: operating at 32.768 kHz)					
Input/ Output Port	COMS Input	36 (44 max.)	8 (shared with INT, SI, SO)	Can be pulled up using software, except for P00	32 (40 max.)	8 (shared with INT, SI, SO)	Can be pulled up using software, except for P00
	CMOS Input/ Output		20 (4 lines can directly drive LED)			16 (4 lines can directly drive LED)	
	CMOS Output		4/8 (shared with segment output, can be selected using software)			4/8 (shared with segment output, can be selected using software)	
	N-ch Input/ Output		8 (can directly drive LED, can be sustain with 10 V, and can be pulled up by mask option)			8 (can directly drive LED, can be sustain with 10 V, and can be pulled up by mask option)	
Timer/Counter		• Timer/event counter • Basic interval timer • Watch timer					
Serial Interface		• Built-in NEC-standard serial bus interface (SBI) • Normal clock synchronized serial interface is also possible					
A/D Converter		6-channel analog input, 8-bit resolution			—		
Vector Interrupt		External: 3, internal: 3					
Test Input		External: 1, internal: 1					
Instruction Set		• Bit data set/reset/test/boolean operation • 4-bit data transfer/arithmetic/increment/decrement/comparison • 8-bit data transfer					
Display Function		LCD controller • Segment outputs: 20 (4/8 can be set for output port by using software) • Common outputs: 4 • Display mode (static, 1/2, 1/3, 1/4) • Built-in step-down resistor network for LCD drive voltage supply (mask option)			LCD controller • Segment outputs: 32 (4/8 can be set for output port by using software) • Common outputs: 4 • Display mode (static, 1/2, 1/3, 1/4) • Built-in step-down resistor network for LCD drive voltage supply (mask option)		
Operating Voltage		2.7 to 6.0 V					
Package		80-pin plastic QFP (□14mm)			80-pin plastic QFP (14×20 mm)		

APPENDIX B. DEVELOPMENT TOOLS ★

The following development support tools are readily available to support development of systems using μPD75328:

PROM writing tools

Hardware	IE-75000-R *1 IE-75001-R	In-circuit emulator for 75X series
	IE-75000-R-EM *2	Emulation board for IE-75000-R and IE-75001-R
	EP-75328GC-R EV-9200GC-80	Emulation prove for μPD75328GC, provided with 80-pin conversion socket EV-9200GC-80.
	PG-1500	PROM programmer
	PA-75P328GC	PROM programmer adapter solely used for μPD75P328GC. It is connected to PG-1500.
Software	IE Control Program	Host machine • PC-9800 series (MS-DOS™ Ver.3.30 to Ver.5.00A*3) • IBM PC/AT™ (PC DOS™ Ver.3.1)
	PG-1500 Controller	
	RA75X Relocatable Assembler	

*1: Maintenance product
2: Not provided with IE-75001-R.
3: Ver.5.00/5.00A has a task swap function, but this function cannot be used with this software.

Remarks: For development tools from other companies, refer to 75X Series Selection Guide (IF-151).

★ APPENDIX C. RELATED DOCUMENTS

GENERAL NOTES ON CMOS DEVICES

① STATIC ELECTRICITY (ALL MOS DEVICES)

Exercise care so that MOS devices are not adversely influenced by static electricity while being handled.

The insulation of the gates of the MOS device may be destroyed by a strong static charge. Therefore, when transporting or storing the MOS device, use a conductive tray, magazine case, or conductive buffer materials, or the metal case NEC uses for packaging and shipment, and use grounding when assembling the MOS device system. Do not leave the MOS device on a plastic plate and do not touch the pins of the device.

Handle boards on which MOS devices are mounted similarly .

② PROCESSING OF UNUSED PINS (CMOS DEVICES ONLY)

Fix the input level of CMOS devices.

Unlike bipolar or NMOS devices, if a CMOS device is operated with nothing connected to its input pin, intermediate level input may be generated due to noise, and an inrush current may flow through the device, causing the device to malfunction. Therefore, fix the input level of the device by using a pull-down or pull-up resistor. If there is a possibility that an unused pin serves as an output pin (whose timing is not specified), each pin should be connected to V_{DD} or GND through a resistor.

Refer to “Processing of Unused Pins” in the documents of each devices.

③ STATUS BEFORE INITIALIZATION (ALL MOS DEVICES)

The initial status of MOS devices is undefined upon power application.

Since the characteristics of an MOS device are determined by the quantity of injection at the molecular level, the initial status of the device is not controlled during the production process. The output status of pins, I/O setting, and register contents upon power application are not guaranteed. However, the items defined for reset operation and mode setting are subject to guarantee after the respective operations have been executed.

When using a device with a reset function, be sure to reset the device after power application.

[MEMO]

M4 92.6