



# 1024K x 8 MoBL Static RAM

## Features

- **High Speed**
  - 55 ns and 70 ns availability
- **Voltage range:**
  - CY62158CV25: 2.2V–2.7V
  - CY62158CV30: 2.7V–3.3V
  - CY62158CV33: 3.0V–3.6V
- **Ultra low active power**
  - Typical active current: 1.5 mA @ f = 1 MHz
  - Typical active current: 5.5 mA @ f = f<sub>max</sub> (70 ns speed)
- **Low standby power**
- **Easy memory expansion with  $\overline{CE}_1$ ,  $\overline{CE}_2$  and  $\overline{OE}$  features**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**

## Functional Description

The CY62158CV25/30/33 are high-performance CMOS static RAMs organized as 1024K words by 8 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL™)

in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption by 80% when addresses are not toggling. The device can be put into standby mode reducing power consumption by more than 99% when deselected ( $\overline{CE}_1$  HIGH or  $\overline{CE}_2$  LOW).

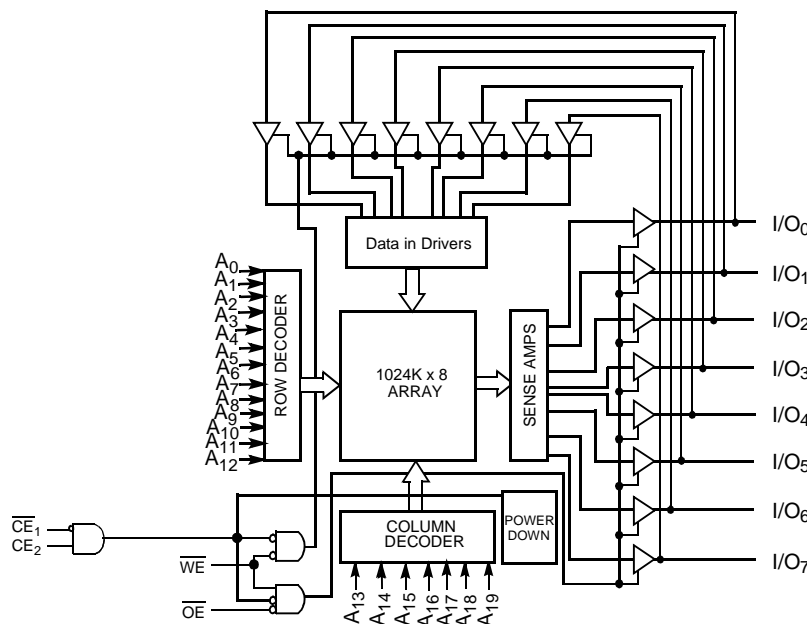
Writing to the device is accomplished by taking Chip Enable 1 ( $\overline{CE}_1$ ) and Write Enable (WE) inputs LOW and Chip Enable 2 ( $\overline{CE}_2$ ) HIGH. Data on the eight I/O pins (I/O<sub>0</sub> through I/O<sub>7</sub>) is then written into the location specified on the address pins (A<sub>0</sub> through A<sub>19</sub>).

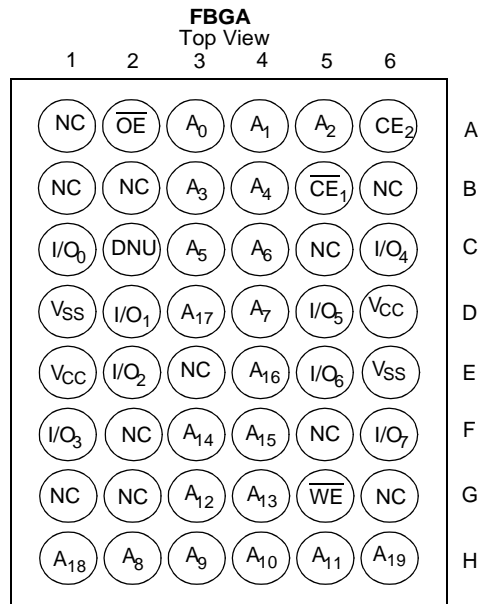
Reading from the device is accomplished by taking Chip Enable 1 ( $\overline{CE}_1$ ) and Output Enable (OE) LOW and Chip Enable 2 ( $\overline{CE}_2$ ) HIGH while forcing Write Enable (WE) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O<sub>0</sub> through I/O<sub>7</sub>) are placed in a high-impedance state when the device is deselected ( $\overline{CE}_1$  LOW and  $\overline{CE}_2$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), or during a write operation ( $\overline{CE}_1$  LOW and  $\overline{CE}_2$  HIGH and WE LOW).

The CY62158CV25/30/33 are available in a 48-ball FBGA package.

## Logic Block Diagram



**Pin Configurations** <sup>[1, 2]</sup>

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....-65°C to +150°C  
 Ambient Temperature with Power Applied. ....55°C to +125°C  
 Supply Voltage to Ground Potential ...-0.5V to V<sub>CCmax</sub> + 0.5V

DC Voltage Applied to Outputs in High Z State<sup>[3]</sup>.....

-0.5V to V<sub>CC</sub> + 0.5V  
 DC Input Voltage<sup>[3]</sup>.....-0.5V to V<sub>CC</sub> + 0.5V  
 Output Current into Outputs (LOW).....20 mA  
 Static Discharge Voltage .....>2001V (per MIL-STD-883, Method 3015)  
 Latch-Up Current .....>200 mA

**Operating Range**

Product	Range	Ambient Temperature	V <sub>CC</sub>
CY62158CV25	Industrial	-40°C to +85°C	2.2V to 2.7V
CY62158CV30			2.7V to 3.3V
CY62158CV33			3.0V to 3.6V

**Product Portfolio**

Product	V <sub>CC</sub> Range			Speed	Power Dissipation (Industrial)					
					Operating (I <sub>CC</sub> )				Standby (I <sub>SB2</sub> )	
					f = 1 MHz		f = f <sub>max</sub>			
					Min.	Typ. <sup>[4]</sup>	Max.	Typ. <sup>[4]</sup>	Max.	Typ. <sup>[4]</sup>
CY62158CV25	2.2V	2.5V	2.7V	55 ns	1.5 mA	3 mA	7 mA	15 mA	6 μA	25 μA
				70 ns	1.5 mA	3 mA	5.5 mA	12 mA		
CY62158CV30	2.7V	3.0V	3.3V	55 ns	1.5 mA	3 mA	7 mA	15 mA	8 μA	25 μA
				70 ns	1.5 mA	3 mA	5.5 mA	12 mA		
CY62158CV33	3.0V	3.3V	3.6V	55 ns	1.5 mA	3 mA	7 mA	15 mA	10 μA	30 μA
				70 ns	1.5 mA	3 mA	5.5 mA	12 mA		

**Notes:**

- NC pins are not connected to the die.
- C2 (DNU) can be left as NC or V<sub>SS</sub> to ensure proper application.
- V<sub>IL(min.)</sub> = -2.0V for pulse durations less than 20 ns.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ.)</sub>, T<sub>A</sub> = 25°C.

**Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions		CY62158CV25-55			CY62158CV25-70			Unit
				Min.	Typ. <sup>[4]</sup>	Max.	Min.	Typ. <sup>[4]</sup>	Max.	
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -0.1 mA	V <sub>CC</sub> = 2.2V	2.0			2.0			V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 0.1 mA	V <sub>CC</sub> = 2.2V			0.4			0.4	V
V <sub>IH</sub>	Input HIGH Voltage			1.8		V <sub>CC</sub> +0.3V	1.8		V <sub>CC</sub> +0.3V	V
V <sub>IL</sub>	Input LOW Voltage			-0.3		0.6	-0.3		0.6	V
I <sub>IX</sub>	Input Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>		-1		+1	-1		+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled		-1		+1	-1		+1	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	f = f <sub>MAX</sub> = 1/t <sub>RC</sub>	V <sub>CC</sub> = 2.7V		7	15		5.5	12	mA
		f = 1 MHz	I <sub>OUT</sub> = 0 mA CMOS Levels		1.5	3		1.5	3	
I <sub>SB1</sub>	Automatic CE Power-Down Current — CMOS Inputs	$\overline{CE}_1 \geq V_{CC} - 0.2V$ or $CE_2 \leq 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ , $f = f_{max}$ (Address and Data Only), $f = 0$ (OE, WE)			6	25		6	25	μA
I <sub>SB2</sub>	Automatic CE Power-Down Current — CMOS Inputs	$\overline{CE}_1 \geq V_{CC} - 0.2V$ or $CE_2 \leq 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ , $f = 0$ , V <sub>CC</sub> = 2.7V								

Parameter	Description	Test Conditions		CY62158CV30-55			CY62158CV30-70			Unit
				Min.	Typ. <sup>[4]</sup>	Max.	Min.	Typ. <sup>[4]</sup>	Max.	
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -1.0 mA	V <sub>CC</sub> = 2.7V	2.4			2.4			V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 2.1 mA	V <sub>CC</sub> = 2.7V			0.4			0.4	V
V <sub>IH</sub>	Input HIGH Voltage			2.2		V <sub>CC</sub> +0.3V	2.2		V <sub>CC</sub> +0.3V	V
V <sub>IL</sub>	Input LOW Voltage			-0.3		0.8	-0.3		0.8	V
I <sub>IX</sub>	Input Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>		-1		+1	-1		+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled		-1		+1	-1		+1	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	f = f <sub>MAX</sub> = 1/t <sub>RC</sub>	V <sub>CC</sub> = 3.3V		7	15		5.5	12	mA
		f = 1 MHz	I <sub>OUT</sub> = 0 mA CMOS Levels		1.5	3		1.5	3	
I <sub>SB1</sub>	Automatic CE Power-Down Current — CMOS Inputs	$\overline{CE}_1 \geq V_{CC} - 0.2V$ or $CE_2 \leq 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ , $f = f_{max}$ (Address and Data Only), $f = 0$ (OE, WE)			8	25		8	25	μA
I <sub>SB2</sub>	Automatic CE Power-Down Current — CMOS Inputs	$\overline{CE}_1 \geq V_{CC} - 0.2V$ or $CE_2 \leq 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ , $f = 0$ , V <sub>CC</sub> = 3.3V								

**Electrical Characteristics** Over the Operating Range (continued)

Parameter	Description	Test Conditions	CY62158CV33-55			CY62158CV33-70			Unit
			Min.	Typ. <sup>[4]</sup>	Max.	Min.	Typ. <sup>[4]</sup>	Max.	
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -1.0 mA V <sub>CC</sub> = 3.0V	2.4			2.4			V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 2.1 mA V <sub>CC</sub> = 3.0V			0.4			0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2		V <sub>CC</sub> +0.3V	2.2		V <sub>CC</sub> +0.3V	V
V <sub>IL</sub>	Input LOW Voltage		-0.3		0.8	-0.3		0.8	V
I <sub>IX</sub>	Input Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1		+1	-1		+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled	-1		+1	-1		+1	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	f = f <sub>MAX</sub> = 1/t <sub>RC</sub> f = 1 MHz		7	15		5.5	12	mA
		V <sub>CC</sub> = 3.6V I <sub>OUT</sub> = 0 mA CMOS Levels		1.5	2		1.5	2	
I <sub>SB1</sub>	Automatic CE Power-Down Current — CMOS Inputs	$\overline{CE}_1 \geq V_{CC} - 0.2V$ or $CE_2 \leq 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ , f = f <sub>max</sub> (Address and Data Only), f=0 (OE, WE)		10	30		10	30	μA
I <sub>SB2</sub>	Automatic CE Power-Down Current — CMOS Inputs	$\overline{CE}_1 \geq V_{CC} - 0.2V$ or $CE_2 \leq 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ , f = 0, V <sub>CC</sub> = 3.6V							

**Capacitance<sup>[5]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz,	6	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>CC</sub> = V <sub>CC(typ.)</sub>	8	pF

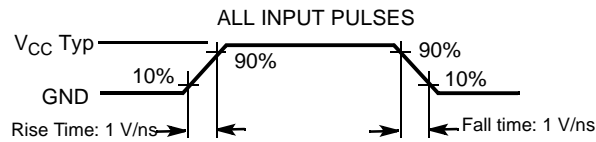
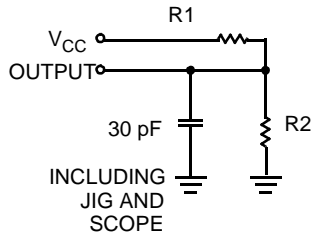
**Thermal Resistance**

Description	Test Conditions	Symbol	BGA	Unit
Thermal Resistance <sup>[5]</sup> (Junction to Ambient)	Still Air, soldered on a 3 x 4.5 inch, two-layer printed circuit board	θ <sub>JA</sub>	55	°C/W
Thermal Resistance <sup>[5]</sup> (Junction to Case)		θ <sub>JC</sub>	16	°C/W

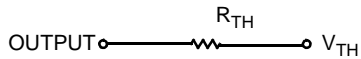
**Note:**

5. Tested initially and after any design or process changes that may affect these parameters.

### AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT

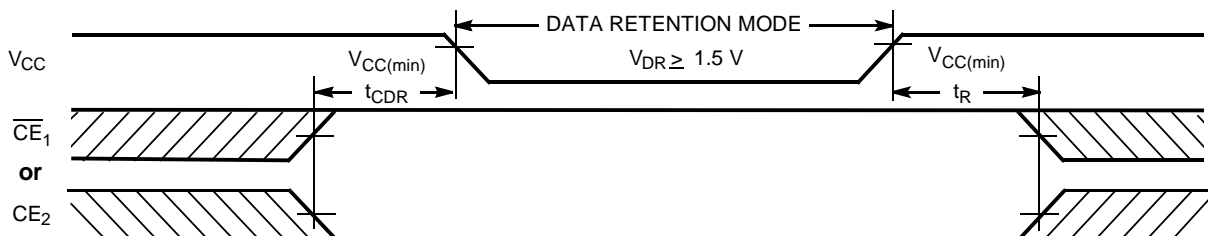


Parameters	2.5V	3.0V	3.3V	Unit
R1	16.6	1.105	1.216	K Ohms
R2	15.4	1.550	1.374	K Ohms
R <sub>TH</sub>	8.0	0.645	0.645	K Ohms
V <sub>TH</sub>	1.20	1.75	1.75	Volts

### Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions	Min.	Typ. <sup>[4]</sup>	Max.	Unit
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention		1.5		V <sub>CCmax</sub>	V
I <sub>CCDR</sub>	Data Retention Current	V <sub>CC</sub> = 1.5V CE <sub>1</sub> ≥ V <sub>CC</sub> - 0.2V or CE <sub>2</sub> ≤ 0.2V V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V		4	20	μA
t <sub>CDR</sub> <sup>[5]</sup>	Chip Deselect to Data Retention Time		0			ns
t <sub>R</sub> <sup>[6]</sup>	Operation Recovery Time		t <sub>RC</sub>			ns

### Data Retention Waveform



**Note:**

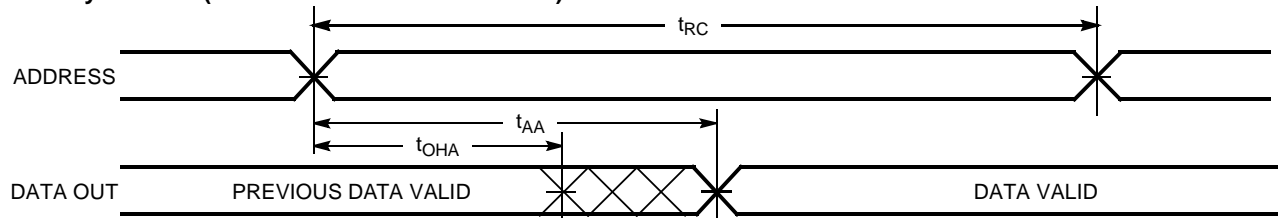
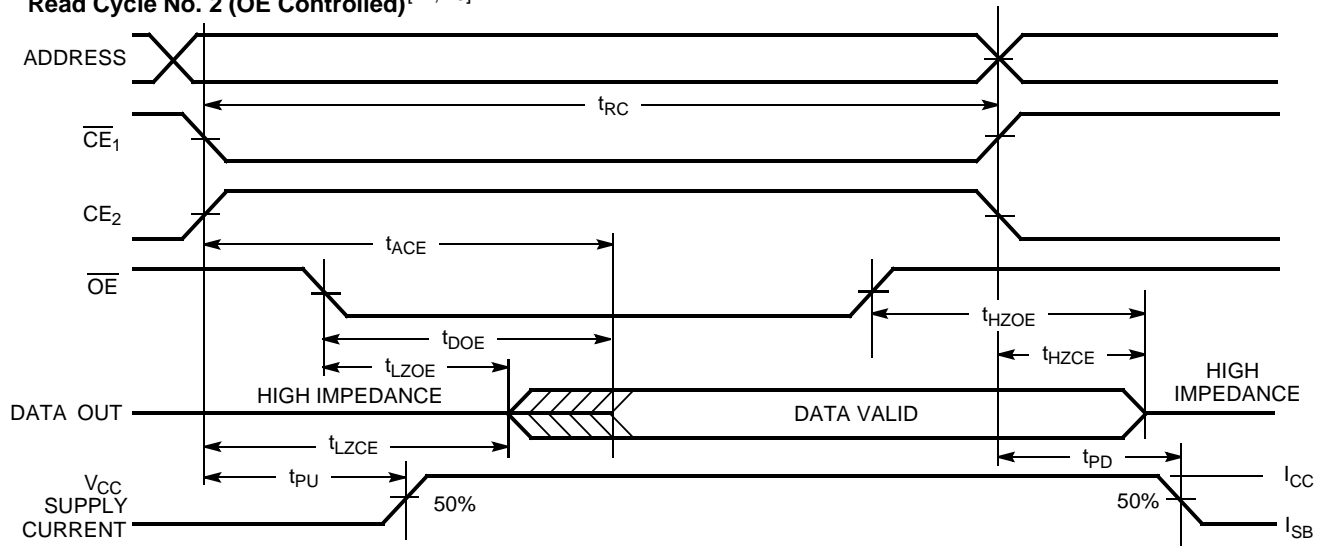
- Full Device AC operation requires linear V<sub>CC</sub> ramp from V<sub>DR</sub> to V<sub>CC(min.)</sub> ≥ 100 μs or stable at V<sub>CC(min.)</sub> ≥ 100 μs.

**Switching Characteristics** Over the Operating Range<sup>[7]</sup>

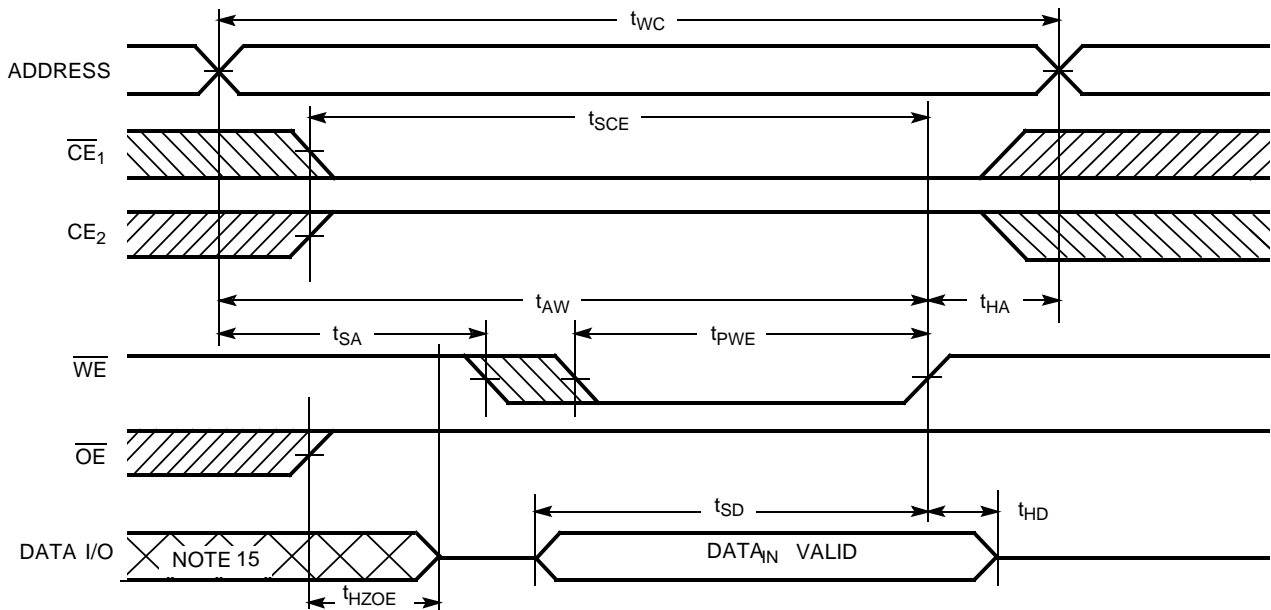
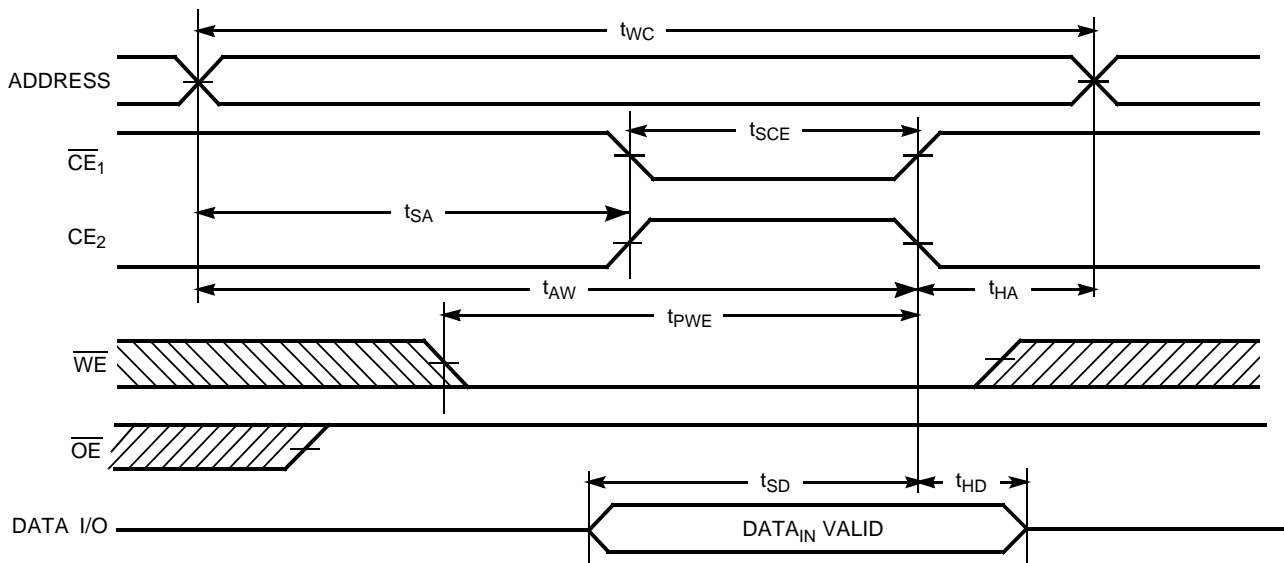
Parameter	Description	55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>						
t <sub>RC</sub>	Read Cycle Time	55		70		ns
t <sub>AA</sub>	Address to Data Valid		55		70	ns
t <sub>OHA</sub>	Data Hold from Address Change	10		10		ns
t <sub>ACE</sub>	$\overline{CE}_1$ LOW and CE <sub>2</sub> HIGH to Data Valid		55		70	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		25		35	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low Z <sup>[8]</sup>	5		5		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z <sup>[8, 9]</sup>		20		25	ns
t <sub>LZCE</sub>	$\overline{CE}_1$ LOW and CE <sub>2</sub> HIGH to Low Z <sup>[8]</sup>	10		10		ns
t <sub>HZCE</sub>	$\overline{CE}_1$ HIGH or CE <sub>2</sub> LOW to High Z <sup>[8, 9]</sup>		20		25	ns
t <sub>PU</sub>	$\overline{CE}_1$ LOW and CE <sub>2</sub> HIGH to Power-Up	0		0		ns
t <sub>PD</sub>	$\overline{CE}_1$ HIGH or CE <sub>2</sub> LOW to Power-Down		55		70	ns
<b>WRITE CYCLE<sup>[10]</sup></b>						
t <sub>WC</sub>	Write Cycle Time	55		70		ns
t <sub>SCE</sub>	$\overline{CE}_1$ LOW and CE <sub>2</sub> HIGH to Write End	45		60		ns
t <sub>AW</sub>	Address Set-Up to Write End	45		60		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		ns
t <sub>SA</sub>	Address Set-Up to Write Start	0		0		ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	45		50		ns
t <sub>SD</sub>	Data Set-Up to Write End	25		30		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High Z <sup>[8, 9]</sup>		20		25	ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low Z <sup>[8]</sup>	5		5		ns

**Notes:**

7. Test conditions assume signal transition time of 5 ns or less, timing reference levels of  $V_{CC(typ.)}/2$ , input pulse levels of 0 to  $V_{CC(typ.)}$ , and output loading of the specified  $I_{OL}/I_{OH}$  and 30-pF load capacitance.
8. At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZOE</sub> is less than t<sub>LZOE</sub>, and t<sub>HZWE</sub> is less than t<sub>LZWE</sub> for any given device.
9. t<sub>HZOE</sub>, t<sub>HZCE</sub>, and t<sub>HZWE</sub> transitions are measured when the outputs enter a high impedance state.
10. The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE}_1 = V_{IL}$ , and CE<sub>2</sub> = V<sub>IH</sub>. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.

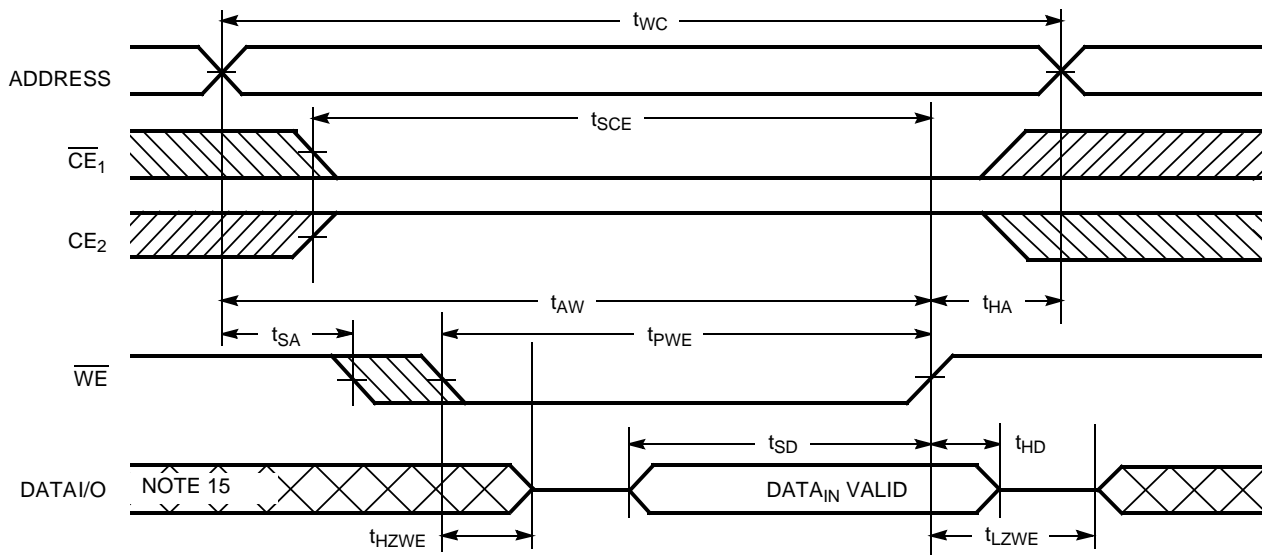
**Switching Waveforms**
**Read Cycle No. 1 (Address Transition Controlled)**<sup>[11, 12]</sup>

**Read Cycle No. 2 ( $\overline{OE}$  Controlled)**<sup>[12, 13]</sup>

**Notes:**

11. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}_1 = V_{IL}$ ,  $CE_2 = V_{IH}$ .
12.  $\overline{WE}$  is HIGH for read cycle.
13. Address valid prior to or coincident with  $\overline{CE}_1$  transition LOW and  $CE_2$  transition HIGH.

**Switching Waveforms**
**Write Cycle No. 1 (WE Controlled)** <sup>[10, 14, 16]</sup>

**Write Cycle No. 2 ( $\overline{CE}_1$  or  $CE_2$  Controlled)** <sup>[10, 14, 16]</sup>

**Notes:**

14. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .
15. During this period, the I/Os are in output state and input signals should not be applied.
16. If  $\overline{CE}_1$  goes HIGH or  $CE_2$  goes LOW simultaneously with  $\overline{WE}$  HIGH, the output remains in high-impedance state.

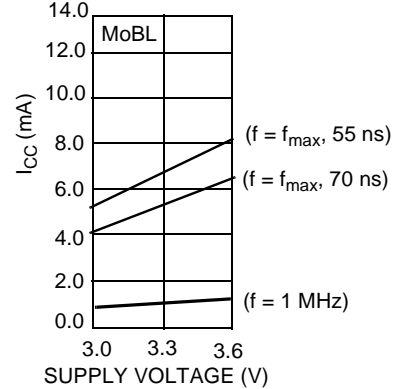
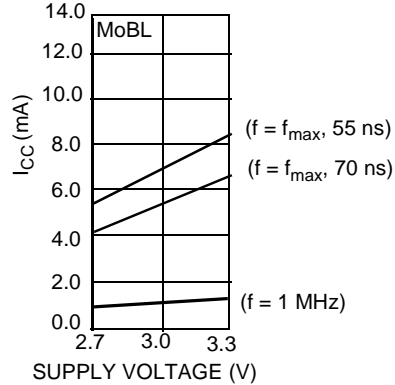
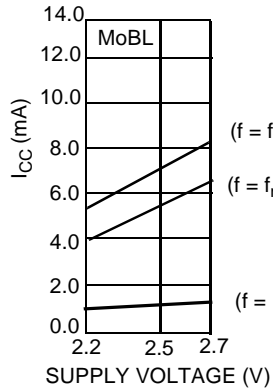


**Switching Waveforms**
**Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) <sup>[16]</sup>**


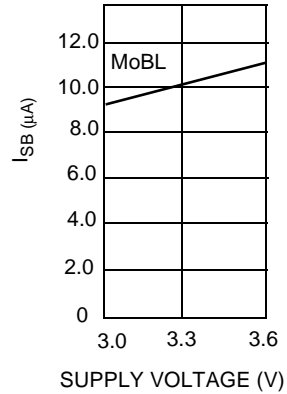
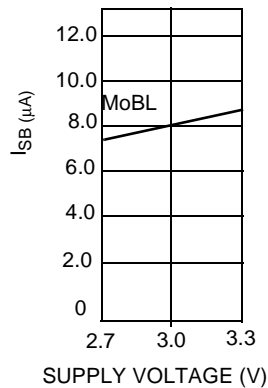
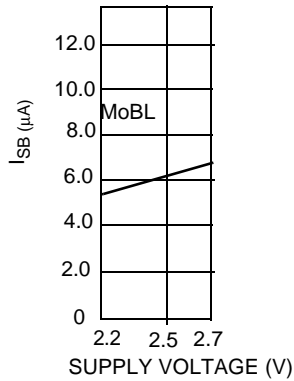
### Typical DC and AC Characteristics

(Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = V_{CC(typ.)}$ ,  $T_A = 25^\circ\text{C}$ .)

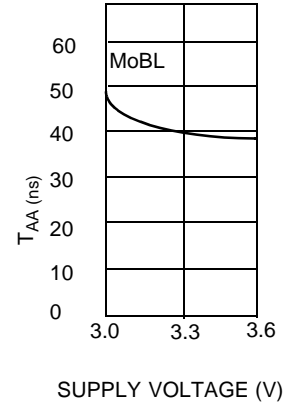
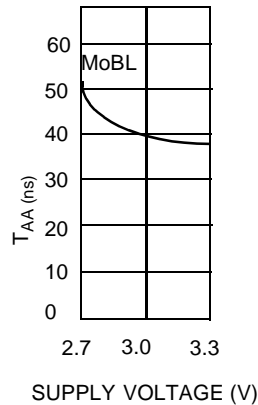
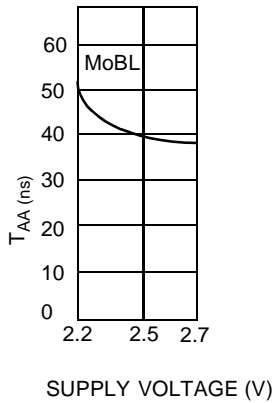
#### Operating Current vs. Supply Voltage



#### Standby Current vs. Supply Voltage



#### Access Time vs. Supply Voltage

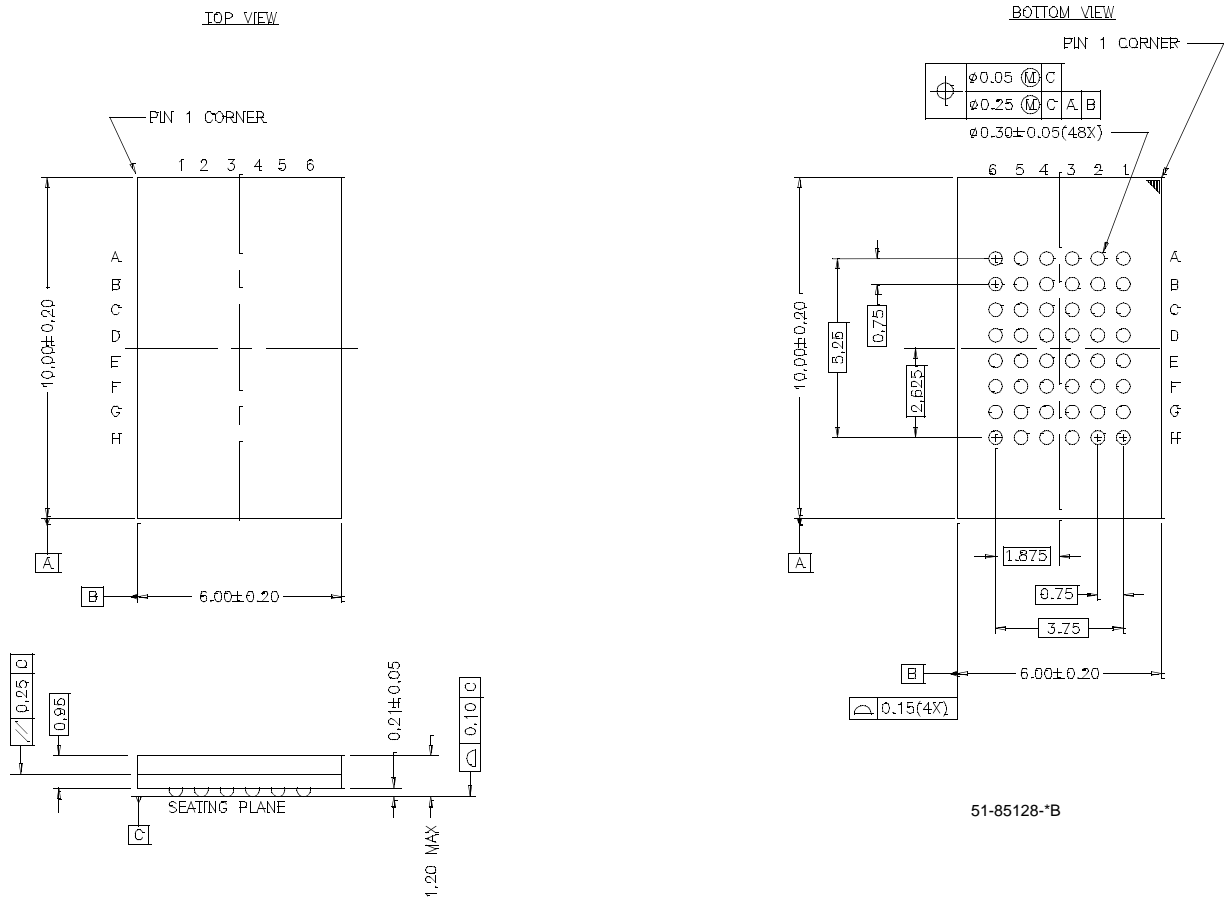


#### Truth Table

CE <sub>1</sub>	CE <sub>2</sub>	WE	OE	Inputs/Outputs	Mode	Power
H	X	X	X	High Z	Deselect/Power-Down	Standby ( $I_{SB}$ )
X	L	X	X	High Z	Deselect/Power-Down	Standby ( $I_{SB}$ )
L	H	H	L	Data Out (I/O <sub>0</sub> -I/O <sub>7</sub> )	Read	Active ( $I_{CC}$ )
L	H	H	H	High Z	Output Disabled	Active ( $I_{CC}$ )
L	H	L	X	Data in (I/O <sub>0</sub> -I/O <sub>7</sub> )	Write	Active ( $I_{CC}$ )

**Ordering Information**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CY62158CV25LL-70BAI	BA48F	48-Ball Fine Pitch BGA	Industrial
	CY62158CV30LL-70BAI			
	CY62158CV33LL-70BAI			
55	CY62158CV30LL-55BAI			
	CY62158CV33LL-55BAI			

**Package Diagrams**
**48-Ball (6 mm x 10 mm x 1.2 mm) FBGA BA48F**


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**	106361	05/22/01	MGN	New Data Sheet - Advance Information
*A	107773	07/16/01	MGN	Add 55 ns Bin to Advance Information
*B	111945	01/31/02	GAV	Advance to Final
*C	114219	05/01/02	GUG/ MGN	Improved Typical and Max Icc Values