OKI Semiconductor

MSM60802

PCMCIA Host Interface Controller

DESCRIPTION

The MSM60802 is OKI's first single-chip, highly integrated PC Card (PCMCIA) HostSide™ interface controller, offering compliancy with the PCMCIA 2.1, JEIDA 4.1, and ATA 1.01 industry standards. This device is optimized for usage in notebook and hand-held computers that require low-cost, single-socket support with extremely low power consumption for enhancing battery life. For small-form-factor designs, OKI delivers a minimum board-area solution by eliminating external buffers.

The HostSide™ controller is unique in several aspects, but most importantly regarding its register and software compatibility to the Intel 82365SL B step IC. Software compatibility significantly simplifies the design process and shortens time-to-market.

Plug-and-play compatibility is becoming more popular with PC Cards. The HostSide™ controller offers seamless transitions through full ExCA™ (QuickSwap) extensions. Another benefit of internal buffers is hot insertion capability.

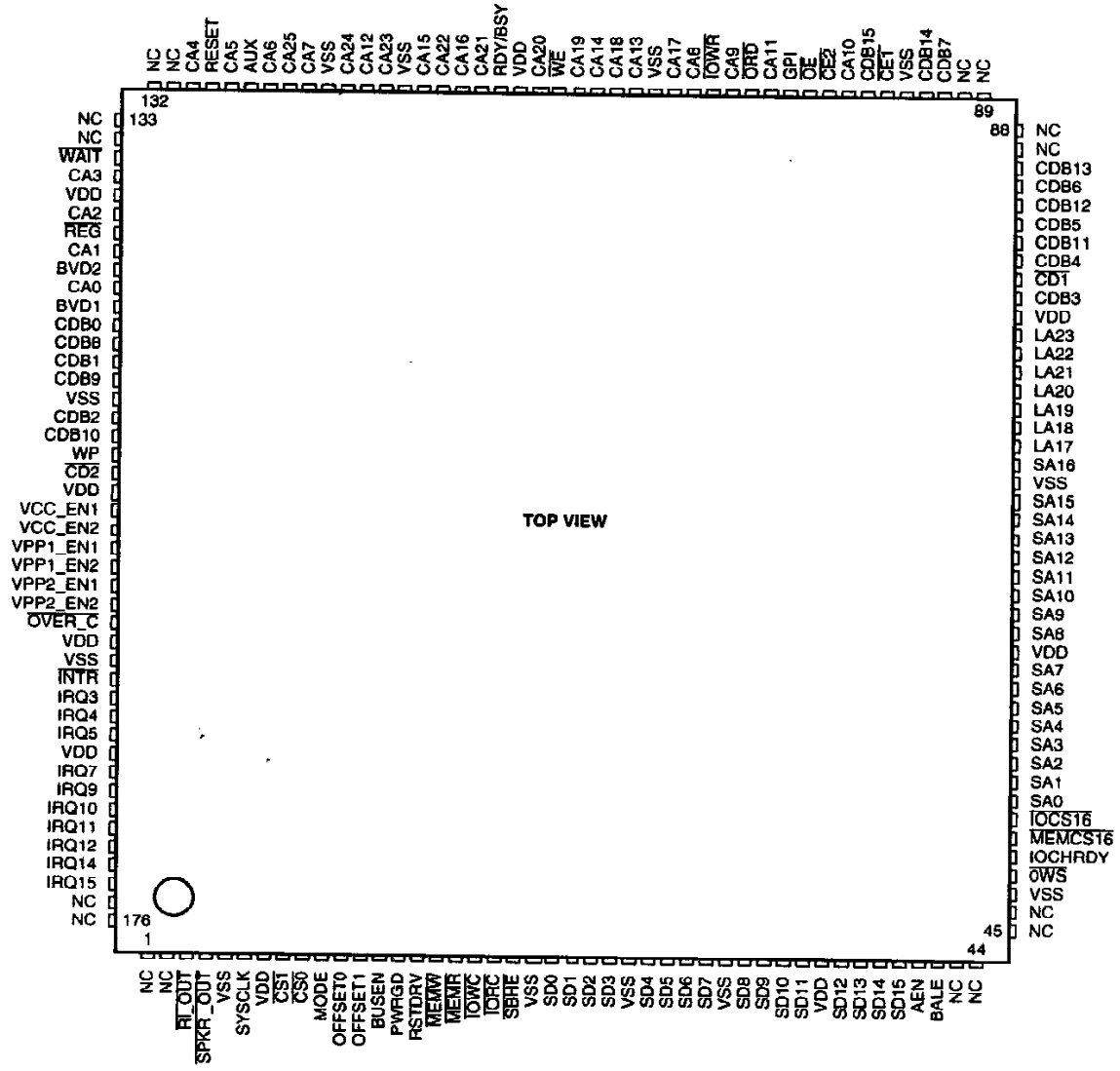
All necessary registers, decoders, and buffers are integrated to reduce the system form factor and to eliminate discrete components. A comprehensive interface allows device configuration, software setup, and firmware parameter setup by a host (PC) system.

The MSM60802 is manufactured on OKI's high-quality CMOS process, providing unrivaled low-power performance with a 3-V or 5-V operating range. Power-management circuitry further reduces power consumption through active monitoring techniques. In an effort to further reduce board space usage, the HostSide™ IC is offered in a 176-pin TQFP package.

FEATURES

- Single-chip PCMCIA host controller for reduced board space.
- Register- and software-compatible with Intel 82365SL B step PCMCIA controller for simplified design
- Mixed-voltage (3-V and 5-V) support, providing easy transition path
- Direct connection between ISA bus and PCMCIA socket for enhanced performance
- Compliant with PCMCIA 2.1, JEIDA 4.1, and ATA 1.01, facilitating compatibility
- ExCA™ compatible with hot-insertion compatibility
- Five independent, programmable memory windows per slot, meeting user requirements
- Two independent, programmable I/O windows per slot, simplifying partitioning
- Programmable access cycle timing, enhancing throughput
- Pulse- or level-mode interrupts, providing flexibility
- Execute-in-place (XIP) operation
- Programmable sleep modes for increased power savings
- 8-bit or 16-bit PCMCIA and CPU interface support for most architecture variations
- PCMCIA RESET compatibility, reducing design overhead
- 176-pin TQFP package, minimizing board space

PIN CONFIGURATION

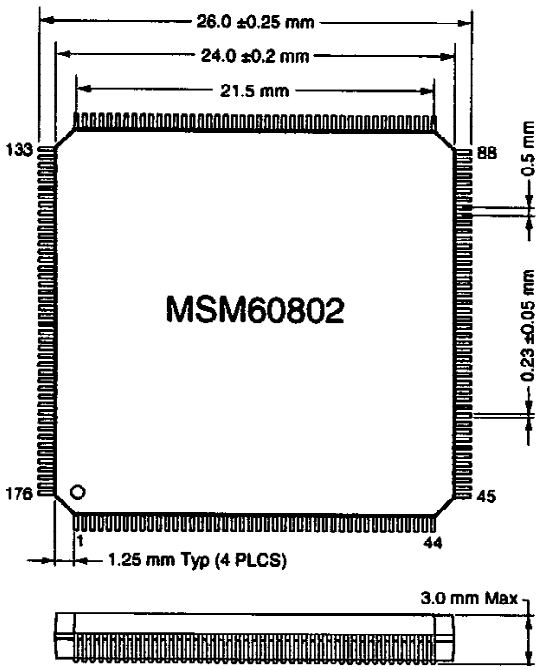


PIN LAYOUT

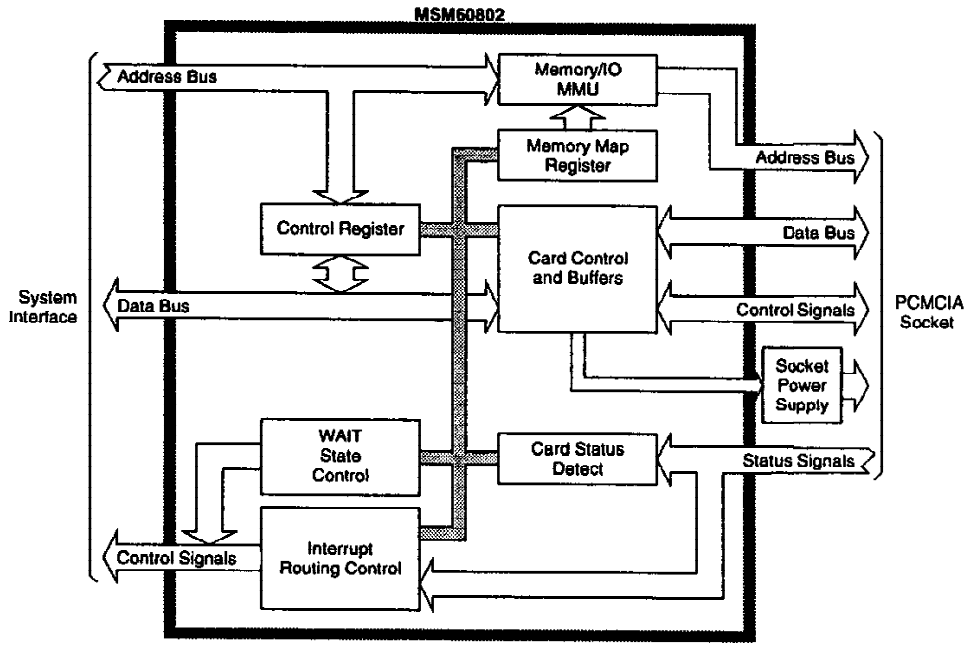
Pin	Pin Name	Pin	Pin Name	Pin	Pin Name	Pin	Pin Name	Pin	Pin Name	Pin	Pin Name
1	NC	31	VSS	61	SA8	91	CDB7	121	CA12	151	WP
2	NC	32	SD8	62	SA9	92	CDB14	122	CA24	152	$\overline{CD2}$
3	$\overline{RI\_OUT}$	33	SD9	63	SA10	93	VSS	123	VSS	153	VDD
4	$\overline{SPKR\_OUT}$	34	SD10	64	SA11	94	$\overline{CE1}$	124	CA7	154	VCC_EN1
5	VSS	35	SD11	65	SA12	95	CDB15	125	CA25	155	VCC_EN2
6	SYSCLK	36	VDD	66	SA13	96	CA10	126	CA6	156	VPP1_EN1
7	VDD	37	$\overline{SD12}$	67	SA14	97	$\overline{CE2}$	127	AUX	157	VPP1_EN2
8	$\overline{CS1}$	38	SD13	68	SA15	98	$\overline{OE}$	128	CA5	158	VPP2_EN1
9	$\overline{CS0}$	39	SD14	69	VSS	99	GPI	129	RESET	159	VPP2_EN2
10	MODE	40	SD15	70	SA16	100	CA11	130	CA4	160	$\overline{OVER\_C}$
11	OFFSET 0	41	AEN	71	LA17	101	$\overline{IORD}$	131	NC	161	VDD
12	OFFSET 1	42	BALE	72	LA18	102	CA9	132	NC	162	VSS
13	BUSEN	43	NC	73	LA19	103	$\overline{IOWR}$	133	NC	163	$\overline{INTR}$
14	PWRGD	44	NC	74	LA20	104	CA8	134	NC	164	IRQ3
15	RSTDRV	45	NC	75	LA21	105	CA17	135	$\overline{WAIT}$	165	IRQ4
16	$\overline{MEMW}$	46	NC	76	LA22	106	VSS	136	CA3	166	IRQ5
17	$\overline{MEMR}$	47	VSS	77	LA23	107	CA13	137	VDD	167	VDD
18	$\overline{IOWC}$	48	$\overline{OWS}$	78	VDD	108	CA18	138	CA2	168	IRQ7
19	$\overline{IORC}$	49	IOCHRDY	79	CBD3	109	CA14	139	$\overline{REG}$	169	IRQ9
20	$\overline{SBHE}$	50	$\overline{MEMCS16}$	80	$\overline{CD1}$	110	CA19	140	CA1	170	IRQ10
21	VSS	51	$\overline{IOCS16}$	81	CDB4	111	$\overline{WE}$	141	BVD2	171	IRQ11
22	SD0	52	SA0	82	CDB11	112	CA20	142	CA0	172	IRQ12
23	SD1	53	SA1	83	CDB5	113	VDD	143	BVD1	173	IRQ14
24	SD2	54	SA2	84	CDB12	114	RDY/BSY	144	CDB0	174	IRQ15
25	SD3	55	SA3	85	CDB6	115	CA21	145	CDB8	175	NC
26	VSS	56	SA4	86	CDB13	116	CA16	146	CDB1	176	NC
27	SD4	57	SA5	87	NC	117	CA22	147	CDB9		
28	SD5	58	SA6	88	NC	118	CA15	148	VSS		
29	SD6	59	SA7	89	NC	119	VSS	149	CDB2		
30	SD7	60	VDD	90	NC	120	CA23	150	CDB10		

PACKAGE DIAGRAM

176-Pin
Thin Quad Flat Pack
(TQFP)



BLOCK DIAGRAM



PIN DESCRIPTIONS

Pin Name	Direction and Strength	Description
AEN	Input	**System Address Enable.** This active-HIGH input signal should be connected to the AEN signal on the ISA bus. If the system asserts this signal HIGH, access to I/O and the internal MSM60802 registers is disabled, $\overline{CE1}$ and $\overline{CE2}$ are asserted LOW, and memory access is enabled. If the system deasserts this signal LOW, access to I/O and internal registers is also enabled.
AUX	I/O 4 mA	**Auxiliary.** This is a multi-purpose I/O pin for user applications.
BALE	Input	**Bus Address Latch Enable.** This active-HIGH input signal should be connected to the BALE signal on the ISA bus. The system asserts this signal HIGH at the beginning of every bus cycle to latch the address from the system address bus, SA[23:17].
BUSEN	Output 4 mA	**Bus Enable.** If the PCMCIA bus is enabled, the MSM60802 asserts this signal LOW.
BVD1 ($\overline{STSCHG}$)	Input	This is a dual-function PCMCIA pin with different characteristics on memory and configured I/O cards. **Battery Status 1.** On memory cards, this signal indicates a low battery on the PC card. If the BVD1 bit in the *Card Status Interrupt Configuration Register* (see page 19) is set to '1' then the interrupt selected by the IRQ_Sx bit in this register is requested. The BVD1_CH bit in the *Card Status Flag Register* (see page 18) is also set to '1' on the falling edge of BVD1. **Status Changed.** On configured I/O cards, the card signals a change of its status by setting this signal LOW. If the BVD1 bit in the *Card Status Interrupt Configuration Register* (see page 19) is set to '1' then the interrupt selected by the IRQ_Sx bit in this register is requested. The BVD1_CH bit in the *Card Status Flag Register* (see page 18) is also set to '1' on the falling edge of $\overline{STSCHG}$, and the MSM60802 asserts the $\overline{RI\_OUT}$ signal LOW when the $\overline{STSCHG}$ input is LOW.
BVD2 ($\overline{SPKR}$)	Input	This is a dual-function PCMCIA pin with different characteristics on memory and configured I/O cards. **Battery Status 2.** On memory cards, this signal indicates a low battery on the PC card. If the BVD2 bit in the Card Status *Interrupt Configuration Register* (see page 19) is set to '1' then the interrupt selected by the IRQ_Sx bit in this register is requested. The BVD2_CH bit in the *Card Status Flag Register* (see page 18) is also set to '1' on the falling edge of BVD1. **Digital Audio.** On I/O cards, the PC card can use this signal to transmit digital audio signals to the host system. When configured for I/O card operation, no interrupt is generated when the level of $\overline{SPKR}$ changes and the BVD2_CH bit in the Card Status Flag Register is set to '0' continuously.
CA[25:0]	3-state Output 4 mA	**Card Address Bus.** This signal directly connects to the PCMCIA socket's A[25:0] signals.
CDB[15:0]	I/O 4 mA	**Card Data Bus.** This signal directly connects to the PCMCIA socket's D[15:0] signals.
$\overline{CD1}$, $\overline{CD2}$	Input Schmitt Trigger 50 kΩ pull-up	**Card Detect.** When no card is present, these signals are pulled HIGH. An inserted card pulls both of these signals LOW. See Register Index 04H and 05H for details.
$\overline{CE1}$, $\overline{CE2}$	3-state Output 4 mA	**Card Enable.** The MSM60802 asserts these signals LOW to enable the PC card for read and write accesses.
$\overline{CS1}$, $\overline{CS0}$	Input 50 kΩ pull-down	**External I/O Address Decode.** If the MSM60802 MODE signal input is not asserted HIGH, the $\overline{CS1}$ and $\overline{CS0}$ signals select the system addresses for the MSM60802 *Register Select Register* and the *Data Transfer Register*. Four addresses are selectable via the CS0 and CS1 pins, allowing users to hard-wire or configure jumpers for selection of MSM60802 register addresses that avoid potential address conflicts. See also the description for the MODE signal input.

$\overline{CS0}$	$\overline{CS1}$	Address (Hex)	
		Register Select Register	Data Transfer Register
0	0	3E0	3E1
0	1	3E2	3E3
1	0	240	241
1	1	100	101

PIN DESCRIPTIONS (Continued)

Pin Name	Direction and Strength	Description
GPI	Input	**General Purpose Input.** The MSM60802 images the inverted state of this input pin in bit D7 of the *Card Status Register* (see page 15). If the GPI_EN bit in the *Card Detect and General Control Register* (see page 28) is set to '1,' then a transition on this input can generate a card status-change interrupt. The GPI_TC bit in the same register controls the direction of signal change that causes an interrupt.
$\overline{\text{INTR}}$	3-state Output 8 mA	**Interrupt Request.** This active-LOW output should be connected to a system interrupt signal, i.e., the system signal $\overline{\text{ETSMI}}$. The $\overline{\text{INTR}}$ signal is used to require a maskable interrupt from the system CPU. If the MSM60802 asserts $\overline{\text{INTR}}$ LOW, all other status interrupt requests (IRQ's) are disabled.
IOCHRDY	3-state Output 16 mA	**I/O Channel Ready.** This active-HIGH output should be connected to the host signal IOCHRDY. When asserted HIGH, this output indicates that the current I/O read or write cycle is completed. If the PCMCIA signal $\overline{\text{WAIT}}$ signal is active, or the MSM60802 is programmed to insert WAIT states, the MSM60802 will reflect this by deasserting the IOCHRDY signal LOW.
$\overline{\text{IOCS16}}$	3-state Output 16 mA	**I/O Chip Select 16.** This active-LOW output signal should be connected to the host signal $\overline{\text{IOCS16}}$. The $\overline{\text{IOCS16}}$ signal is generated either by the MSM60802 or by the PC card. When asserted LOW, this signal indicates that 16-bit I/O cycles can be performed.
$\overline{\text{IORC}}$	Input	**I/O Read Cycle.** This active-LOW input signal should be connected to the host signal $\overline{\text{IORC}}$. If the accessed address is in the configured and enabled I/O window, the MSM60802 performs a PCMCIA I/O read cycle to the PC I/O card when this signal is asserted LOW.
$\overline{\text{IORD}}$	3-state Output 4 mA	**I/O Read.** This active-LOW signal indicates that the MSM60802 is performing an I/O read access to the PC card.
$\overline{\text{IOWC}}$	Input	**I/O Write Cycle.** This input signal should be connected to the host signal $\overline{\text{IOWC}}$. If the accessed address is in the configured and enabled I/O window, the MSM60802 performs a PCMCIA I/O write cycle to the PC I/O card when this signal is asserted LOW.
$\overline{\text{IOWR}}$	3-state Output 4 mA	**I/O Write.** This active-LOW signal indicates that the MSM60802 is performing an I/O write access to the PC card.
$\overline{\text{IREQ}}$	Input	**Interrupt Request.** See the signal description for RDY/ BSY ($\overline{\text{IREQ}}$).
IRQ[15:14] IRQ[12:9] IRQ[7] IRQ[5:3]	3-state Output 8 mA	**Interrupt Request.** These output signals should be connected to the equivalent signals of the host system. The PCMCIA interrupt request is routed to one of these interrupt signals. The system can choose the interrupt signal by writing a configuration into IRQ_Cx bits in the *Interrupt and General Control Register* (see page 17). A status change of the PC card might also force a system interrupt, if this function is enabled in the *Card Status Interrupt Configuration Register* (see page 19).
LA[23:17] SA[16:0]	Input	**Local Address Bus and System Address Bus.** These signals should be connected to the system address bus, SA[16:0] and LA[23:17]. LA23 is the most-significant and SA0 is the least-significant bit. If connected to an 8-bit ISA bus, LA[19:17] should be connected to SA[19:17] of the ISA bus and LA[23:20] must be pulled down.
$\overline{\text{MEMCS16}}$	3-state Output 16 mA	**Memory Chip Select 16-Bit.** This output signal should be connected to the host signal $\overline{\text{MEMCS16}}$. The MSM60802 asserts this signal LOW to indicate that a 16-bit memory cycle can be performed. The signal is decoded from the system address and is controlled by the MCS bit in the *Address Window Enable Register* (see page 20).
$\overline{\text{MEMR}}$	Input	**System Memory Read.** This input signal should be connected to the host signal $\overline{\text{MEMR}}$. If the accessed address is in the configured and enabled memory window, the MSM60802 performs a PCMCIA memory read cycle to the PC card attribute or common memory when this signal is asserted LOW.
$\overline{\text{MEMW}}$	Input	**System Memory Write.** This input signal should be connected to the host signal $\overline{\text{MEMW}}$. If the accessed address is in the configured and enabled memory window, the MSM60802 performs a PCMCIA memory write cycle to the PC card attribute or common memory when this signal is asserted LOW.

PIN DESCRIPTIONS (Continued)

<table>
<tr><th>Pin Name</th><th>Direction and Strength</th><th>Description</th></tr>
<tr><td>MODE</td><td>Input
50 kΩ pull-up</td><td>Mode Select. When asserted HIGH, this input makes the $\overline{CS0}$ and $\overline{CS1}$ inputs select addresses for the Register Select Register and Data Transfer Register. When deasserted LOW, the system addresses for the Register Select Register and the Data Transfer Register are decoded externally. For external decoding, the CS1 input must be tied LOW. See the table below.
<table>
<tr><th>Mode</th><th>$\overline{CS0}$</th><th>$\overline{CS1}$</th><th>Register Select Register</th><th>Data Transfer Register</th></tr>
<tr><td>1</td><td>x</td><td>x</td><td colspan="2">See Signal Description for $\overline{CS0}$ and $\overline{CS1}$</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>A0 = 0</td><td>A0 = 1</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Not selected</td><td>Not selected</td></tr>
</table></td></tr>
<tr><td>$\overline{OE}$</td><td>3-state Output
4 mA</td><td>Output Enable. This active-LOW signal indicates that the MSM60802 is performing a read access to the PC card's common memory or attribute memory.</td></tr>
<tr><td>OFFSET [1:0]</td><td>Input
50 kΩ pull-down</td><td>Index Offset Control. These input signals allow four different address offsets for the MSM60802 Status and Control Registers. The table below shows available offset values for the register addresses. Refer to the subsection "Status and Control Registers" on page 12 for more information.
<table>
<tr><th>OFFSET1</th><th>OFFSET0</th><th>Offset</th></tr>
<tr><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>40 Hex</td></tr>
<tr><td>1</td><td>0</td><td>80 Hex</td></tr>
<tr><td>1</td><td>1</td><td>C0 Hex</td></tr>
</table></td></tr>
<tr><td>$\overline{OVER\_C}$</td><td>Input
Schmitt Trigger
50 kΩ pull-up</td><td>Overcurrent Input Pin. If the OVER_CS and OVER_EN bits in the Card Detect and General Control Register (see page 28) are set to '1,' then a falling edge at this input switches off the power supply via the power control pins and forces a status change interrupt.</td></tr>
<tr><td>PWRGD</td><td>Input
Schmitt Trigger
50 kΩ pull-up</td><td>Power Good. This active-HIGH signal should be connected to the host signal that indicates a good system supply voltage. If the system is asserting PWRGD HIGH and the bit DIS_RES in the Card Bus and Power Control Register (see page 16) is set to '1,' then the reset signal RSTDRV is ignored.</td></tr>
<tr><td>RDY/ BSY ($\overline{IREQ}$)</td><td>Input</td><td>This is a dual-function PCMCIA pin with different characteristics on memory and configured I/O cards.
Ready/Busy. On memory cards, the PC card pulls this signal LOW to indicate that it is still busy after a reset has been forced. Pulling the RDY/BSY signal clears the RDY/BSY bit in the Card Status Register (see page 15). When the RDY/BSY bit in the Card Status Register is set to '1,' the PC card is ready and may be accessed. The RDY/BSY bit is set to '1' continuously if the socket is configured for I/O operations.
Interrupt Request. On I/O cards, the PC card can request a host system interrupt by asserting this signal LOW. The IRQ_Cx bits in the Interrupt and General Control Register (see page 17) select the generated interrupt level. The MSM60802 then generates an interrupt back to the host via the selected IRQ.</td></tr>
<tr><td>$\overline{REG}$</td><td>3-state Output
4 mA</td><td>Register Select and I/O Enable. This MSM60802 sets this signal HIGH (not active) for common memory operations and drives this signal active LOW for I/O and attribute memory operations. For I/O operations, this signal is generated by the MSM60802 automatically. For attribute memory access, the $\overline{REG}$ bit in the Card Memory Offset Address High Byte Register (see page 27) must be set to '1.'</td></tr>
<tr><td>RESET</td><td>3-state Output
4 mA</td><td>Card Reset. The MSM60802 asserts this signal HIGH level to force a hardware reset on the PC card. If the C_RESET bit in the Interrupt and General Control Register (see page 17) is cleared to '0,' then the RESET output is asserted HIGH. Setting the C_RESET bit to '1' deasserts the RESET signal.</td></tr>
<tr><td>$\overline{RI\_OUT}$</td><td>3-state Output
8 mA</td><td>Ring Indicate (Wakeup). For systems with configured I/O cards, the MSM60802 asserts this signal LOW to signal to the host system that it should switch from sleep mode to active mode. The $\overline{RI\_OUT}$ signal reflects the status of the $\overline{STSCHG}$ signal received from a configured I/O PC card via the $\overline{STSCHG}$ input.</td></tr>
<tr><td>RSTDRV</td><td>Input
Schmitt Trigger</td><td>System Cold Reset. This input signal should be connected to the host signal RSTDRV. The system can reset the MSM60802 by asserting this signal HIGH. If the Power Good signal, PWRGD, is HIGH and the DIS_RES bit in the Card Bus and Power Control Register (see page 16) is set to '1,' the MSM60802 will ignore RSTDRV.</td></tr>
</table>

PIN DESCRIPTIONS (Continued)

Pin Name	Direction and Strength	Description
$\overline{SBHE}$	Input	**System Bus High Enable.** This input signal should be connected to the host signal $\overline{SBHE}$. The system drives this signal LOW to indicate that the upper byte of data on the data bus is valid. If this signal is deasserted HIGH, the MSM60802 will only perform 8-bit cycles to the PCMCIA socket.
SA[16:0]	Input	**System Address Bus.** See the signal description for LA[23:17].
SD[15:0]	I/O 8 mA	**System Data Bus.** These bidirectional signals should be connected to the system data bus, SD[15:0].
$\overline{SPKR}$	Input	**Speaker In.** See the signal description for BVD2 ($\overline{SPKR}$).
SPKR_OUT	3-state Output 8 mA	**Speaker Out.** To perform digital audio functions, this output passes through the signal received at the $\overline{SPKR}$ input from a configured PC I/O card. The output can be disabled with the D2 bit of the Extension Register (Index 0FFH).
$\overline{STSCHG}$	Input	**Status Changed.** For information, see the signal description for BVD1 ($\overline{STSCHG}$).
SYSCLK	Input	**System Clock.** This input signal should be connected to the host system's CLOCK signal. The MSM60802 supports clock frequencies in the 4.77-MHz to 8.33-MHz range. The clock frequency effects the timings by changing the pulse width of $\overline{INTR}$ (three SYSCLK cycles), and the delays for 16-bit $\overline{MEMR}$ and 16-bit $\overline{MEMW}$ operations.
VCC_EN1 VCC_EN2	Output 8 mA	**V_{CC} Power Enable.** The MSM60802 asserts this LOW to activate PC card V_{CC} power.
VPP1_EN1 VPP1_EN2	Output 8 mA	**V_{PP1} Power Enable.** This signal is active HIGH.
VPP2_EN1 VPP2_EN2	Output 8 mA	**V_{PP2} Power Enable.** This signal is active HIGH
$\overline{WAIT}$	Input	**Extend Bus Cycle.** The PC card can activate this active-LOW signal to extend a memory or I/O cycle.
$\overline{WE}$	3-state Output 4 mA	**Write Enable.** This active-low signal indicates a write access to the common memory or attribute memory of the PC card.
WP ($\overline{IOIS16}$)	Input	**Write Protect.** By pulling this signal high, the PC card indicates that the card is write protected. The MSM60802 will not qualify this signal. To prevent write access, the WP_EN bit in the Card Memory Offset Address High Byte Register has to be set. **I/O port is 16-bit.** The PC card indicates if a addressed I/O port is capable of 16-bit accesses by asserting this signal LOW.
$\overline{OWS}$	3-state Output 16 mA	**Zero WAIT State.** This signal (active low) should be connected to the host system signal $\overline{OWS}$. It indicates that the system should execute cycles with no extra WAIT states. It is controlled by Ix_ZWS (I/O Control Register) and ZWS (Memory Window x Start Address High Byte Register).

FUNCTIONAL DESCRIPTION

The following information describes the MSM60802 main function blocks.

MEM/IO MMU

The Memory Management Unit (MMU) is controlled by the Memory Map Register and decodes the system addresses LA[23:17] and SA[16:0]. If addresses are accessed within a configured memory or I/O window, the memory management unit transfers the access to the PCMCIA socket. For memory address operations, the MMU adds the configured address offset to the system address.

Memory Map Register

The Memory Map Registers control MEM/IO MMU. The system address windows must be defined by writing to these registers. Five memory windows and two I/O windows can be defined simultaneously.

Control Registers

Control Registers interface between the internal function blocks of the MSM60802 and the host system. By reading or writing the Control Registers, the MSM60802 and the PCMCIA Interface can be configured.

To access a control register, the system must at first select this register by writing the register's index number into the Register Select Register. To read or write the selected register, the system must access the Data Transfer Register. Both system addresses of the Register Select Register and the Data Transfer Register are adjustable by two chip select signals.

Card Control and Buffers

If the MEM/IO MMU detects a valid memory or I/O cycle to the PC card, the card control and buffers function block generates all necessary control signals, such as card enables, and then connects the data bus to the PC card. This function block also drives signals for switching the PCMCIA socket power supply.

Card Status Detect

The Card Status Detect function block monitors the PCMCIA interface status signals state, similar to STSCHG, and automatically sets flags in the control register if a status has change. The interface and card status is imaged in the Card Status Register and in the Card Status Flag Register.

Interrupt Routing Control

If a PCMCIA I/O card requests a system interrupt, the Interrupt Routing Control function block transfers this request to a system interrupt signal. The same system interrupt signal must be selected and enabled from the MSM60802 control register.

If a PCMCIA status signal changes and Interrupt Routing Control is configured, the function block activates a system interrupt signal.

Interrupt routing is controlled by the Interrupt and General Control Register and the Card Status Interrupt Configuration Register. By using control bits in the Global Control Register, the active level and mode (pulse or level interrupt) are selectable.

WAIT State Control

The WAIT State Control function block can generate additional WAIT states, if this function is enabled by the system and if the PC card so requests. The WAIT state generator is clocked by the signal SYSCLK. The WAIT State Control functions can be configured in the I/O Control Register and in the Memory Window Start Address High Byte. The PC card memory access signals ($\overline{OE}$, $\overline{WE}$) can be synchronously delayed by the SYSCLK or the inverted SYSCLK.

PC Card Addressing

Memory Operations

The PCMCIA interface can address a total address space of 64 Mbytes of common memory and/or attribute memory. The ISA bus system is capable of addressing a 16-Mbyte memory space.

The MSM60802 can map parts of the PCMCIA memory space into the host system's address space. The system can define memory windows by writing the start and the stop address (system address) of the required memory window and an offset into MSM60802 registers. The start address is the first system address of the memory window that the system uses to access the PC card. The stop address is the last system address of the same memory window.

The PCMCIA address is calculated by the MSM60802 by adding the offset to the actual system address. If the system address is greater or equal to the window start address and lower or equal to the window stop address, the MSM60802 performs a memory access to the PC card.

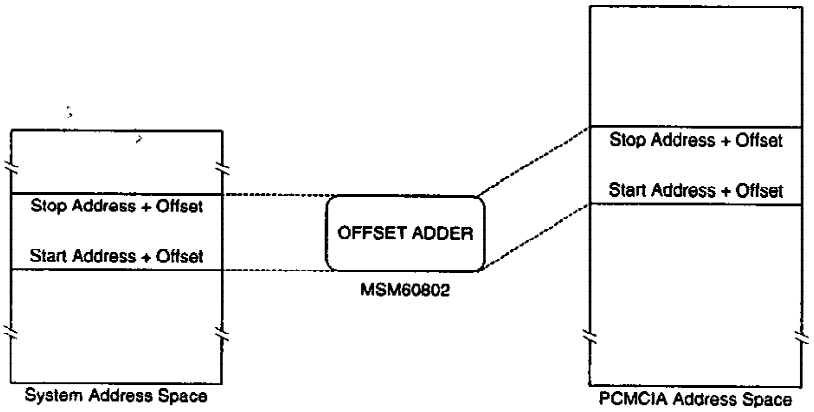


Figure 1. PC Card Memory Window Addressing

Each 4-Kbyte boundary above 64 Kbyte can be used as a memory window start address. The start address must be configured in the Memory Window x Start Address Low Byte and Memory Window x Start Address High Byte register. The stop address must be written to the Memory Window x Stop Address Low Byte and Memory Window x Stop Address High Byte register. The offset must be written into the Card Memory Offset Address x High Byte and Card Memory Offset Address x Low Byte register.

Using the MSM60802, the system can configure five of these memory windows simultaneously. Each window can be enabled separately. The card address is calculated as the two's complement of the system address and the offset. Refer to the following table for an example.

Memory Start Address	Memory Stop Address	Offset	PC Card Start Address	PC Card Stop Address
1Exxx Hex	1Fxxx Hex	0xxx Hex	1Exxx Hex	1Fxxx Hex
1Exxx Hex	1Fxxx Hex	1xxx Hex	1Fxxx Hex	20xxx Hex
1Exxx Hex	1Fxxx Hex	3FFE2xxx Hex	00xxx Hex	01xxx Hex

When a system memory window is defined by start address and stop address, the whole PC card address space can be addressed by changing the offset. It is not necessary to define the start and stop address again. To access the attribute memory of a PC card, the system must set the $\overline{REG}$ bit inside the Card Memory Offset Address x High Byte register. Memory windows should not be overlapped.

I/O Operations

For I/O operations, the system is allowed to use each address within the first 64 Kbytes of the system address space. The system must also define a system start address and a system stop address; for I/O operations, however, the MSM60802 adds no offset to the system address. If the system indicates a valid I/O cycle, and if the system address is greater or equal to the defined start address and lower or equal to the defined stop address, the MSM60802 transfers the system address to the PCMCIA socket.

The system must write the start address into the I/O Window x Start Address Low Byte and I/O Window x Start Address High Byte Register and the stop address into the I/O Window x Stop Address Low Byte and I/O Window x Stop Address High Byte register.

Using the MSM60802, the system can handle two I/O address windows simultaneously. Both windows can be enabled separately. It is possible to open both types of address windows (I/O windows and memory windows) simultaneously.

REGISTERS

MSM60802 Control Register Addressing

The host system can control the functions and the status of the MSM60802 and connected PCMCIA socke via 50 eight-bit-wide control registers. These control registers inside the MSM60802 are addressed indi rectly. To address a register, the register's index must be written into the Register Select Register. By read ing or writing the Data Transfer Register, the system can read or change the contents of the selecte register.

The system addresses of the Register Select Register and of the Data Transfer Register can be determine by the MSM60802 $\overline{CS1}$ and $\overline{CS0}$ input signals and the MODE signal.

Mode	$\overline{CS0}$	$\overline{CS1}$	Register-Select-Register	Data-Transfer-Register
1	0	0	3E0 Hex	3E1 Hex
1	0	1	3E2 Hex	3E3 Hex
1	1	0	240 Hex	241 Hex
1	1	1	100 Hex	101 Hex
0	0	1	A0 = 0 (external mode)	A0 = 1 (external decode)
0	1	1	Not selected	Not selected

Status and Control Registers

The table on the next page shows all status and control registers, and the index that the host must write into the Register Select Register to access them. The OFFSET[1:0] input pins define the offset that must be added to the index address to access the control registers, as shown in the table below.

OFFSET1	OFFSET0	Offset
0	0	0
0	1	40 Hex
1	0	80 Hex
1	1	C0 Hex

Status and Control Registers

Index	Direction	Register Name
00h + Offset	Read only	Revision Number
01h + Offset	Read only	Card Status
02h + Offset	Read/Write	Card Bus and Power Control
03h + Offset	Read/Write	Interrupt and General Control
04h + Offset	Read only	Card Status Flag
05h + Offset	Read/Write	Card Status Interrupt Configuration
06h + Offset	Read/Write	Address Window Enable
07h + Offset	Read/Write	I/O Control
08h + Offset	Read/Write	I/O Window 0 Start Address Low Byte
09h + Offset	Read/Write	I/O Window 0 Start Address High Byte
0Ah + Offset	Read/Write	I/O Window 0 Stop Address Low Byte
0Bh + Offset	Read/Write	I/O Window 0 Stop Address High Byte
0Ch + Offset	Read/Write	I/O Window 1 Start Address Low Byte
0Dh + Offset	Read/Write	I/O Window 1 Start Address High Byte
0Eh + Offset	Read/Write	I/O Window 1 Stop Address Low Byte
0Fh + Offset	Read/Write	I/O Window 1 Stop Address High Byte
10h + Offset	Read/Write	Memory Window 0 Start Address Low Byte
11h + Offset	Read/Write	Memory Window 0 Start Address High Byte
12h + Offset	Read/Write	Memory Window 0 Stop Address Low Byte
13h + Offset	Read/Write	Memory Window 0 Stop Address High Byte
14h + Offset	Read/Write	Card Memory Offset Address 0 Low Byte
15h + Offset	Read/Write	Card Memory Offset Address 0 High Byte
16h + Offset	Read/Write	Card Detect and General Control
17h + Offset	Read/Write	Reserved
18h + Offset	Read/Write	Memory Window 1 Start Address Low Byte
19h + Offset	Read/Write	Memory Window 1 Start Address High Byte
1Ah + Offset	Read/Write	Memory Window 1 Stop Address Low Byte
1Bh + Offset	Read/Write	Memory Window 1 Stop Address High Byte
1Ch + Offset	Read/Write	Card Memory Offset Address 1 Low Byte
1Dh + Offset	Read/Write	Card Memory Offset Address 1 High Byte
1Eh + Offset	Read/Write	Global Control Register
1Fh + Offset	Read/Write	Reserved
20h + Offset	Read/Write	Memory Window 2 Start Address Low Byte
21h + Offset	Read/Write	Memory Window 2 Start Address High Byte
22h + Offset	Read/Write	Memory Window 2 Stop Address Low Byte
23h + Offset	Read/Write	Memory Window 2 Stop Address High Byte
24h + Offset	Read/Write	Card Memory Offset Address 2 Low Byte
25h + Offset	Read/Write	Card Memory Offset Address 2 High Byte
26h + Offset	Read/Write	Reserved

Status and Control Registers (Continued)

Index	Direction	Register Name
27h + Offset	Read/Write	Reserved
28h + Offset	Read/Write	Memory Window 3 Start Address Low Byte
29h + Offset	Read/Write	Memory Window 3 Start Address High Byte
2Ah + Offset	Read/Write	Memory Window 3 Stop Address Low Byte
2Bh + Offset	Read/Write	Memory Window 3 Stop Address High Byte
2Ch + Offset	Read/Write	Card Memory Offset Address 3 Low Byte
2Dh + Offset	Read/Write	Card Memory Offset Address 3 High Byte
2Eh + Offset	Read/Write	Reserved
2Fh + Offset	Read/Write	Reserved
30h + Offset	Read/Write	Memory Window 4 Start Address Low Byte
31h + Offset	Read/Write	Memory Window 4 Start Address High Byte
32h + Offset	Read/Write	Memory Window 4 Stop Address Low Byte
33h + Offset	Read/Write	Memory Window 4 Stop Address High Byte
34h + Offset	Read/Write	Card Memory Offset Address 4 Low Byte
35h + Offset	Read/Write	Card Memory Offset Address 4 High Byte
36h + Offset	Read/Write	Reserved
37h + Offset	Read/Write	Reserved
38h + Offset	Read/Write	Reserved
39h + Offset	Read/Write	Reserved
3Ah + Offset	Read/Write	Reserved
3Bh + Offset	Read/Write	Reserved
3Ch + Offset	Read/Write	Reserved
3Dh + Offset	Read/Write	Reserved
3Eh + Offset	Read/Write	Clock Register
3Fh + Offset	Read/Write	Extension Register

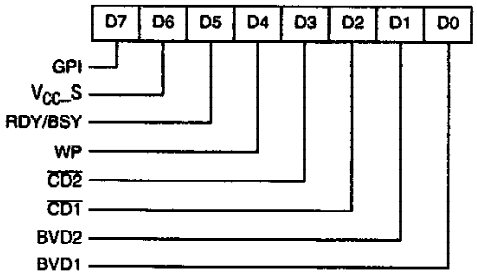
CONTROL AND STATUS REGISTERS

This section contains descriptions of the Control and Status Registers.

Revision Number Register
Index: 00 Hex

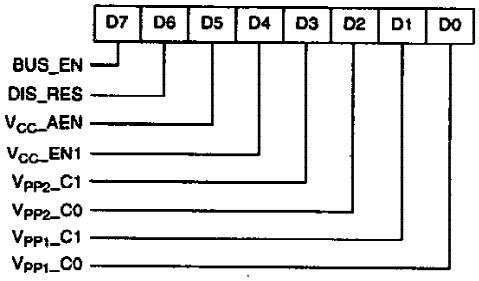
The Revision Number Register indicates the release of the MSM60802 (93 Hex).

Card Status Register
Index: 01 Hex



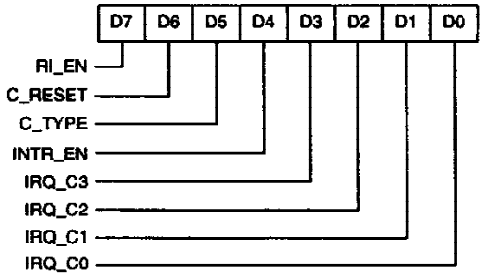
Bit(s)	Card Status Register Description
D7 GPI	**General Purpose Input.** This bit images the inverted state of the input signal GPI.
D6 V_{CC}_S	**V_{CC} Power Control.** V_{CC}_S = 0 indicates that the supply and programming voltages V_{CC}, V_{PP1} and V_{PP2} of the PCMCIA socket are turned off. V_{CC}_S = 1 indicates that V_{CC}, V_{PP1} or V_{PP2} are turned on. The value of the voltage is defined in the Card Bus and Power Control Register.
D5 RDY/BSY	**Ready / Busy.** RDY/BSY = 0 indicates that the socket is not ready; access to the PC card is not allowed. RDY/BSY = 1 indicates that the PC card is ready and be accessible. If the socket is configured for I/O operations, RDY/BSY is permanently set to '1.'
D4 WP	**Write Protect.** WP = 0 indicates that the inserted memory card is not write protected. WP = 1 indicates that the inserted memory card is write protected. If the socket is configured for I/O operations, the signal is permanently set at '0.'
D3, D2 $\overline{CDx}$	**Card Detect.** Card Detect 2 ($\overline{CD2}$), Card Detect 1 ($\overline{CD1}$). $\overline{CD1}$ = 0 indicates that the PCMCIA socket is empty. $\overline{CD2}$, $\overline{CD1}$ = 1 indicates that a PC card has been inserted into the socket.
D1, D0 BVDx	**Battery Status.** BVD2 (Battery Status 2) and BVD1 (Battery Status 1) indicate the memory card battery state, as shown in the example below. If the PCMCIA interface is configured for I/O operations, BVD2 is permanently set at '1', with BVD1 reflecting the state of STSCHG. BVD1 = 0; BVD2 = 0 → Battery Dead BVD1 = 0; BVD2 = 1 → Battery Dead BVD1 = 1; BVD2 = 0 → Battery Low BVD1 = 1; BVD2 = 1 → Battery Good

Card Bus and Power Control Register
Index: 02 Hex



Bit(s)	Card Bus and Power Control Description
D7 BUS_EN	**Bus Enable.** Set this bit to '0' to switch all control signals, address signals, and data signals to the PCMCIA socket into 3-state mode. If this bit is set to '1,' the bus from the MSM60802 to the PCMCIA socket switches into active mode.
D6 DIS_RES	**Disable Reset.** The system sets this bit to '0' to force a reset by RSTDRV and to reset all resettable registers. The system sets this bit to '1' for the MSM60802 to ignore the RSTDRV signal, as long as PWRGD is '1.'
D5 V_{CC}_AEN	**System Address Enable.** The system sets this bit to '0' if the supply voltage V_{CC} of the socket must be switched on, by setting V_{CC}_EN = '1'. The system sets this bit to '1' if the socket supply voltage V_{CC} will be automatically switched on after detection of the PC card.
D4 V_{CC}_EN1	**V_{CC} Power Control.** The system sets this bit to '0' to turn off the socket's supply voltage, V_{CC}. The system sets this bit to '1' to turn on the socket supply voltage V_{CC}. If a card is not detected or the card is removed ($\overline{CD1}$, $\overline{CD2}$), the power control signals are not active, although VCC_EN1 is not set to '0'.
D3, D2, D1, D0 V_{PPx}_Cy	**V_{PPx} Power Control.** These four register bits are imaged at the PCMCIA power control pins V_{PPx}_ENy. The system can control the programming voltage by setting these bits. If both V_{PPx}_Cy signals are set, V_{PPx} is turned 'Off.'

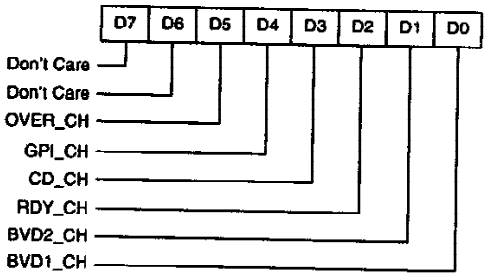
Interrupt and General Control Register
Index: 03 Hex



Bit(s)	Interrupt and General Control Description
D7 RI_EN	**Ring Indicate Enable.** Set this bit to '0' to permanently 3-state the output signal $\overline{\text{RI\_OUT}}$. Set this bit to '1' for the STSCHG signal of an I/O card to pass through to the $\overline{\text{RI\_OUT}}$ pin (3-state → low).
D6 C_RESET	**Card Reset.** Set this bit to '0' to activate the RESET signal; the PCMCIA socket is then reset continuously. This bit is '0' after a reset of the MSM60802. Set this bit to '1' to disable the PCMCIA socket reset.
D5 C_TYPE	**Card Type.** If the system sets this bit to '0', the MSM60802 only supports memory cards without any I/O functions. If the system sets this bit to '1', the MSM60802 supports I/O cards.
D4 INTR_EN	**Interrupt Request Enable.** If the system sets this bit to '1', a status change is indicated at the output signal $\overline{\text{INTR}}$ by switching the output from 3-state to 'low' for a minimum of three SYSCLK cycles.
D3, D2, D1, D0 IRQ_Cx	**Interrupt Requests.** These bits are used by the system to select the system interrupt signal, which reacts to a PCMCIA I/O interrupt request ($\overline{\text{REQ}}$). Depending on the state of LEV_EN (refer to the *"Global Control Register Index: 1E Hex"*) or CIPM (Clock Register), all IRQx signals drive active low interrupts or low to high edge-trigger interrupts. Refer to the IRQ_Cx Interrupt Configuration table below for details.

IRQ_C3	IRQ_C2	IRQ_C1	IRQ_C0	Interrupt Level
0	0	0	0	Inactive
0	0	1	1	IRQ3 enabled
0	1	0	0	IRQ4 enabled
0	1	0	1	IRQ5 enabled
0	1	1	1	IRQ7 enabled
1	0	0	1	IRQ9 enabled
1	0	1	0	IRQ10 enabled
1	0	1	1	IRQ11 enabled
1	1	0	0	IRQ12 enabled
1	1	1	0	IRQ14 enabled
1	1	1	1	IRQ15 enabled

Card Status Flag Register
Index: 04 Hex

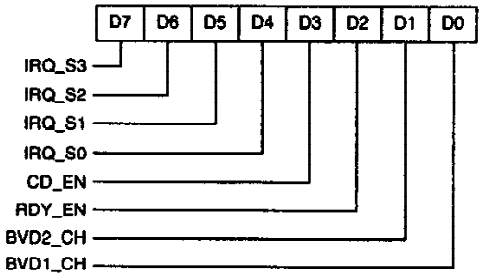


Note: If EX_WB in the Global Control Register is not set to '1', the contents are erased once the system has read the register. The only exception is that OVER_CH must be erased by explicit write back.

Bit(s)	Card Status Flag Description
D5 OVER_CH	**Overcurrent Input.** The state of the $\overline{\text{OVER\_C}}$ signal has been changed from '1' to '0'.
D4 GPI_CH	**General Purpose Input.** The state of the GPI signal has been changed. Refer to the *Card Detect and General Control Register* on page 28 for details.
D3 CD_CH	**Card Detect.** This bit will be set if both card-detect signals $\overline{\text{CD1}}$ and $\overline{\text{CD2}}$ are being asserted LOW or if one or both card-detect signals are being asserted HIGH.
D2 RDY_CH	**Ready/Busy.** The state of the RDY/BSY signal has been changed (rising edge). If the PCMCIA interface is configured for I/O operations, RDY_CH is permanently '0'.
D1, D0 BVDx_CH	**Battery Status.** Battery Status 1 (BVD1), Battery Status 2 (BVD2). The state of the BVD2 signal has been changed (falling edge). If the PCMCIA interface is configured for I/O operations, BVD2_CH is permanently '0'. The state of the BVD1 ($\overline{\text{STSCHG}}$) signal has been changed (falling edge).

Note: These bits are 'low' until they are enabled in the Card Status Interrupt Configuration Register.

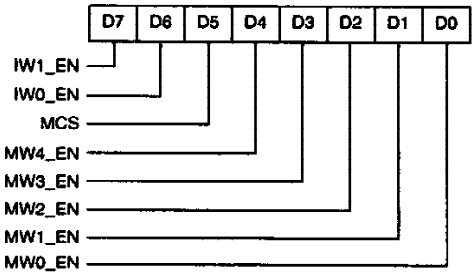
Card Status Interrupt Configuration Register
Index: 05 Hex



Bit(s)	Card Status Interrupt Configuration Description
D7, D6, D5, D4 IRQ_Sx	**Status Interrupt Signals.** By setting these bits, the system selects the interrupt signal, which should react on card status changes. Refer to the CD_EN, RDY_EN, BVDx_EN, OVER_CH, and GPI_CH signals, as well as the configuration table below. Depending on the state of LEV_EN (refer to the *"Global Control Register Index: 1E Hex"*), all IRQx signals drive active low interrupts or low to high edge-trigger interrupts. If INTR_EN in the Interrupt and General Control Register is set, a status change will always be indicated at the output pin $\overline{INTR}$. All other status interrupt signals are disabled.
D3 CD_EN	**Card Detect Enable.** If the level of a card-detect signal changes, the selected interrupt will be requested.
D2 RDY_EN	**Ready/Busy.** The state of the RDY/BSY signal has been changed (rising edge). If the PCMCIA interface is configured for I/O operations, RDY_CH is permanently '0'. If the level of the RDY/BSY signal changes, the selected interrupt (refer to *IRQ_Sx*) will be requested. If configured for I/O operations, no interrupt will be requested.
D1, D0 BVDx_CH	**Battery Status.** BVD1 and BVD2. If the level of the signal BVD2 change, the selected interrupt (refer to *IRQ_Sx*) is requested. If the MSM60802 is configured for I/O cards, an interrupt will not be generated. If the level of the signal BVD1 changes, the selected interrupt (refer to *IRQ_Sx*) will be requested. If the socket is configured for I/O card operations, a change of the STSCHG signal will request an interrupt (refer to *IRQ_Sx*).

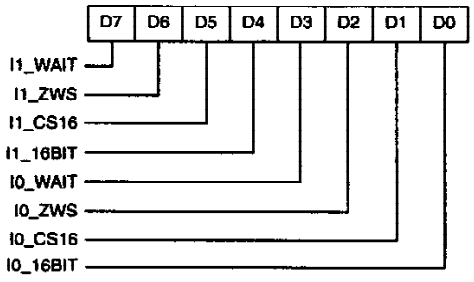
IRQ_S3	IRQ_S2	IRQ_S1	IRQ_S0	Interrupt Level
0	0	0	0	Inactive
0	0	1	1	IRQ3 enabled
0	1	0	0	IRQ4 enabled
0	1	0	1	IRQ5 enabled
0	1	1	1	IRQ7 enabled
1	0	0	1	IRQ9 enabled
1	0	1	0	IRQ10 enabled
1	0	1	1	IRQ11 enabled
1	1	0	0	IRQ12 enabled
1	1	1	0	IRQ14 enabled
1	1	1	1	IRQ15 enabled

Address Window Enable Register
Index: 06 Hex



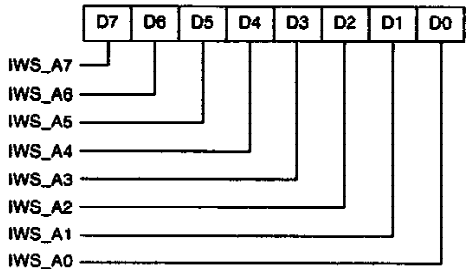
Bit(s)	Address Window Enable Description
D7 IW1_EN	**Enable I/O Window 1.** Set this bit to '1' for the system to enable I/O window 1 for I/O operations.
D6 IW0_EN	**Enable I/O Window 0.** Set this bit to '1' for the system to enable I/O window 0 for I/O operations.
D5 MCS	**Memory Chip Select.** Set this bit to '1' for to generate $\overline{\text{MEMCS16}}$ by decoding the system address signals LA[23:17] or SA[16:12]; otherwise, the signal is generated by decoding signals LA[23:17].
D4 MW4_EN	**Enable Memory Window 4.** Set this bit to '1' for the system to enable memory window 4 which accesses the PC card's common or attribute memory.
D3 MW3_EN	**Enable Memory Window 3.** Set this bit to '1' for the system to enable memory window 3 which accesses the PC card's common or attribute memory.
D2 MW2_EN	**Enable Memory Window 2.** Set this bit to '1' for the system to enable memory window 2 which access the PC card's common or attribute memory.
D1 MW1_EN	**Enable Memory Window 1.** Set this bit to '1' for the system to enable memory window 1 which accesses the PC card's common or attribute memory.
D0 MW0_EN	**Enable Memory Window 0.** Set this bit to '1' for the system to enable memory window 0 which accesses the PC card's common or attribute memory.

I/O Control Register
Index: 07 Hex



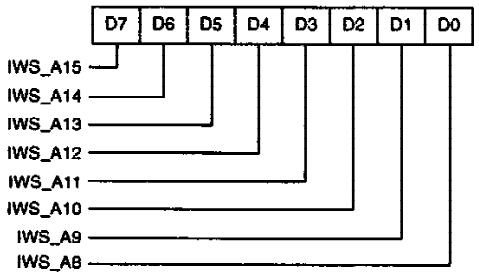
Bit(s)	I/O Control Description
D7, D3 Ix_WAIT	**Extend I/O Cycle.** If the system sets this bit to '1', the MSM60802 WAIT state generator inserts one extra WAIT state during 16-bit I/O cycles for I/O window x.
D6, D2 Ix_ZWS	**Zero WAIT State.** If the system sets this bit to '1', no extra WAIT state is inserted during 8-bit I/O cycles to I/O window x. Output signal $\overline{\text{OWS}}$ will be set active. If $\overline{\text{SBHE}}$ is '0' and SA0 is '0' during 8-bit I/O cycles, $\overline{\text{OWS}}$ is not active.
D5, D1 Ix_CS16	**Chip Select 16.** If the system sets this bit to '0', the output signal $\overline{\text{IOCS16}}$ images the state of the Ix_16BIT in this register. If the system sets this bit to '1', the output signal $\overline{\text{IOCS16}}$ is generated by the PC card signal $\overline{\text{IOIS16}}$.
D4, D0 Ix_16BIT	**16 Bit I/O.** If the system sets this bit to '0', the PC card is accessed as a 8-bit I/O card. If the system sets this bit to '1', the PC card is accessed as a 16-bit I/O card.

I/O Window x Start Address Low Byte
Index: 08 Hex (Window 0)
Index: 0C Hex (Window 1)



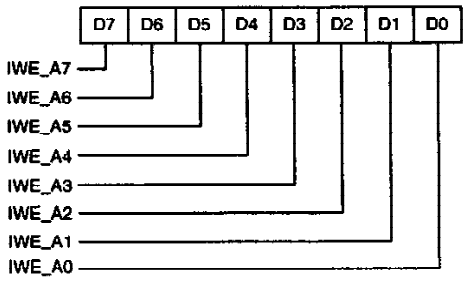
Bit(s)	I/O Control Description
D7 - D0 IWS_Ax	**I/O Window Low Byte Start.** IWS_Ax contains bits [7:0] of the I/O window start address.

I/O Window x Start Address High Byte
Index: 09 Hex (Window 0)
Index: 0D Hex (Window 1)



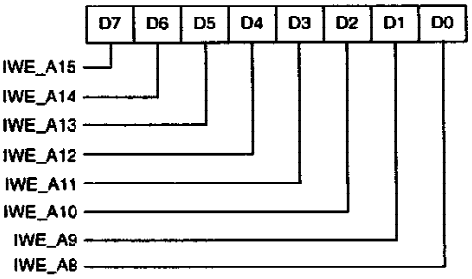
Bit(s)	I/O Control Description
D7 - D0 IWS_Ax	**I/O Window High Byte Start.** IWS_Ax contains bits [15:8] of the I/O window start address.

I/O Window x Stop Address Low Byte
Index: 0A Hex (Window 0)
Index: 0E Hex (Window 1)



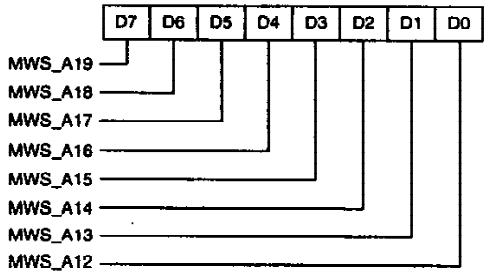
Bit(s)	I/O Control Description
D7 - D0 IWE_Ax	**I/O Window Low Byte End.** IWE_Ax contains bits [7:0] of the I/O window stop address.

I/O Window x Stop Address High Byte
Index: 0B Hex (Window 0)
Index: 0F Hex (Window 1)



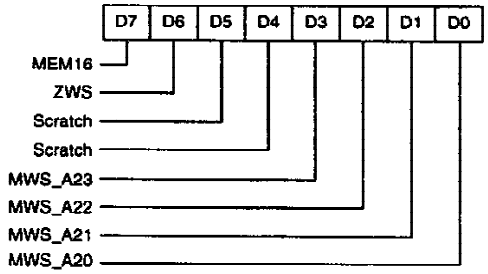
Bit(s)	I/O Control Description
D7 - D0 IWE_Ax	**I/O Window High Byte End.** IWE_Ax contains bits [15:8] of the I/O window stop address.

Memory Window x Start Address Low Byte
Index: 10 Hex (Window 1)
Index: 18 Hex (Window 2)
Index: 20 Hex (Window 3)
Index: 28 Hex (Window 4)
Index: 30 Hex (Window 5)



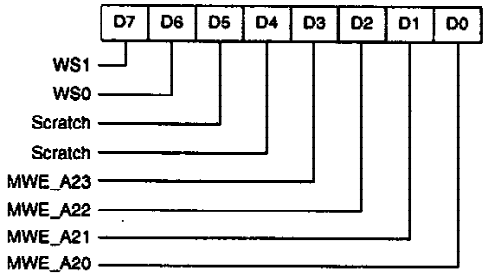
Bit(s)	I/O Control Description
D7 - D0 MWS_Ax	**Memory Window Start.** MWS_Ax contains bits [19:12] of the memory window start address.

Memory Window x Start Address High Byte
Index: 11 Hex (Window 1)
Index: 19 Hex (Window 2)
Index: 21 Hex (Window 3)
Index: 29 Hex (Window 4)
Index: 31 Hex (Window 5)



Bit	Description
D7 MEM16	**Memory Chip Select 16.** Set this bit to '0' for 8-bit memory access; $\overline{\text{MEMCS16}}$ will not be active. Set this bit to '1' for 16-bit memory access; $\overline{\text{MEMCS16}}$ will be active as in AWE_REG.
D6 ZWS	**Zero WAIT State.** Set this bit to '0' for the output signal $\overline{\text{OWS}}$ to not be inserted during memory cycles. Set this bit to '1' to activate $\overline{\text{OWS}}$. If the PC card does not activate the $\overline{\text{WAIT}}$ signal, no extra WAIT state will be inserted.
D5, D4 Scratch	**Scratch.** For personal use.
D3 - D0 MWS_Ax	**Memory Window Start.** Contains bits [23:20] of the memory window start address.

Memory Window x Stop Address High Byte
Index: 13 Hex (Window 1)
Index: 1B Hex (Window 2)
Index: 23 Hex (Window 3)
Index: 2B Hex (Window 4)
Index: 33 Hex (Window 5)



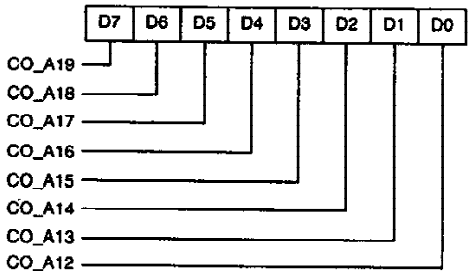
Bit	Description
D7, D6 WSx	**WAIT State** (WS1, WS0). The system can configure the number of inserted WAIT states during 16-bit memory cycles by setting WS1 and WS0. Refer to the WSx Configuration Table below for detail.

WS1	WS0	WAIT States
0	0	0
0	1	1
1	0	2
1	1	3

Note that if the PC card supports $\overline{\text{WAIT}}$, the PC card inserts WAIT states by itself. The internal WAIT state generator must then be disabled by setting WS1 and WS0 to '0'.

D5, D4 Scratch	**Scratch.** For personal use.
D3 - D0 MWE_Ax	**Memory Window End.** Contains bits [23:20] of the memory window stop address.

Card Memory Offset Address Low Byte
Index: 14 Hex (Window 1)
Index: 1C Hex (Window 2)
Index: 24 Hex (Window 3)
Index: 2C Hex (Window 4)
Index: 34 Hex (Window 5)

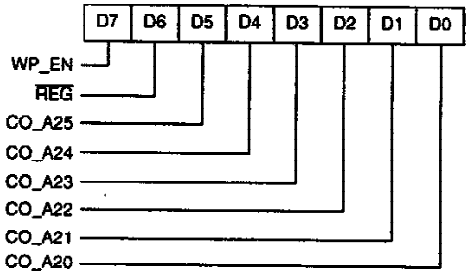


CO_Ax contains bits [19:12] of the offset that is added to the system address for memory operations

Bit(s)	I/O Control Description
D7 - D0 CO_Ax	**Card Offset.** CO_Ax contains bits [19:12] of the offset that is added to the system address for memory operations.

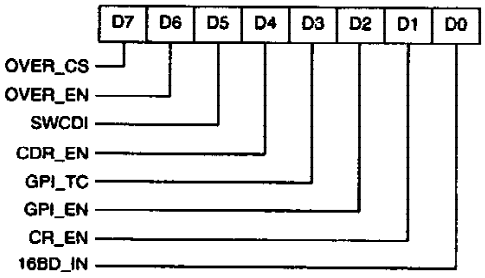
Card Memory Offset Address High Byte

Index: 15 Hex (Window 1)
Index: 1D Hex (Window 2)
Index: 25 Hex (Window 3)
Index: 2D Hex (Window 4)
Index: 35 Hex (Window 5)



Bit	Description
D7 WP_EN	**Write Protect Enable.** Set this bit to '1' to disable write cycles to the PC card.
D6 $\overline{REG}$	**Register Select.** Set this bit to '0' for the system to access the PC card common memory. Set this bit to '1' for the system to access the PC cards attribute memory.
D5 - D0 CO_Ax	**Card Offset.** CO_Ax contains bits [25:20] of the offset that are added to the system address for memory operations.

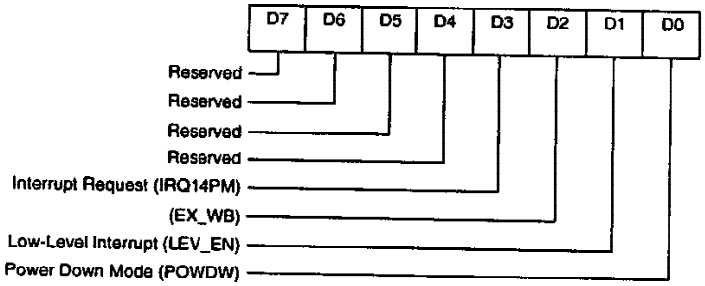
Card Detect and General Control Register
Index: 16 Hex



Bit(s)	Card Detect and General Control Register Description
D7 OVER_CS	**Overcurrent Input.** If this bit is set to '1' and OVER_EN is also set to '1', a transition at the input pin $\overline{\text{OVER\_C}}$ from '1' to '0' will shut down the power supply, via the power control signals. The power supply can be switched on again by resetting the interrupt flag (explicit write back).
D6 OVER_EN	**Overcurrent Enable.** If this bit is set to '1', an $\overline{\text{OVER\_C}}$ transition from '1' to '0' will force a card status change interrupt. The default of this bit is '0.'
D5 SWCDI	**Card Detect Status Change Interrupt.** Setting this bit to '1' causes a card detect status change interrupt. If bit CD_EN is set to '1' before, the SWCDI bit will always be read back as a '0.'
D4 CDR_EN	**Enable Card Detect.** If this bit is set to '1' and the MSM60802 sees a card detect change on the $\overline{\text{CD1}}$ and $\overline{\text{CD2}}$ inputs, then the MSM60802 clears the $\overline{\text{RI\_OUT}}$ output to '0'. The bit CD_CH in the Card Status Flag Register is also set to '1.' An interrupt is not performed. After setting this bit to '1', the MSM60802 asserts the $\overline{\text{RI\_OUT}}$ signal LOW until a read access or write access of '1' (explicit write back) to the bit CD_CH in the Card Status Flag Register has been performed.
D3 GPI_TC	**General Purpose Input Transition Control.** If this bit is set to '0' and bit D2 in this register, GPI_EN, is set to '1,' then a falling edge at the GPI signal input forces a card status change interrupt. If this bit is set to '1' and GPI_EN is set to '1', a rising edge at the input GPI forces a card status change interrupt. The default is '0.'
D2 GPI_EN	**General Purpose Input Enable.** If this bit is set to '0', a GPI transition does not force a card status change interrupt. The default is '0.'
D1 CR_EN	**Card Detect Enable.** If this bit is set to '1' and the $\overline{\text{CD1}}$ and $\overline{\text{CD2}}$ signals are rising, the MSM60802 generates a reset pulse that forces the configuration registers to their default states. SYSCLK does not need to be active to generate an internal reset pulse. Refer to the CR_EN table below, which contains the register defaults after reset. Note that all configuration registers are set to '00 hex' except for those listed in the table.
D0 16BD_IN	**16 Bit Data.** If this bit is set to '1' and the MEM16 bit of the Memory Window x Start Address High Byte Register is also set to '1', then SYSCLK does not synchronously delay the card control signals $\overline{\text{WE}}$ and $\overline{\text{OE}}$. If this bit is set to '0' and MEM16 is set to '1', the control signals $\overline{\text{OE}}$ and $\overline{\text{WE}}$ will be generated from the first falling edge of SYSCLK after the falling edge of $\overline{\text{MEMW}}$ or $\overline{\text{MEMR}}$. The MSM60802 asserts the control signals HIGH corresponding to the rising edge of $\overline{\text{MEMW}}$ or $\overline{\text{MEMR}}$. The default state is '0'.

Index	Register Name	Status
00h + Offset	Revision Number	No reset
01h + Offset	Card Status	Not reset
02h + Offset	Card Bus and Power Control	Not reset except bits VPPxCy
03h + Offset	Interrupt and General Control	Reset except bit INTR_EN
06h + Offset	Address Write Enable	Reset except bit $\overline{\text{MEMCS16}}$
16h + Offset	Card Detect and General Control	Not reset
1Eh + Offset	Global Control Register	Not reset
3Eh + Offset	Clock Register	Not reset
3Fh + Offset	Extension Register	Not reset

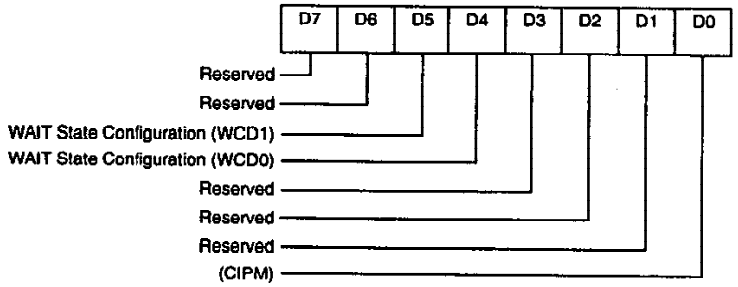
Global Control Register
Index: 1E Hex



Global Control Register Description

Bit	Description
D3 IRQ14PM	**Interrupt Request.** If this bit is set to '1' and the bit LEV_EN is set to '0', then the MSM60802 supports a pulsed PC card interrupt request on the IRQ14 output. All other IRQ outputs still support edge-trigger interrupts. If this bit is set to '1' and the bit LEV_EN is set to '1', then all IRQ's will perform level interrupts and can support pulsed PC card interrupt requests. In this case, the IRQ14PM doesn't care. If this bit is set to '0', then IRQ14 performs the same interrupt mode as all the other interrupt lines. Refer to *"PCMCIA Interrupt Request Handling"* for details.
D2 EX_WB	**Extension Register Write Back.** If this bit is set to '1', an active flag in the Card Status Flag Register is reset by writing a '1' into the active bit. If it is set to '0', reading the Card Status Flag Register will set the flag non-active, except OVER_CH that always must be written back.
D1 LEV_EN	**Low Level Interrupt.** If this bit is set to '1', all IRQx outputs perform low-level interrupts. If the interrupt is not active, the interrupt output is in 3-state condition. If this bit is set to '0', the IRQx outputs requests a host interrupt by switching from '0' to '1'. If the interrupt lines are not enabled, the outputs are in a 3-state condition. After the outputs are enabled, they drive '0'. The interrupts are active while the card interrupt request signal is active, or a card status change interrupt is served. The default state of the bit is '0'.
D0 POWDW	**Power Down Mode.** If this bit is set to '1', the internal clock and the memory and I/O windows are disabled. Refer to *"Power-Down Mode"* for details.

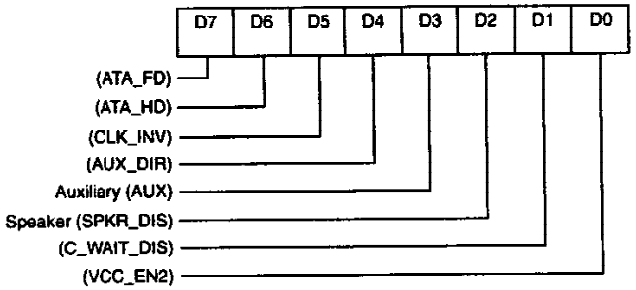
Clock Register
Index: 3E Hex



Clock Register Description

Bit	Description
D5, D4 WCDx	**WAIT State Configuration.** Configuration for WAIT state period: WCD1 = 0; WCD0 = 0: WAIT state timing is generated form SYSCLK; WCD1 = 0; WCD0 = 1: WAIT state timing is generated form SYSCLK / 2; WCD1 = 1; WCD0 = 0; WAIT state timing is generated form SYSCLK / 4; WCD1 = 1; WCD0 = 1; WAIT state timing is generated form SYSCLK / 8;
D3, D2, D1	Reserved
D0 CIPM	If this bit is set, all IRQ's of MSM60802 are able to transfer a pulse-mode PCMCIA interrupt to the ISA bus without inverter.

Extension Register
Index: 3F Hex



Bit	Extension Register Description
D7 ATA_FD	**ATA Floppy Disk.** If this bit is set to '1', during read cycles to the addresses 3F7h and 377h the MSM60802 only drives the data bus signal SD7. The MSM60802 signals SD[6:0] switch into a 3-state condition (for ATA floppy disk drives) during the cycle.
D6 ATA_HD	**ATA Hard Disk.** If this bit is set to '1', then the MSM60802 only drive the data bus signals SD[6:0] during read cycles to the addresses 3F7h and 377h. SD7 is switched into a 3-state condition (for ATA hard disk drives).
D5 CLK_INV	**Clock Invert.** If this bit is set to '0', 16-bit memory cycles are synchronized to the next falling edge of SYSCLK. If the bit is set to '1', 16-bit memory cycles are synchronized to the rising edge of SYSCLK.
D4 AUX_DIR	**Auxiliary Direction.** If this bit is set to '0', AUX is configured as an input. If this bit is set to '1' then the pin is configured as an output.
D3 AUX	**Auxiliary.** If this bit is read, it indicates the state of the AUX pin. If written and configured as an output, this bit sets the state of the AUX pin.
D2 SPKR_DIS	**Speaker Disable.** If the PCMCIA interface is configured for I/O operations, a '1' written to this bit disables the SPKR output of the MSM60802.
D1 C_WAIT_ DIS	**Wait Disable.** If this bit is set to '1', the PCMCIA Interface $\overline{\text{WAIT}}$ signal is ignored.
D0 VCC_EN2	This bit controls the state of V_{CC}_EN2 (see the V_{CC}_EN1 bit in the Card Bus and Power Control Register at index 02H).

PCMCIA Interrupt Request Handling

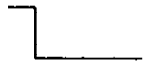
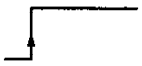
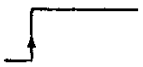
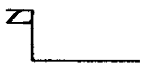
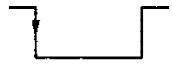
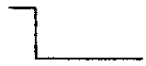
PCMCIA Interrupt Request	ISA Pulsed Mode Interrupt	EISA Pulsed Mode Interrupt	EISA Level Mode Interrupt
Pulsed Mode 	LEV_EN = 1 or CIPM = 1 	LEV_EN = 1 or CIPM = 1 	N/A
Level Mode 	LEV_EN = 0 and CIPM = 0 	LEV_EN = 0 and CIPM = 0 	LEV_EN = 1 or CIPM = 1 

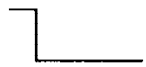
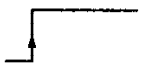
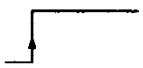
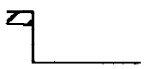
Figure 2. PCMCIA Interrupt Request at IRQ[15, 12, 9, 7, 5, 3] and IRQ14 (IRQ14PM = 0)

PCMCIA Interrupt Request	ISA Pulsed Mode Interrupt	EISA Pulsed Mode Interrupt	EISA Level Mode Interrupt
Pulsed Mode 	LEV_EN = "x" or CIPM = "x" 	LEV_EN = "x" or CIPM = "x" 	N/A
Level Mode 	N/A	N/A	LEV_EN = "x" or CIPM = "x" 

Note: "x" = Don't Care.

Figure 3. PCMCIA Interrupt Request at IRQ14 (IRQ14PM = 1)

Status Interrupt Request Handling

PCMCIA Interrupt Request	ISA Pulsed Mode Interrupt	EISA Pulsed Mode Interrupt	EISA Level Mode Interrupt
Level Mode 	LEV_EN = 0 and CIPM = "x" 	LEV_EN = 0 and CIPM = "x" 	LEV_EN = 1 or CIPM = "x" 

Note: "x" = Don't Care.

Figure 4. Status Interrupt at IRQ[15, 12, 9, 7, 5, 3] and IRQ14 (IRQ14PM = don't care)

Defaults after Reset

After resetting the MSM60802 by the signal RESET, all registers are set to 00 Hex, except the Revision Number Register that is not resettable.

Memory Cycle Synchronization

16 BD_IN	CLK_INV	OE or WE at 16-bit Cycles are Synchronized To
0	0	The next falling edge of SYSCLK
0	1	The next falling edge of SYSCLK
1	0	The falling edge of $\overline{\text{MEMWR}}$ or $\overline{\text{MEMRD}}$
1	1	The falling edge of $\overline{\text{MEMWR}}$ or $\overline{\text{MEMRD}}$

Power-Down Mode

Setting the PWRDN bit (in the Global Control Register) to '1' switches the MSM60802 into a power down mode:

- All I/O and memory windows are disabled but not reset.
- All address and data signals to the PCMCIA socket hold their last driven state before initialization of power-down mode.
- All adders and comparators are disabled.
- All registers are available for read and write cycles.
- $\overline{\text{INTR}}$ performs a falling edge, but not a pulse, when indicated by status interrupts.
- The WAIT state generator and PCMCIA control signals are disabled.

TIMING CHARACTERISTICS

Parameter	Symbol	Rated Value Min	Rated Value Max
SYSCLK cycle period		50	
LA[23:17] setup to BALE falling	T1	45	
SA[16:0] $\overline{SHBE}$ setup to BALE falling	T2	20	
BALE pulse width	T3	50	
LA[23:17] hold from BALE falling	T4	15	
CA[25:0] valid from SA[16:0], memory cycle	T5		56
$\overline{MEMCS16}$ valid from LA[23:17]	T6		40
$\overline{MEMCS16}$ valid from SA[16:0]	T7		32
$\overline{MEMCS16}$ hold from LA[23:17]	T8	0	
SA[16:0] setup to 16-bit memory command SA[16:0] setup to other commands	T9	25 80	
SA[16:0] hold from memory command	T10	25	
CA[25:0] from SA[16:0]	T11	0	
IOCHRDY low from command	T12		30
IRDY active from falling edge of SYSCLK	T13		30
IOCHRDY valid from $\overline{WAIT}$	T14		20
$\overline{OWS}$ active from command	T15		30
$\overline{OWS}$ inactive from command	T16		30
$\overline{OE}$, $\overline{WE}$ active from command, active for 8-bit and 16-bit memory cycles if the bit 16BD_IN in the Card Detect and General Control Register is set. Otherwise, $\overline{OE}$ AND $\overline{WE}$ for 16-bit memory cycles are synchronized with SYSCLK	T17		25
$\overline{OE}$, $\overline{WE}$ inactive from command inactive	T18		25
CE, $\overline{REG}$ valid from SA[16:0]	T19		40
CE, $\overline{REG}$ hold from SA[16:0]	T20	0	
SD[15:0] active from read command active	T21	0	
SD[15:0] hold from read command inactive	T22	0	
SD[15:0] delay from SD[15:0]	T23		30
CD[15:0] 3-state from read command active	T24		25
CD[15:0] delay from SD[15:0]	T25		30
CD[15:0] hold from write command inactive	T26	35	
SD[15:0] hold from write command inactive	T27	20	
CD[15:0] driving from read command inactive	T28	150	
AEN setup to command active	T38	45	
AEN hold from command inactive	T39	25	
SA[16:0] setup to I/O command	T40	80	
SA[16:0] hold from I/O command	T41	25	
CA[25:0] valid from SA[16:0] I/O cycle	T42	25	
$\overline{IORD}$, $\overline{IOWR}$ active from command active	T43		25
$\overline{IORD}$, $\overline{IOWR}$ inactive from command inactive	T44		25

TIMING CHARACTERISTICS (Continued)

Parameter	Symbol	Rated Value		Unit
		Min	Max	
$\overline{IOCS16}$ valid from SA[16:0]	T45		35	
$\overline{IOCS16}$ hold from SA[16:0]	T46	0		
$\overline{IOCS16}$ delay from $\overline{IOIS16}$	T47		20	
SD[7:0] valid from read command to internal register of the MSM60802	T50		80	
SD[7:0] hold from read command inactive	T51	0		
SD[7:0] setup to write command to internal register of the MSM60802	T52	50		
SD[7:0] hold from write command inactive to internal register of the MSM60802	T53	20		
$\overline{CS0}$ active to internal register access	T54	30		
$\overline{CS0}$ hold from internal register access	T55	0		
$\overline{RI\_OUT}$ delay from $\overline{STSCHG}$	T60		30	
Card power supply switched off after $\overline{OVER\_C}$, when OVER_EN and OVER_CS are set	T61		50	
$\overline{IRQx}$ delay from $\overline{REQ}$	T62		30	
$\overline{INTR}$ delay from card status change	T63		50	
$\overline{INTR}$ pulse width	T64	3*SYSCLK		
$\overline{IRQx}$ delay from card status change	T65			50
$\overline{SPKR\_OUT}$ delay from $\overline{SPKR}$	T66			30

TIMING WAVEFORMS

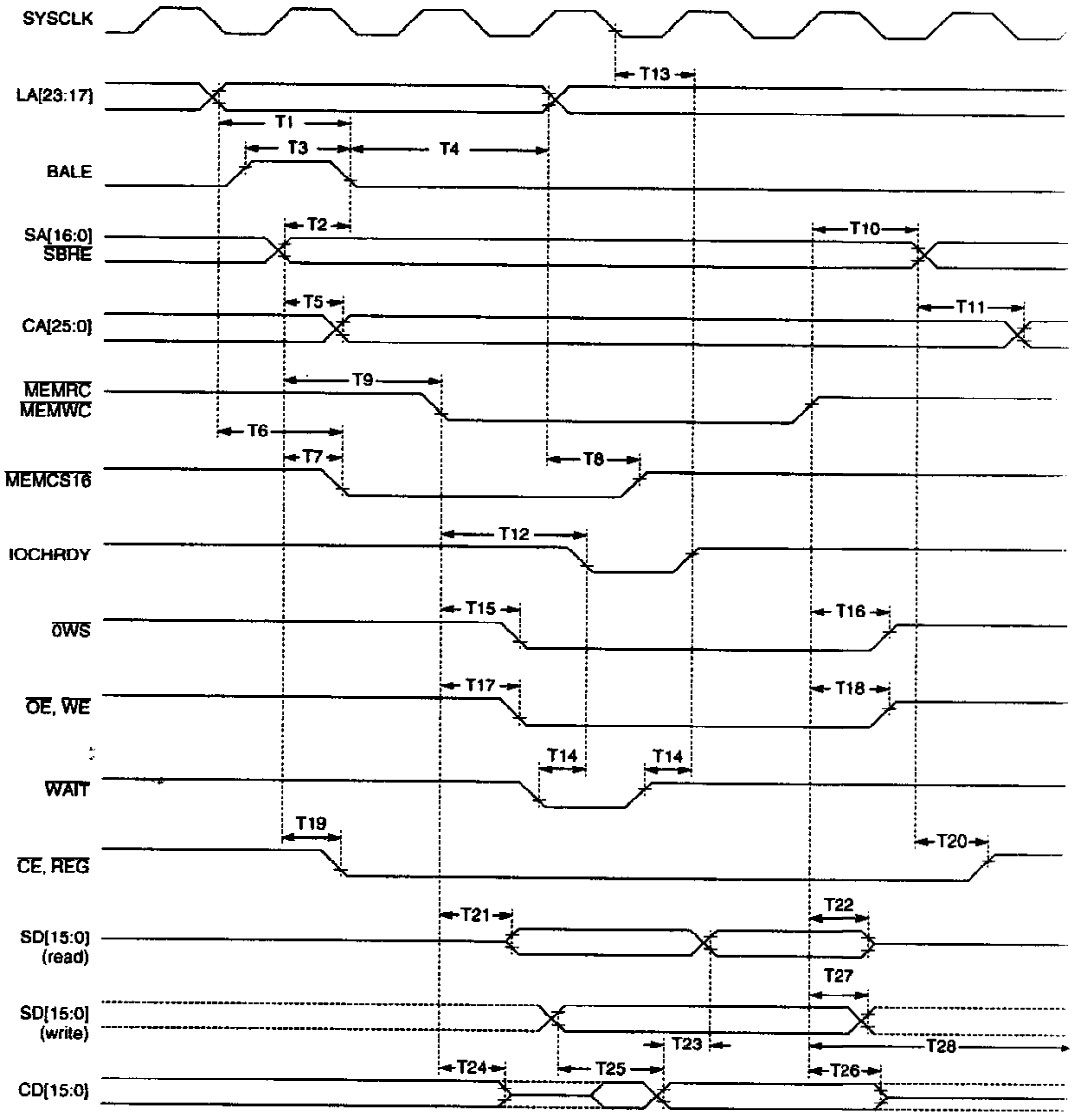
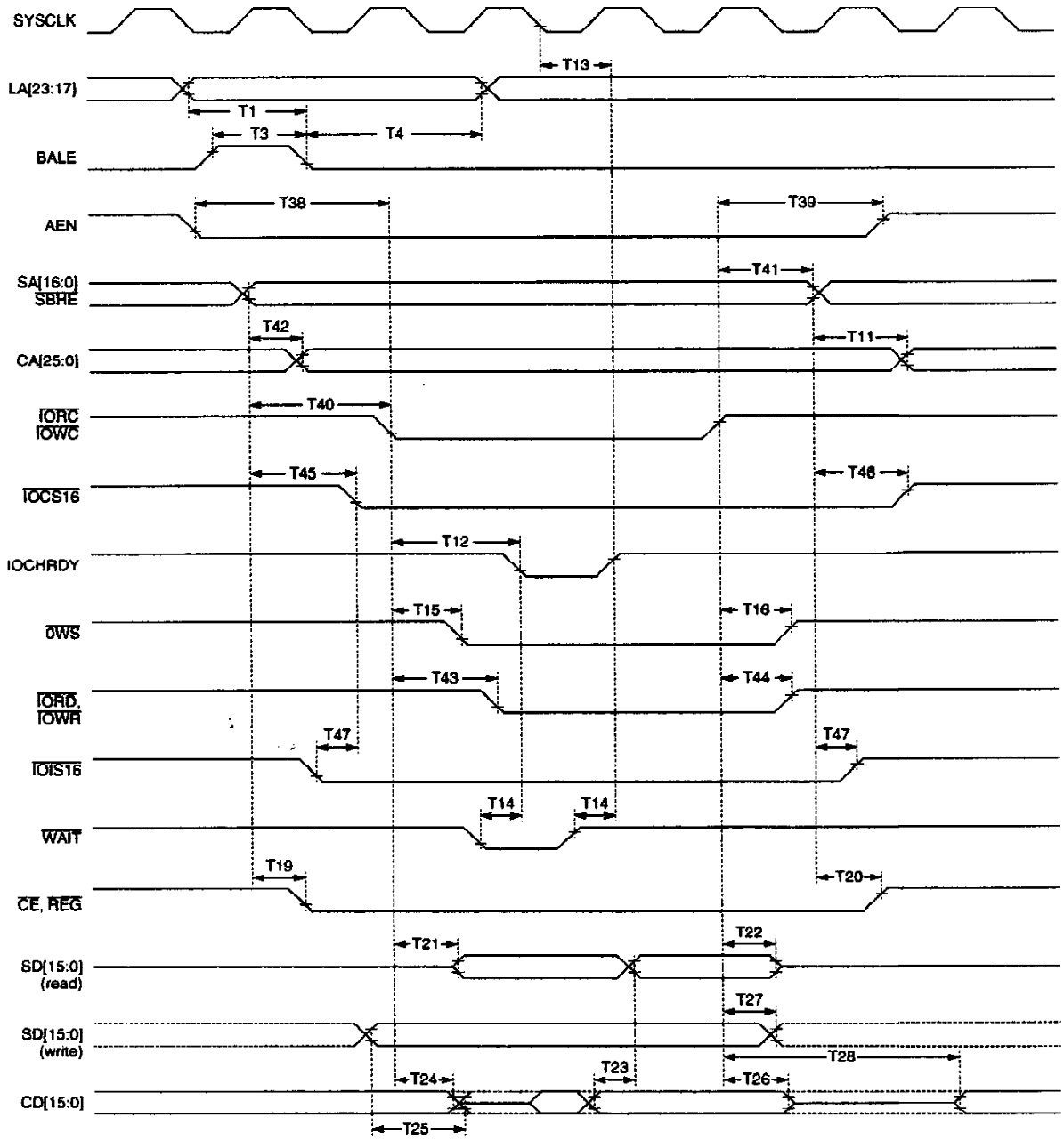


Figure 5. 8/16 Bit I/O Cycles


SYSCLK
LA[23:17]
BALE
AEN
SA[16:0]
SBHE
CA[25:0]
IORC
IOWC
IOCS16
IOCHRDY
0WS
IORD,
IOWR
IOIS16
WAIT
CE, REG
SD[15:0]
(read)
SD[15:0]
(write)
CD[15:0]
T1
T3
T4
T11
T12
T13
T14
T15
T16
T19
T20
T21
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T47

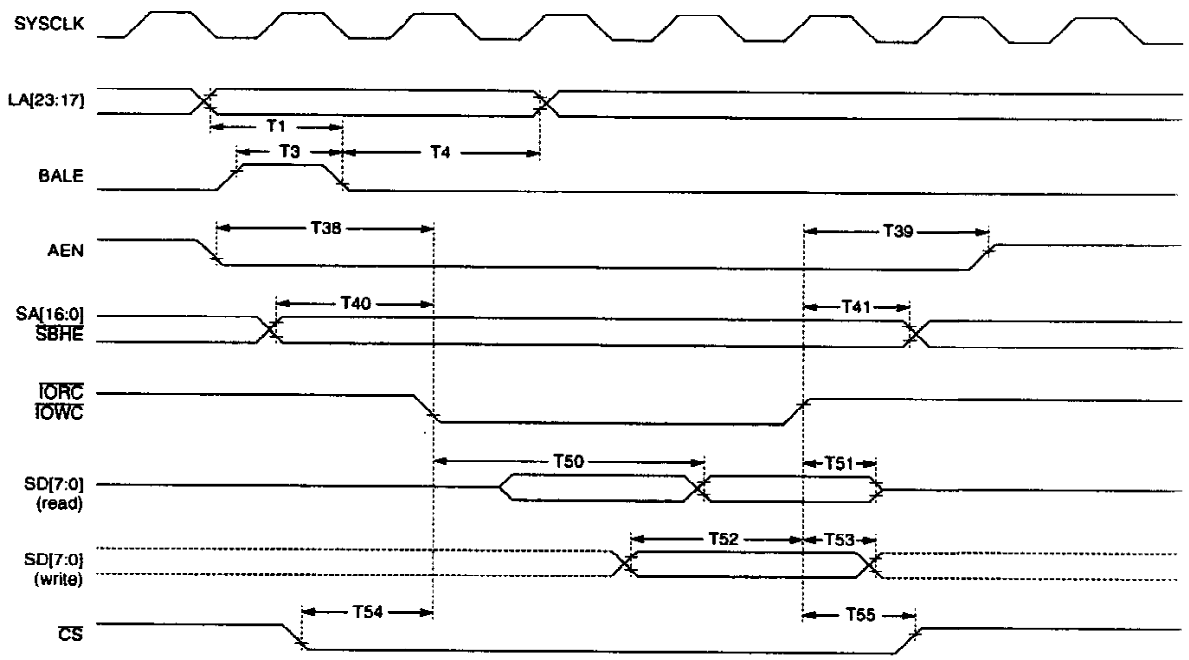

Figure 6. 8-Bit Access to MSM60802 Internal Registers

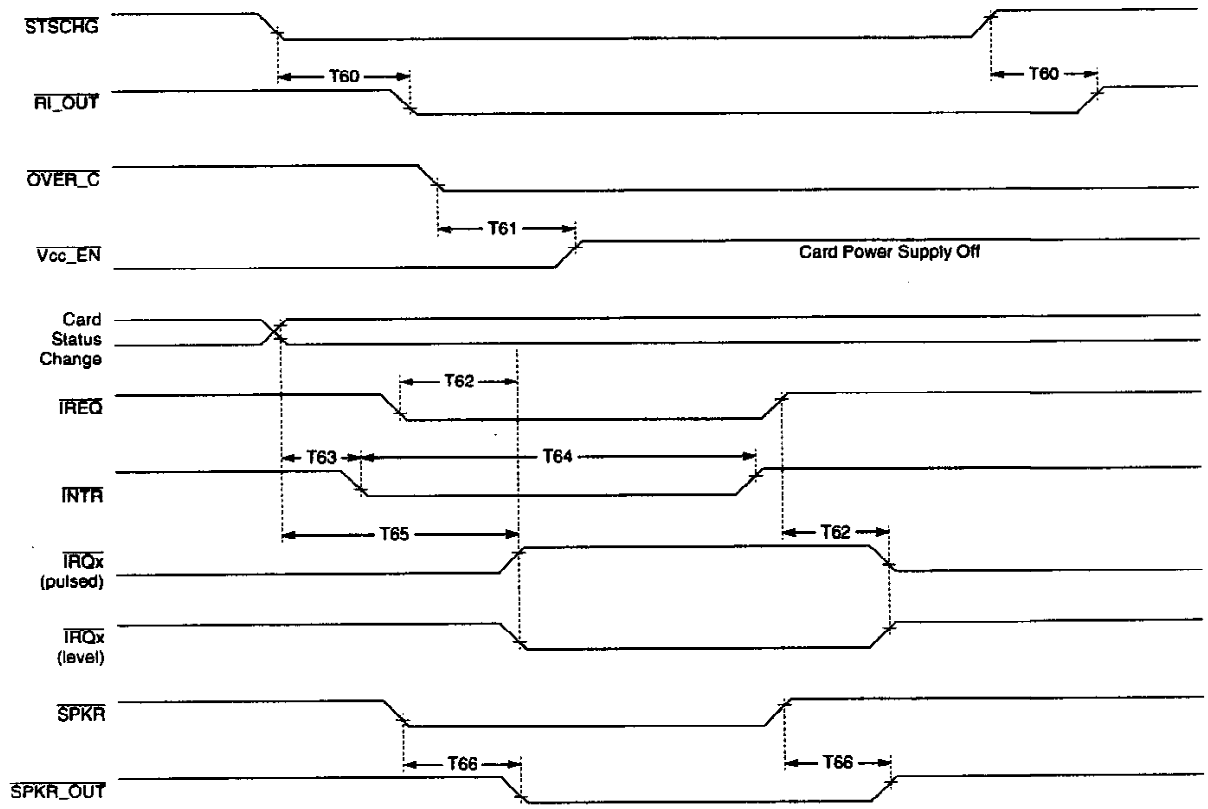

Figure 7. SPKR, STCHG, OVER_C and Interrupt Timing