OKI Semiconductor
This version: Jan. 1998
Previous version: Nov. 1996

MSM7524

DTMF Transceiver

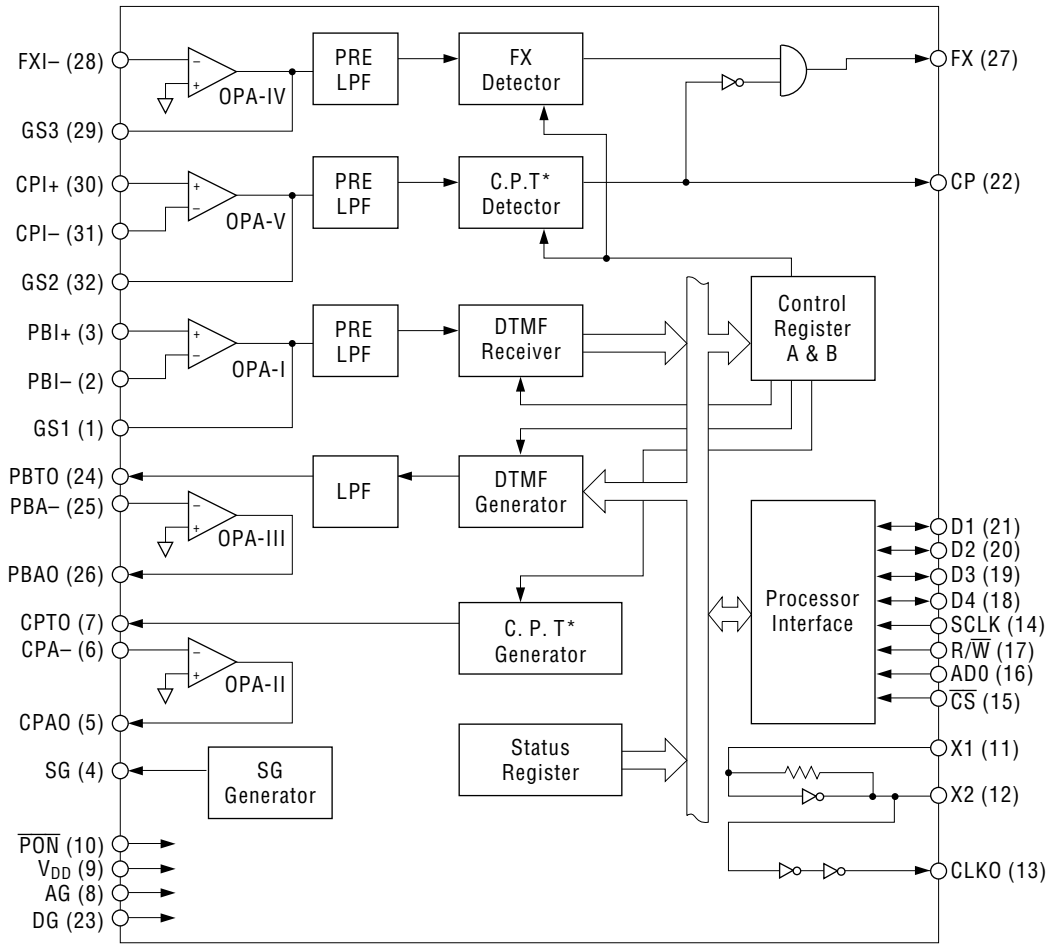
GENERAL DESCRIPTION

The MSM7524 is the single chip DTMF transceiver –generator/receiver– with the call progress tone generator/detector and the special tone –1300 Hz in the first version, possible to be modified– detector.
Each function block can be controlled by an external MCU via 4-bit processor interface.
The chip operates with +5 V single supply with low power consumption, and is suitable for the telephone terminal equipment.

FEATURES

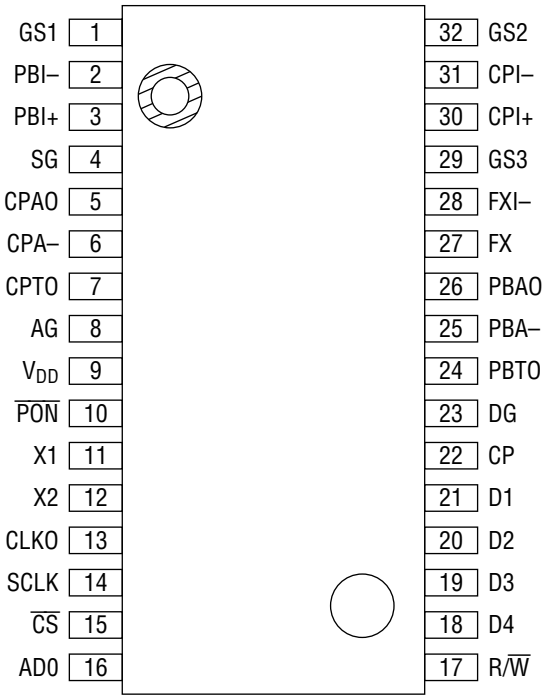
- Power supply voltage : +5 V ±10%
- Low power consumption
  Operating mode : 8 mA Typ.
  Power down mode : 10 µA Typ.
- 4-bit processor interface
- Dynamic range of DTMF receiver : 40 dB
- Low signal distortion output from DTMF generator
- Call progress tone detector : 330 to 640 Hz
- Call progress tone generator : 350/400/440/480 Hz
- Special tone detector: 1300 Hz ±20 Hz (for FAX)
- 3.58 MHz crystal oscillator circuit on chip
- Package :
  32-pin plastic SSOP (SSOP32-P-430-1.00–K) (Product name : MSM7524GS-K)

BLOCK DIAGRAM



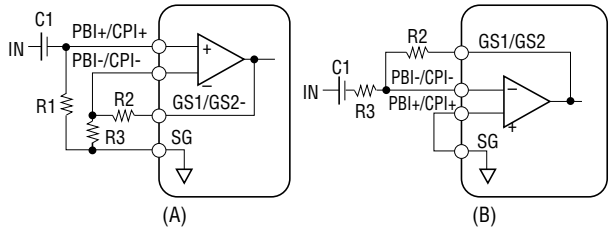
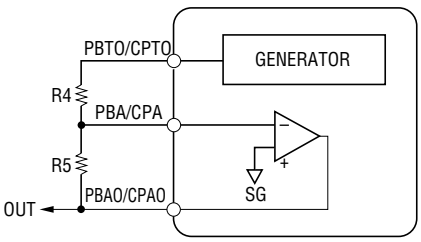
*C. P. T : Call Progress Tone

PIN CONFIGURATION (TOP VIEW)



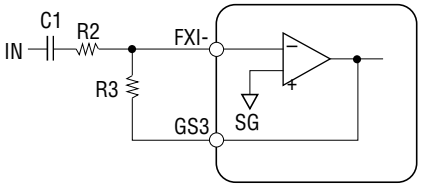
32-Pin Plastic SSOP

PIN DESCRIPTION

Pin No.	Name	I/O	Description
1	GS1	O	Output and two input pins of the on-chip operational amplifier (1). These pins are used to implement the pre-amplifier for DTMF tone receiving. Refer to Fig. 1.
2	PBI–	I	
3	PBI+	I	
			 • R1, R2, R3 ≥ 50 kΩ, C1 = 2.2 µF • Voltage Gain; 1 + R2/R3.....(A) R2/R3.....(B) **Figure 1 Receive Gain Adjustment** Voltage gain should be less than 10(20 dB). DTMF receiver's detect and non-detect amplitude are specified as the receive signal level at GS1.
4	SG	O	On-chip signal ground. The potential is approximately half of V_{DD}.
5	CPAO	O	Output and inverting input pins of the on-chip operational amplifier (II). The non-inverting input is internally connected to SG. When not using this amplifier, these pins should be wired to each other.
6	CPA–	I	
7	CPTO	O	Call progress tone (CPT) output. Tone amplitude is approximately 0 dBm on CPTO, but the transmit signal level can be adjusted by using the on-chip operational amplifier (II). Refer to Fig. 2. Make/Break of CPT transmitting is controlled through the processor interface.  • R4, R5, ≥ 20 kΩ • Voltage Gain; R5/R4 ≤ 10(20 dB) **Figure 2 Transmit Gain Adjustment**

Pin No.	Name	I/O	Description
8	AG	—	Analog ground, 0 V. This pin should be common with DG (pin 23) at the system ground point.
9	V_{DD}	—	Power supply, +5 V.
10	$\overline{PON}$	I	Power down control. When digital "1" is applied to $\overline{PON}$, the whole circuitry on chip falls into the power down mode. This pin is pulled-up to digit "1" internaly.
11	X1	I	X1 and X2 are connected to a 3.579545 MHz crystal to generate a crystal clock for the chip. If required to use an external clock, X1 should be left open and X2 should be connected to the external clock source via a capacitor of 100 pF.
12	X2	O	
13	CLKO	O	3.579545 MHz clock output.
14	SCLK	I	External processor interface clock input. During "WRITE" mode, the data on D4 to D1 pins are written into the internal register at the falling edge of SCLK. During "READ" mode, the output data from the internal register appears on D4 to D1 pins at the rising edge of SCLK. SCLK is not required to be a periodic clock pulse stream. SCLK is internally pulled-down to digital "0".
15	$\overline{CS}$	I	Chip select. When $\overline{CS}$ is on digital "0", "READ" and "WRITE" operations become possible. $\overline{CS}$ is internally pulled-down.
16	AD0	I	Address data input. When digital "1" is applied to AD0, data writing into the control register and data reading out from the status register become possible. When digital "0" is applied to, data writing into the DTMF tone transmit register and data reading out from the DTMF tone receive register become possible. AD0 is internally pulled-down.
17	R/$\overline{W}$	I	"READ" and "WRITE" control signal input. "READ" or "WRITE" operation becomes possible during digital "1" or "0", respectively. R/$\overline{W}$ is internally pulled-down to digital "0".
18	D4	I/O	4-bit micro-processor interface bus. All pins are internally pulled-down.
19	D3	I/O	
20	D2	I/O	
21	D1	I/O	

Pin No.	Name	I/O	Description
22	CP	O	Call progress tone detect. When the tone is detected, CP shows digital "1" state. Detected call progress tone frequency and amplitude range are specified as follows. Frequency; 330 to 640 Hz Amplitude; 0 to –40 dBm (at GS2)
23	DG	—	Digital ground, 0 V. This pin should be common with AG (pin 8) at the system ground point.
24	PBTO	O	DTMF tone output. The signal amplitude of the low-group and the high-group tones are –6.5 dBm and –5.5 dBm at PBTO, respectively, but, the transmit signal amplitude can be adjusted by applying the on-chip operational amplifier (III). Refer to Fig. 2. Make/Break of DTMF tone transmitting is controlled through the processor interface.
25	PBA–	I	Inverting input and output pins of the on-chip operational amplifier (III). The non-inverting input is internally connected to SG. When not using this amplifier, these pins should be wired to each other.
26	PBAO	O	
27	FX	O	Special tone detect. The MSM7524 first version provides this function for 1300 Hz tone which is well-known for FAX auto-receipt. When the tone is detected, FX shows digital "1" state. Detected tone frequency and amplitude range are specified as follows. Frequency: 1280 to 1320 Hz Amplitude: 0 to –34 dBm (at GS3) When CP is on digital "1" (call progress tone is detected), FX is forced to be on digital "0" state regardless of the special tone existence.

Pin No.	Name	I/O	Description
28	FXI–	I	Special tone input and gain adjustment. FXI- and GS3 are connected to the inverting input and the output of the on-chip operational amplifiers (IV). The inverting input of the amplifier (IV) is internally connected to SG. When not using the special tone detect function, FXI- and GS3 should be wired to each other. Regarding the gain adjustment, refer to Fig. 3.
29	GS3	O	 • R2, R3, ≥ 50 kΩ, C1 = 2.2 µF • Voltage Gain; R3/R2 ≤ 10 (20 dB) **Figure 3 Receive Gain Adjustment for FX**
30	CPI+	I	Two input and output pins of the on-chip operational amplifier (V). These pins are useful to implement the pre-amplifier for Call Progress Tone receiving. Refer to Fig. 1. Voltage gain should be less than 10 (20 dB). Detect and non-detect amplitude are specified as the receive signal level at GS2.
31	CPI–	I	
32	GS2	O	

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	Ta = 25°C With respect to AG or DG	–0.3 to +7	V
Input Voltage	V_{IN}		0.3 to V_{DD} + 0.3	V
Storage Temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage		V_{DD}	—	+4.5	+5.0	+5.5	V
Operating Temperature		T_{op}	—	–25	—	+85	°C
Input Clock Frequency		f_{CLK}	External Clock	–0.1	—	+0.1	%
Bypass Capacitor	V_{DD}	C_{VA}	Between V_{DD} and AG	0.1 + 10	—	—	µF
	SG	C_{SA}	Between SG and AG	1	—	—	µF
Digital Input Rise Time		t_{lr}	$\overline{CS}$, AD0, R/$\overline{W}$, D4 to D1, $\overline{PON}$, SCLK	—	—	50	ns
Digital Input Fall Time		t_{lf}		—	—	50	ns
Crystal	Frequency Deviation	—	+25°C ±5°C	–100	—	+100	ppm
	Temperature Characteristics	—	At –25°C to 85°C	–50	—	+50	ppm
	Equivalent Series Resistance	—	—	—	—	50	Ω
	Load Capacitance	—	—	—	16	—	pF

ELECTRICAL CHARACTERISTICS

DC and Digital Inerface Characteristics

(V_{DD} = +5 V ±10%, Ta = –25°C to 85°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Power Supply Voltage	I_{DD1}	Operating Mode		—	8.0	11.0	mA
	I_{DD2}	Power Down Mode		—	10	100	µA
Input Voltage	V_{IH}	—		2.2	—	V_{DD}	V
	V_{IL}			0.0	—	0.8	V
Input Leakage Current	I_{IH}	V_I = 5V	SCLK, $\overline{CS}$, AD0, R/$\overline{W}$, D1 to D4	–10	—	+80	µA
			$\overline{PON}$	–10	—	+10	
	I_{IL}	V_I = 0V	SCLK, $\overline{CS}$, AD0, R/$\overline{W}$, D1 to D4	–10	—	+10	µA
			$\overline{PON}$	–80	—	+10	
Output Voltage	V_{OH}	—	I_{OH} = –0.4 mA	2.4	—	V_{DD}	V
	V_{OL}		I_{OL} = 1.6 mA	0.0	0.2	0.4	V
Analog Output Offset Voltage	V_{OFF}	CPAO, PBAO		–100	—	+100	mV
Analog Input Resistance	R_{IN}	CPI+, CPI-, PBI+, PBI-, FXI-, PBA-, CPA-		—	10	—	MΩ
Analog Output Resistance	R_{OUT}	PBTO, PBAO, CPTO, CPAO, GS1, GS2, GS3		20	—	—	MΩ

ANALOG INTERFACE CHARACTERISTICS

DTMF Generator

(V_{DD} = +5 V ±10%, Ta = –25°C to 85°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
DTMF Tone Transmit Amplitude	V_{PBTL}	at PBTO	Low Group Tone	–8.5	–6.5	–4.5	dBm
	V_{PBTH}		High Group Tone	–7.5	–5.5	–3.5	dBm
Tone Transmit Amplitude Ratio	V_{PBDF}		V_{PBTH}-V_{PBTL}	0.0	1.0	2.0	dB
Tone Frequency Accuracy	f_{DPB}		To Nominal Rrequency	—	—	±1.5	%
Total Harmonic Distortion	THD_{PB}		Total Harmonics - Fundamental	—	—	–23	dB
Out-of-Band Spurious *	V_{SPS}		4 to 8 kHz	—	—	P-20	dB
			8 to 12 kHz	—	—	P-60	dB
			12 kHz to	—	—	P-60	dB

*P: Inband energy

Call Progress Tone (CPT) Generator

(V_{DD} = +5 V ±10%, Ta = –25°C to 85°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Tone Amplitude	V_{CPT}	at CPTO	—	–2.0	0	2.0	dBm
Tone Transmit Amplitude Ratio	f_{CPT0}		CPT2 = 0, CPT1 = 0	380	400	420	Hz
	f_{CPT1}		CPT2 = 0, CPT1 = 1	330	350	370	Hz
	f_{CPT2}		CPT2 = 1, CPT1 = 0	420	440	460	Hz
	f_{CPT3}		CPT2 = 1, CPT1 = 1	460	480	500	Hz
Tone Harmonic Distortion	THD_{CPT}	—	Total Harmonics – Fundamental	—	—	–23	dB

Call Progress Tone (CPT) Detector

(V_{DD} = +5 V ±10%, Ta = –25°C to 85°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Detect Amplitude	V_{DETCP}	f_{IN}: 330 to 640 Hz, at GS2		–40	—	0	dBm
Non-detect Amplitude	V_{REJCP}			—	—	–60	dBm
Hysteresis of Detect Amplitude	V_{HYSCP}	—		—	4.0	—	dB
Detect Frequency	f_{DETCP}	—		330	—	640	Hz
Time to Detect	t_{DETCP}	Refer to Fig. 4.	Detect	70	—	—	ms
Time to Reject	t_{REJCP}		Non-detect	—	—	35	ms
Detect Delay Time	t_{DELCP}			35	50	70	ms
Detect Hold Time	t_{HOLCP}			—	50	—	ms
Non-detect Frequency	f_{REJCP}	—		700	—	—	Hz
				—	—	270	

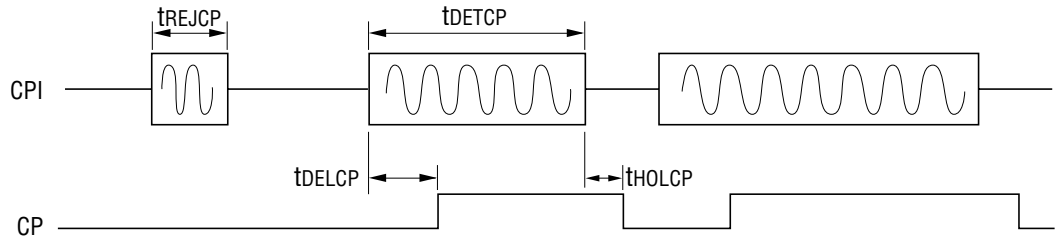


Figure 4 CPT Detect Timing

Special Tone (ex. F-tone for FAX auto-receipt) Detector

(V_{DD} = +5 V ±10%, Ta = –25°C to 85°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Detect Amplitude	V_{DETFX}	f_{IN} : 1,300 Hz ±20 Hz, at GS3		–34	—	0	dBm
Non-detect Amplitude	V_{REJFX}			—	—	–60	dBm
Hysteresis of Detect Amplitude	V_{HYSFX}	—		—	4.0	—	dB
Detect Frequency	f_{DETFX}	—		1,280	—	1,320	Hz
Time to Detect	t_{DETFX}	Refer to Fig. 5.	Detect	70	—	—	ms
Time to Reject	t_{REJFX}		Non-detect	—	—	35	ms
Detect Delay Time	t_{DELFX}			35	50	70	ms
Detect Hold Time	t_{HOLFX}			—	50	—	ms
Non-detect Frequency	f_{REJFX}	—		1360	—	—	Hz
				—	—	1240	

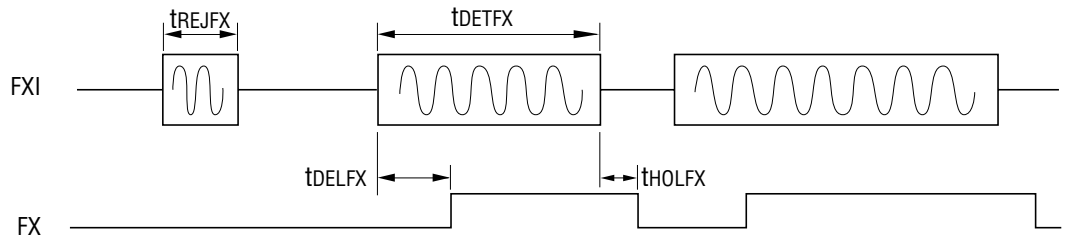


Figure 5 Special Tone Detect Timing

DTMF Receiver

(V_{DD} = +5 V ±10%, Ta = –25°C to 85°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Detect Amplitude	V_{DETDT}	f_{IN} : Nominal Frequency ±1.5%, at GS1		–40	—	0	dBm
Non-detect Amplitude	V_{REJDT}			—	—	–60	dBm
Detect Frequency	f_{DETDT}	To Nominal Frequency		—	—	±1.5	%
Non-detect Frequency	f_{REJDT}			±3.8	—	—	%
Level Twist	V_{TWIST}	$V_{High\ Group}$–$V_{Low\ Group}$		–6.0	—	+6.0	dB
Noise to Signal Ratio (N/S)	$V_{N/S}$	N : 0.3 to 3.4 kHz		—	–12	—	dB
Dial Tone Rejection Ratio	V_{REJ}	350 to 480 Hz		22	—	—	dB
Signal Repetition Time	t_{CYCDT}	Refer to Fig. 6.		120	—	—	ms
Time to Detect	t_{DETDT}		Detect	49	—	—	
Time to Reject	t_{REJFDT}		Non-detect	—	—	24	
Interdigit Pause	t_{PAUDT}			30	—	—	
Acceptable Drop Out	t_{BRKDT}			—	—	2	
Detect Delay Time	t_{DELDT}			24	41	49	
Detect Hold Time	t_{HOLDT}			21	28	35	

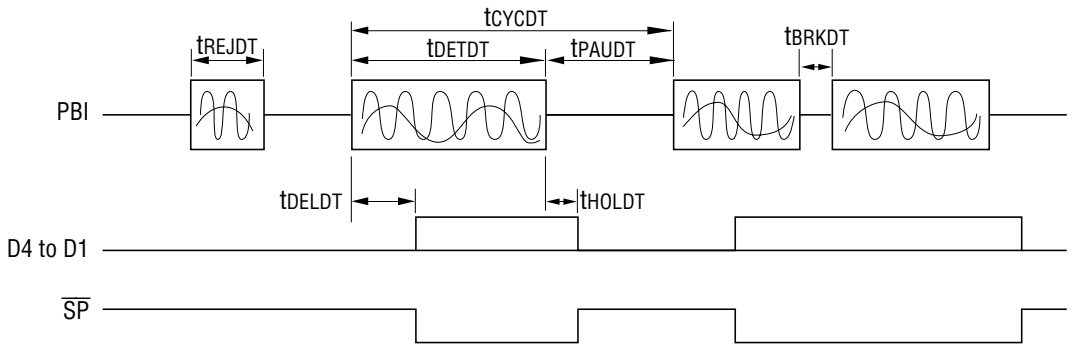


Figure 6 DTMF Receiver Timing

Processor Interface Characteristics

(V_{DD} = +5 V ±10%, Ta = –25°C to 85°C)

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit
SCLK Period		t_{CYC}	Refer to Fig. 7.	1	—	—	ns
SCLK Pulse Width		t_{HI}	Digital "1"	400	—	—	
		t_{LO}	Digital "0"	400	—	—	
AD0	Setup Time	t_{AS}	AD0 → SCLK	80	—	—	
	Hold Time	t_{AH}	SCLK → AD0	10	—	—	
$\overline{CS}$	Setup Time	t_{CS}	$\overline{CS}$ → SCLK	80	—	—	
	Hold Time	t_{CH}	SCLK → $\overline{CS}$	10	—	—	
R/$\overline{W}$	Setup Time	t_{RWS}	R/$\overline{W}$ → SCLK	80	—	—	
	Hold Time	t_{RWH}	SCLK → R/$\overline{W}$	10	—	—	
D4 to D1 (Write)	Setup Time	t_{DWS}	D4 to D1 → SCLK	80	—	—	
	Hold Time	t_{DWH}	SCLK → D4 to D1	10	—	—	
D4 to D1 (Read)	Delay Time	t_{DRD}	SCLK → D4 to D1	—	—	150	
	Hold Time	t_{DRH}	D4 to D1 → SCLK	10	—	—	

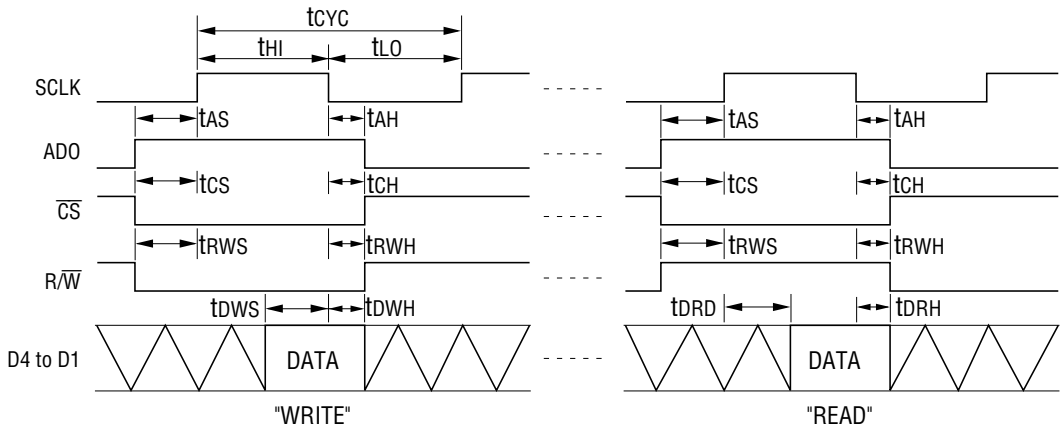


Figure 7 Processor Interface READ/WRITE Timing

PROCESSOR INTERFACE

Internal Register Address and Function

Table-1

AD0	R/$\overline{W}$	READ/WRITE	Registers
0	0	WRITE	DTMF Tone Transmit Data
0	1	READ	DTMF Tone Receive Data
1	0	WRITE	Control Data
1	1	READ	Status Data

DTMF Tone Transmit/Receive Data Registers

Table-2

D4	D3	D2	D1	Digit	Low-Group Tone (Hz)	High-Group Tone (Hz)
0	0	0	1	1	697	1209
0	0	1	0	2		1336
0	0	1	1	3		1477
0	1	0	0	4	770	1209
0	1	0	1	5		1336
0	1	1	0	6		1477
0	1	1	1	7	852	1209
1	0	0	0	8		1336
1	0	0	1	9		1477
1	0	1	0	0	941	1336
1	0	1	1	*		1209
1	1	0	0	#		1477
1	1	0	1	A	697	1633
1	1	1	0	B	770	
1	1	1	1	C	852	
0	0	0	0	D	941	

Control Data Register A

Table-3-1

D4	D3	D2	D1
RSEL	—	CPEN	MFC

Table-3-2

Bit	Name	Function
D4	RSEL	Control data register select. "0" : Register A is selected. "1" : Register B is selected on the next Write cycle to the Control Register address. Subsequent Write cycles to the Control Register are directed back to Control Register A.
D3	—	Not used. Set to digital "0" or "1".
D2	CPEN	Call Progress Tone (CP)/Special tone (FX) detect control. "0" : Disable CP and FX. Both CP and FX are held on digital "0". "1" : Enable CP and FX.
D1	MFC	DTMF Tone Transmit Make/Break control. "0" : Disable. PBTO outputs only DC potential at SG. "1" : Enable. DTMF tone is generated via PBTO.

Control Data Register B

Table-4-1

D4	D3	D2	D1
CPT2	CPT1	CPTC	—

Table-4-2

Bit	Name	Function
D4 D3	CPT2 CPT1	Call Progress tone frequency select. CPT2 / CPT1 / Frequency (Hz): 0 / 0 / 400 0 / 1 / 350 1 / 0 / 440 1 / 1 / 480
D2	CPTC	Call Progress tone Transmit/Make/Break control. "0" : Disable. CPTO outputs only DC potential at SG. "1" : Enable. Call Progress tone is generated via CPTO.
D1	MFC	Not used. Set to digital "0" or "1".

Note) All control data on Registers A and B should be cleared by software and/or $\overline{\text{PON}}$ control. Power-down control by $\overline{\text{PON}}$ makes all logic status and control data to be cleared.

Status Data Register

Table-5-1

D4	D3	D2	D1
$\overline{SP}$	SPFLG	CPFLG	AFLG

Table-5-2

Bit	Name	Function
D4	$\overline{SP}$	Signal Present for DTMF tone receive. "0" : Valid data is in the receive data register. "1" : Data is invalid.
D3	SPFLG	Flag for valid DTMF tone receive. SPFLG is reset to digital "0" after an external processor reads out the status register data.
D2	CPFLG	Flag for valid Call Progress tone detect. CPFLG is reset to digital "0" after an external processor reads out the status register data.
D1	AFLG	AFLG is set to digital "1" when SPFLG and/or CPFLG is set to digital "1". After an external processor reads out the status register data, AFLG is reset to digital "0".

PROCESSOR CONTROL

Table-6

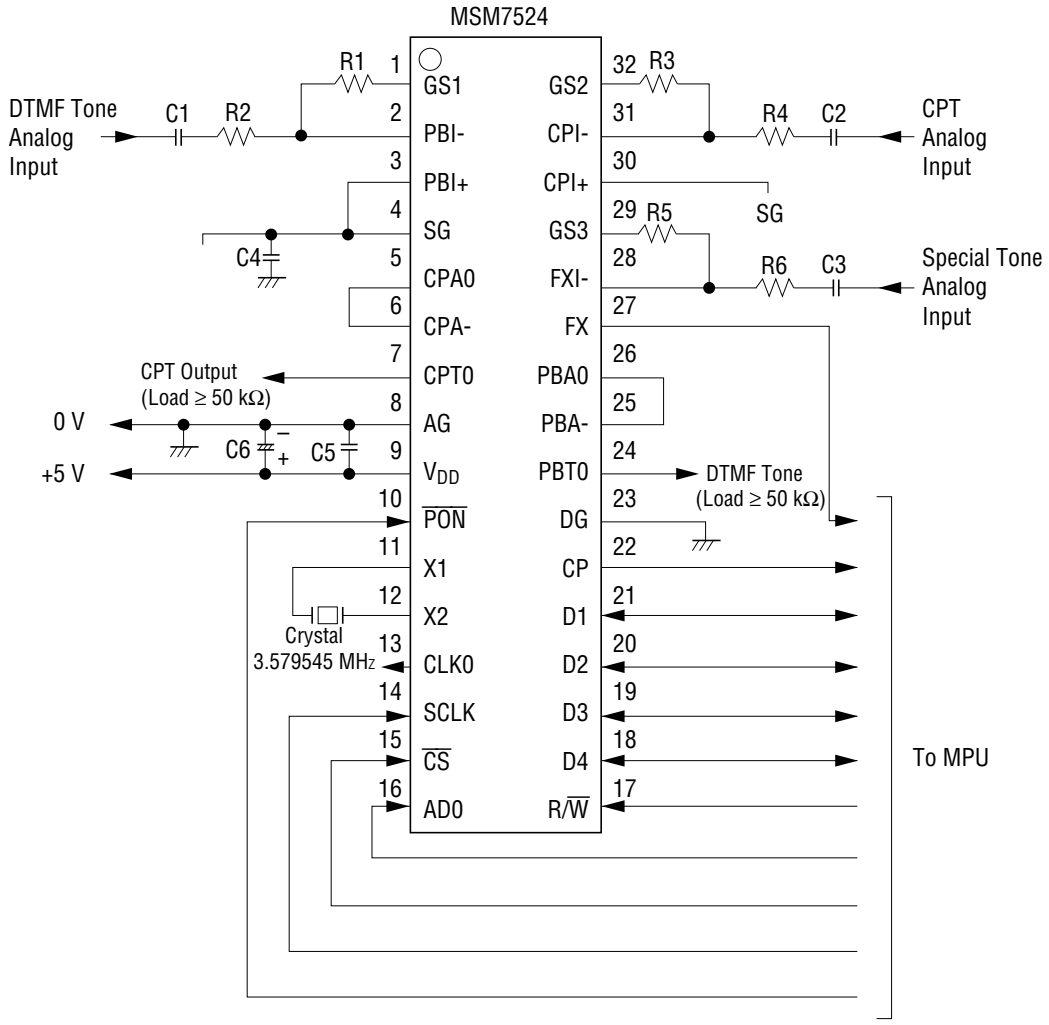
An example of the micro-processor control for each mode is shown in Table-6.

Mode	Processor Control		$\overline{CS}$	AD0	R/$\overline{W}$	D4	D3	D2	D1	Valid Register
Power ON	① Clear CRA. (CRB is selected next.)		0	1	0	1	0	0	0	CRA
	② Clear CRB. (CRA is selected next.)		0	1	0	0	0	0	0	CRB
	③ Next mode is selected.		0	1	0	X	X	X	X	CRA
DTMF Tone Receive	① Observe STR. (Non detect state)		0	1	1	1	0	0	0	STR
	② Observe STR. (Detect state)		0	1	1	0	1	0	1	STR
	③ Observe STR. (Detect state or After read STR)		0	1	1	0	0	0	0	STR
	④ Read RR.		0	0	1	X	X	X	X	RR
	⑤ Observe STR. (For next tone)		0	1	1	1	0	0	0	STR
CPT Detect	① CPT detect enable.		0	1	0	0	—	1	0	CRA
	② Observe STR. (Non detect state)		0	1	1	1	0	0	0	STR
	③ Observe STR. (Detect state)		0	1	1	1	0	1	1	STR
	④ Observe STR*. (Detect state or After read STR)		0	1	1	1	0	0	0	STR
DTMF Tone Transmit	① DTMF tone data.		0	0	0	X	X	X	X	TR
	② DTMF tone transmit "Make".		0	1	0	0	—	0	1	CRA
	③ DTMF tone transmit "Break".		0	1	0	0	—	0	0	CRA
CPT Transmit	① Select CRB.	Transmit "Make"	0	1	0	1	—	0	0	CRA
	② CPT transmit ON.		0	1	0	X	X	1	—	CRB
	③ Select CRB.	Transmit "Break"	0	1	0	1	—	0	0	CRA
	④ CPT transmit OFF.		0	1	0	X	X	0	—	CRB

* CP is still held on digital "1" while CPT is detected.

Note) CPT : Call Progress Tone
CRA : Control Resister A
CRB : Control Register B
STR : Status Register
TR : DTMF Tone Transmit Register
RR : DTMF Tone Receive Register
X : Expected Data
— : Digital " 0" or "1"

APPLICATION CIRCUIT



R1 to R6 ≥ 50 kΩ, C1, C2, C3 = 0.22 µF, C4, C5 = 1 µF, C6 = 10 µF

DTMF Tone : R1/R2 *R1 = R2 = 50 kΩ, Receive Range : –40 to 0 dBm
Receive Gain

CPT Detect : R3/R4 *R3 = R4 = 50 kΩ, Detect Range : –40 to 0 dBm
Gain

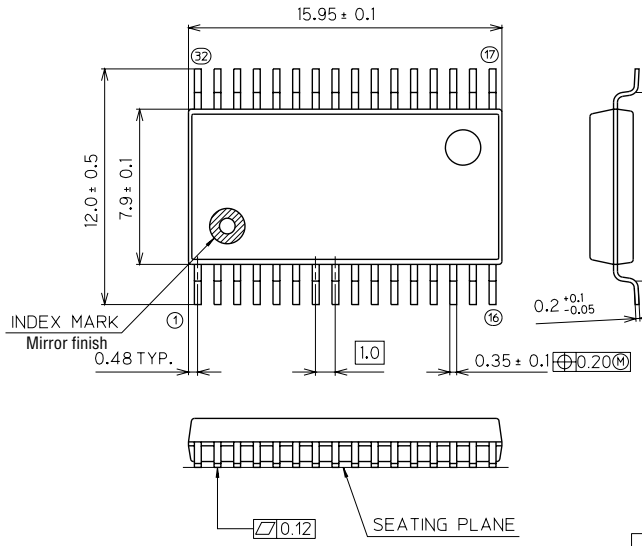
Special Tone : R5/R6 *R5 = 100 kΩ, Detect Range : –40 to 6 dBm
Detect Gain R6 = 50 kΩ

Note) The decoupling capacitors (C4, C5, C6) should be connected close to the device.

PACKAGE DIMENSIONS

(Unit : mm)

SSOP32-P-430-1.00-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.60 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).