

## Single-Ended Bus Transceiver

### Features

- Single-Ended Transceiver
- Survives Shorts and Transients on Automotive Bus
- Wide Power Supply Voltage Range
- Fault Detection
- ISO 9141 Compatible

### Description

The Si9243EY is a monolithic bus transceiver designed to provide bidirectional serial communication in automotive diagnostic applications.

The device incorporates protection against overvoltages and short circuits to GND or  $V_B$ . The transceiver pin is protected and can be driven beyond the  $V_{BAT}$  voltage.

The Si9243EY contains temperature and short circuit fault detection circuits. In the transmit mode, load shorts and opens are generally detected by the processor monitoring RXK and TX. When the two mirror each other there is no fault, but the Si9243EY will turn off the K output in the event of over temperature or short circuit to

$V_{BAT}$  to protect the IC. The fault will be reset when TX toggles “high.”

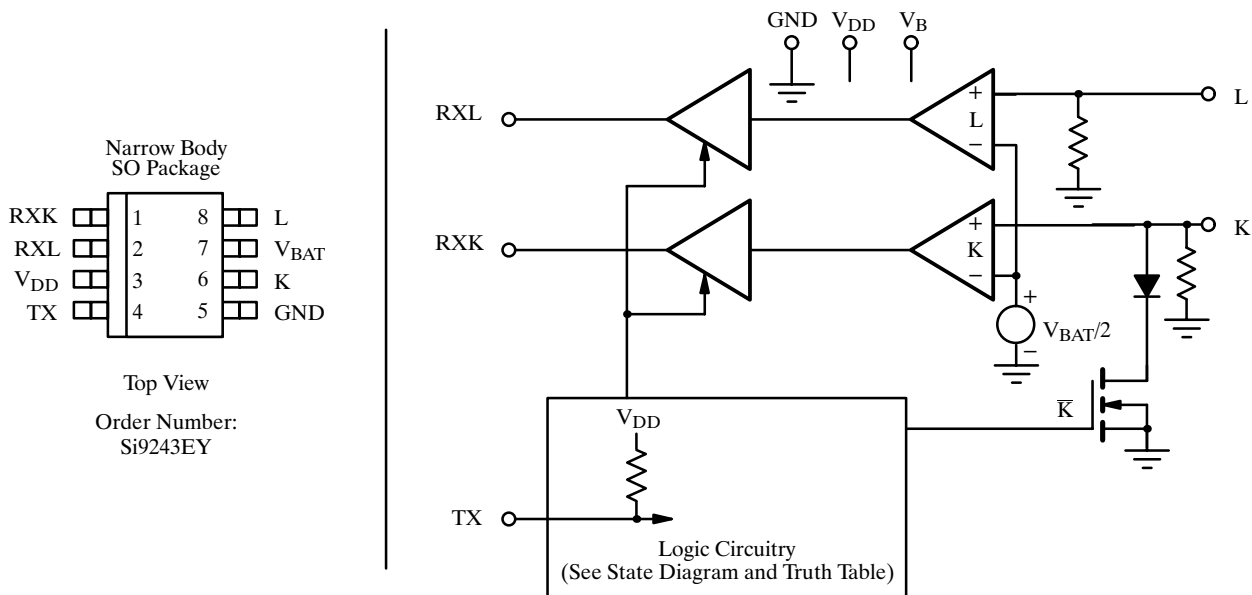
TX is set “high” for receive only.

The RX output is capable of driving CMOS or  $1 \times$  LSTTL load.

The Si9243EY is built on the Siliconix BiC/DMOS process. This process supports bipolar transistors, CMOS, and DMOS. An epitaxial layer prevents latchup.

The Si9243EY is available in a 8-pin SO package and operates over the automotive temperature range ( $-40$  to  $125^\circ\text{C}$ ).

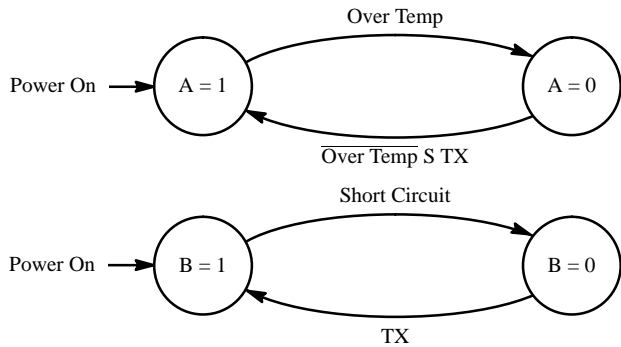
### Pin Configuration and Functional Block Diagram



Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70017. Application Note AN602 may also be obtained via FaxBack, request document #70573.

# Si9243EY

## Output Table and State Diagrams



Note: Over Temp is a condition and not meant to be a logic signal.

Inputs	State Variable		Output Table				Comments
	TX	A	B	K	RXK	L	
0	1	1	0	0	0	0	Over Temp Short Circuit
1	1	1	1	1	1	1	
0	1	1	0	0	1	1	
1	1	1	1	1	0	0	
X	0	1	HiZ	K	L	L	
0	1	0	HiZ	1	L	L	
1	1	1	1	1	1	1	Receive Mode
1	1	1	0	0	0	0	

X = "1" or "0"  
HiZ = High Impedance State

## Absolute Maximum Ratings

Voltage Referenced to Ground

Voltage On  $V_{BAT}$  ..... 45 V

Voltage K, L ..... -16 V to  $V_{BAT} + 1$  V

Voltage On Any Pin (Except  $V_{BAT}$ , K, L)

or Max. Current ..... -0.3 V to  $V_{DD} + 0.3$  V or 10 mA

Voltage on  $V_{DD}$  ..... 7 V

Short Circuit Duration (to  $V_{BAT}$  or GND) ..... Continuous

Operating Temperature ( $T_A$ ) ..... -40 to 125°C

Junction and Storage Temperature ..... -55 to 150°C

Thermal Resistance  $\Theta_{JA}$  ..... 125°C/W

## Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_{DD} = 4.5$ to $5.5$ V, $V_{BAT} = 7.25$ to $35$ V	Temp <sup>a</sup>	Limits E Suffix: -40 to 125°C			Unit
				Min <sup>b</sup>	Typ <sup>c</sup>	Max <sup>b</sup>	
<b>Transmitter and Logic Levels</b>							
TX Input Low Voltage	$V_{ILT}$		Full			1.5	V
TX Input High Voltage	$V_{IHT}$		Full	3.5			
K Output Low Voltage	$V_{OLK}$	$R_L = 510 \Omega$ , $C_L = 10$ nF $V_{BAT} = 35$ V, $V_{DD} = 4.5$ V	Full			4.9	V
			Full			$0.2 V_{BAT}$	
K Output High Voltage	$V_{OHK}$	$R_L = 510 \Omega$ , $C_L = 10$ nF See Test Circuit	Full	$0.91 V_{BAT}$			V
K Rise, Fall Times	$t_r$ , $t_f$		Full			9.6	
K Output Sink Resistance	$R_{si}$	TX = 0 V	Full			110	$\Omega$
K Output Capacitance <sup>d</sup>	$C_O$		Full			20	pF
TX Input Capacitance <sup>d</sup>	$C_{INT}$		Full			10	pF
TX Input Current	$I_{INT}$	$V_{DD} = 5.5$ V, TX = 1.5 V, 3.5 V	Full	-60		-4	$\mu$ A

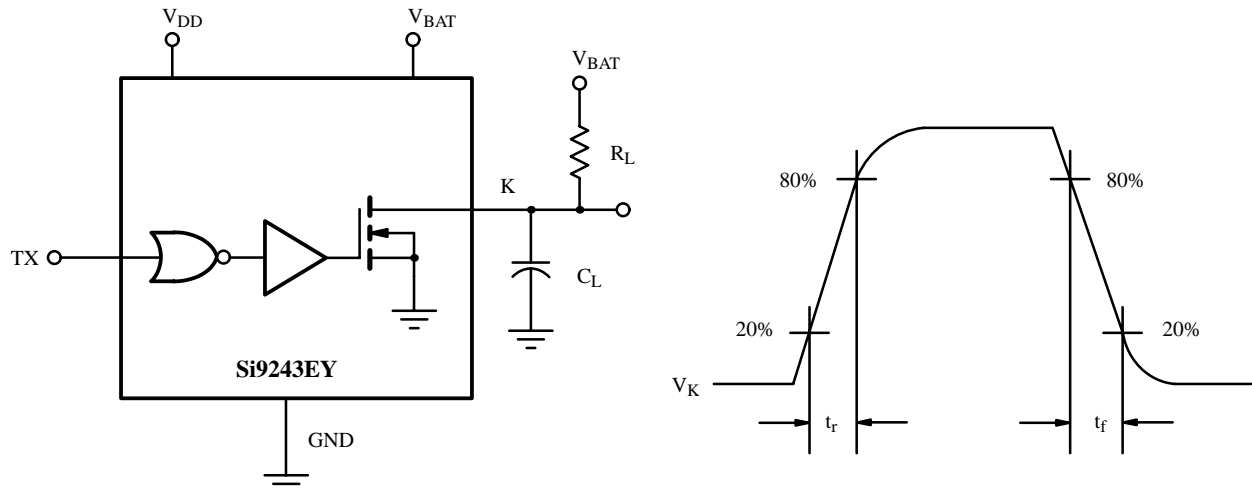
## Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_{DD} = 4.5$ to $5.5$ V, $V_B = 7.25$ to $35$ V	Temp <sup>a</sup>	Limits E Suffix: $-40$ to $125^\circ\text{C}$			Unit
				Min <sup>b</sup>	Typ <sup>c</sup>	Max <sup>b</sup>	
<b>Receiver</b>							
L and K Input Low Voltage	$V_{ILK}$		Full		$0.4 V_{BAT}$	$0.33 V_{BAT}$	V
L and K Input High Voltage	$V_{IHK}$		Full	$0.7 V_{BAT}$	$0.6 V_{BAT}$		
L and K Input Hysteresis <sup>d</sup>	$V_{HYS}$		Full	$0.1 V_{BAT}$			
RXL and RXK Output Low Voltage	$V_{OLR}$	TX = 4 V	Full	$V_{ILK}, V_{ILL} = 0.33 V_{BAT}$ $I_{OLR} = 1$ mA		0.4	
RXL and RXK High Voltage	$V_{OHR}$			$V_{IHK}, V_{IHL} = 0.70 V_{BAT}$ $I_{OHR} = -40$ $\mu\text{A}$			
L and K Input Currents	$I_{IHK}$			$V_{IHK} = V_B$			
<b>Supplies</b>							
Bat Supply Current	$I_{BAT}$	TX = 1.5 V, K, L Open	Full		2.7	5.0	mA
Logic Supply Current	$I_{DD}$	TX = 1.5 V, K, L Open	Full		1	3.0	
<b>Miscellaneous</b>							
Baud Rate	BR	$R_L = 510 \Omega$ , $C_L = 10$ nF	Full	10.4			kBaud
TX Minimum Pulse Width <sup>d, e</sup>	$t_{TX}$		Full	1			$\mu\text{s}$

### Notes

- Room =  $25^\circ\text{C}$ , Cold and Hot = as determined by the operating temperature suffix.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- Guaranteed by design, not subject to production test.
- Minimum pulse width to reset a fault condition.

## Test Circuit



# Si9243EY

## Application Circuit

