HARRIS Semiconductor

HA-5127/883

July 1994

Ultra Low Noise, Precision Operational Amplifier

Features

- **This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **High Slew Rate . . . . . 7V/μs (Min)**
- **Unity Gain Bandwidth . . . . . 5MHz (Min)**
- **Low Noise Voltage (at 1kHz) . . . . . 4.5nV/$\sqrt{Hz}$ (Max)**
- **Low Offset Voltage. . . . . .100μV (Max)**
- **Low Offset Drift With Temperature. . . . 1.8μV/^{o}C (Max)**
- **High CMRR . . . . . .100dB (Min)**
- **High Voltage Gain . . . . . 700kV/V (Min)**

Applications

- **High Speed Signal Conditioners**
- **Wide Bandwidth Instrumentation Amplifiers**
- **Low Level Transducer Amplifiers**
- **Fast, Low Level Voltage Comparators**
- **Highest Quality Audio Preamplifiers**
- **Pulse/RF Amplifiers**

The HA-5127/883 monolithic operational amplifier features an excellent combination of precision DC and wideband high speed characteristics. Utilizing the Harris D.I. technology and advanced processing techniques, this unique design unites low noise precision instrumentation performance with high speed, wideband capability.

This amplifier's impressive list of features include low V_{OS}, wide gain-bandwidth, high open loop gain, and high CMRR. Additionally, this flexible device operates over a wide supply range while consuming only 120mW of power.

Using the HA-5127/883 allows designers to minimize errors while maximizing speed and bandwidth.

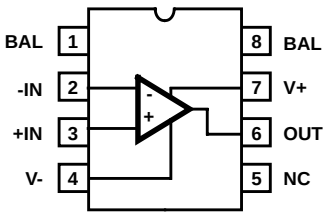
This device is ideally suited for low level transducer signal amplifier circuits. Other applications which can utilize the HA-5127/883's qualities include instrumentation amplifiers, pulse or RF amplifiers, audio preamplifiers, and signal conditioning circuits.

Ordering Information

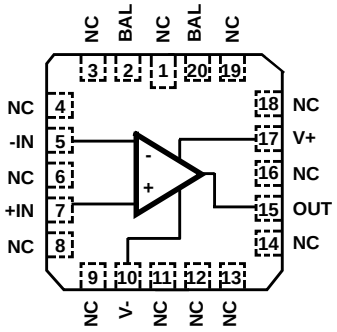
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA2-5127/883	-55^{o}C to +125^{o}C	8 Pin Can
HA4-5127/883	-55^{o}C to +125^{o}C	20 Lead Ceramic LCC
HA7-5127/883	-55^{o}C to +125^{o}C	8 Lead CerDIP

Pinouts

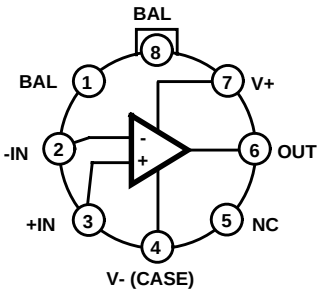
HA-5127/883 (CERDIP)
TOP VIEW



HA-5127/883 (CLCC)
TOP VIEW



HA-5127/883 (METAL CAN)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

Spec Number **511008-883**
File Number **3751**

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 44V
Differential Input Voltage (Note 2) 0.7V
Voltage at Either Input Terminal . . . . . V+ to V-
Input Current. 25mA
Differential Output Current . . . . . Full Short Circuit Protection
Junction Temperature (T_J) . . . . . +175°C
Storage Temperature Range . . . . . -65°C to +150°C
ESD Rating. . . . . <2000V
Lead Temperature (Soldering 10s) . . . . . +300°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
CerDIP Package	115°C/W	28°C/W
Ceramic LCC Package	65°C/W	15°C/W
Metal Can Package	155°C/W	67°C/W

Package Power Dissipation Limit at +75°C for $T_J \leq +175°C$
CerDIP Package 870mW
Ceramic LCC Package 1.54W
Metal Can Package 645mW
Package Power Dissipation Derating Factor Above +75°C
CerDIP Package . . . . . 8.7mW/°C
Ceramic LCC Package . . . . . 15.4mW/°C
Metal Can Package . . . . . 6.5mW/°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions

Operating Temperature Range . . . . . -55°C to +125°C
Operating Supply Voltage . . . . . ±15V

$V_{INCM} \leq 1/2\ (V+ - V-)$
$R_L \geq 600\Omega$

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $V_{SUPPLY} = \pm 15V$, $R_{SOURCE} = 50\Omega$, $R_{LOAD} = 100k\Omega$, $V_{OUT} = 0V$, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Offset Voltage	V_{IO}	$V_{CM} = 0V$	1	+25°C	-100	100	µV
			2, 3	+125°C, -55°C	-300	300	µV
Input Bias Current	I_B	$V_{CM} = 0V$, $R_S = 10k\Omega, 50\Omega$ $\left(\frac{\lvert +I_B \rvert + \lvert -I_B \rvert}{2}\right)$	1	+25°C	-	80	nA
			2, 3	+125°C, -55°C	-	150	nA
Input Offset Current	I_{IO}	$V_{CM} = 0V$, $+R_S = 10k\Omega$, $-R_S = 10k\Omega$	1	+25°C	-75	75	nA
			2, 3	+125°C, -55°C	-135	135	nA
Common Mode Range	+CMR	V+ = +4.7V, V- = -25.3V	1	+25°C	10.3	-	V
			2, 3	+125°C, -55°C	10.3	-	V
	-CMR	V+ = +25.3V, V- = -4.7V	1	+25°C	-	-10.3	V
			2, 3	+125°C, -55°C	-	-10.3	V
Large Signal Voltage Gain	$+A_{VOL}$	$V_{OUT} = 0V$ and +10V, $R_L = 2k\Omega$	4	+25°C	700	-	kV/V
			5, 6	+125°C, -55°C	300	-	kV/V
	$-A_{VOL}$	$V_{OUT} = 0V$ and -10V, $R_L = 2k\Omega$	4	+25°C	700	-	kV/V
			5, 6	+125°C, -55°C	300	-	kV/V
Common Mode Rejection Ratio	+CMRR	$\Delta V_{CM} = +11V$	1	+25°C	100	-	dB
		$\Delta V_{CM} = +10V$	2, 3	+125°C, -55°C	100	-	dB
	-CMRR	$\Delta V_{CM} = -11V$	1	+25°C	100	-	dB
		$\Delta V_{CM} = -10V$	2, 3	+125°C, -55°C	100	-	dB

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: V_{SUPPLY} = ±15V, R_{SOURCE} = 50Ω, R_{LOAD} = 100kΩ, V_{OUT} = 0V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Output Voltage Swing	$+V_{OUT1}$	R_L = 2kΩ	4	+25°C	11.5	-	V
			5, 6	+125°C, -55°C	11.5	-	V
	$-V_{OUT1}$	R_L = 2kΩ	4	+25°C	-	-11.5	V
			5, 6	+125°C, -55°C	-	-11.5	V
	$+V_{OUT2}$	R_L = 600Ω	4	+25°C	10	-	V
	$-V_{OUT2}$	R_L = 600Ω	4	+25°C	-	-10	V
Output Current	$+I_{OUT}$	V_{OUT} = -10V	4	+25°C	16.5	-	mA
	$-I_{OUT}$	V_{OUT} = +10V	4	+25°C	-	-16.5	mA
Quiescent Power Supply Current	$+I_{CC}$	V_{OUT} = 0V, I_{OUT} = 0mA	1	+25°C	-	4	mA
			2, 3	+125°C, -55°C	-	4	mA
	$-I_{CC}$	V_{OUT} = 0V, I_{OUT} = 0mA	1	+25°C	-4	-	mA
			2, 3	+125°C, -55°C	-4	-	mA
Power Supply Rejection Ratio	+PSRR	ΔV_{SUP} = 14V	1	+25°C	86	-	dB
		ΔV_{SUP} = 13.5V	2, 3	+125°C, -55°C	86	-	dB
	-PSRR	ΔV_{SUP} = 14V	1	+25°C	86	-	dB
		ΔV_{SUP} = 13.5V	2, 3	+125°C, -55°C	86	-	dB
Offset Voltage Adjustment	$+V_{IO}$Adj	Note 1	1	+25°C	V_{IO}-1	-	mV
			2, 3	+125°C, -55°C	V_{IO}-1	-	mV
	$-V_{IO}$Adj	Note 1	1	+25°C	V_{IO}+1	-	mV
			2, 3	+125°C, -55°C	V_{IO}+1	-	mV

NOTE:

1. Offset adjustment range is [V_{IO} (Measured) ±1mV] minimum referred to output. This test is for functionality only to assure adjustment through 0V.
2. For differential input voltages greater than 0.7V, the input current must be limited to 25mA to protect the back-to-back input diodes.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: V_{SUPPLY} = ±15V, R_{SOURCE} = 50Ω, R_{LOAD} = 2kΩ, C_{LOAD} = 50pF, A_{VCL} = +1V/V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Slew Rate	+SR	V_{OUT} = -3V to +3V	7	+25°C	7	-	V/µs
	-SR	V_{OUT} = +3V to -3V	7	+25°C	7	-	V/µs
Rise and Fall Time	t_R	V_{OUT} = 0 to +200mV 10% ≤ T_R ≤ 90%	7	+25°C	-	150	ns
	t_F	V_{OUT} = 0 to -200mV 10% ≤ T_F ≤ 90%	7	+25°C	-	150	ns
Overshoot	+OS	V_{OUT} = 0 to +200mV	7	+25°C	-	40	%
	-OS	V_{OUT} = 0 to -200mV	7	+25°C	-	40	%

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: V_{SUPPLY} = ±15V, R_{LOAD} = 2kΩ, C_{LOAD} = 50pF, A_V = +1V/V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		
					MIN	MAX	UNITS
Average Offset Voltage Drift	$V_{IO}TC$	V_{CM} = 0V	1	-55°C to +125°C	-	1.8	µV/°C
Differential Input Resistance	R_{IN}	V_{CM} = 0V	1	+25°C	0.8	-	MΩ
Low Frequency Peak-to-Peak Noise	E_{NP-P}	0.1Hz to 10Hz	1	+25°C	-	0.25	μV_{P-P}
Input Noise Voltage Density	E_N	R_S = 20Ω, f_O = 10Hz	1	+25°C	-	10.0	$nV/\sqrt{Hz}$
		R_S = 20Ω, f_O = 100Hz	1	+25°C	-	5.6	$nV/\sqrt{Hz}$
		R_S = 20Ω, f_O = 1kHz	1	+25°C	-	4.5	$nV/\sqrt{Hz}$
Input Noise Current Density	I_N	R_S = 2MΩ, f_O = 10Hz	1	+25°C	-	4.0	$pA/\sqrt{Hz}$
		R_S = 2MΩ, f_O = 100Hz	1	+25°C	-	2.3	$pA/\sqrt{Hz}$
		R_S = 2MΩ, f_O = 1kHz	1	+25°C	-	0.6	$pA/\sqrt{Hz}$
Unity Gain Bandwidth	UGBW	V_O = 100mV	1	+25°C	5	-	MHz
Full Power Bandwidth	FPBW	V_{PEAK} = 10V	1, 2	+25°C	111	-	kHz
Minimum Closed Loop Stable Gain	CLSG	R_L = 2kΩ, C_L = 50pF	1	-55°C to +125°C	±1	-	V/V
Settling Time	t_S	To 0.1% for a 10V Step	1	+25°C	-	2	µs
Output Resistance	R_{OUT}	Open Loop	1	+25°C	-	100	Ω
Quiescent Power Consumption	PC	V_{OUT} = 0V, I_{OUT} = 0mA	1, 3	-55°C to +125°C	-	120	mW

NOTES:

1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.
2. Full Power Bandwidth guarantee based on Slew Rate measurement using FPBW = Slew Rate/($2\pi V_{PEAK}$).
3. Quiescent Power Consumption based upon Quiescent Supply Current test maximum. (No load on output.)

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 AND 2) (NOTE 2)
Interim Electrical Parameters (Pre Burn-In)	1
Final Electrical Test Parameters	1 (Note 1), 2, 3, 4, 5, 6, 7
Group A Test Requirements	1, 2, 3, 4, 5, 6, 7
Groups C and D Endpoints	1

NOTES:

1. PDA applies to Subgroup 1 only.
2. The Subgroup assignments of the parameters in these tables were patterned after Mil-M-38510/135, with the exception of V_{IO}, which is Subgroups 1, 2, 3.

Die Characteristics

DIE DIMENSIONS:
104 x 65 x 19 mils ± 1 mils
2650 x 1650 x 483µm ± 25.4µm

METALLIZATION:
Type: Al, 1% Cu
Thickness: 16kÅ ± 2kÅ

GLASSIVATION:
Type: Nitride (Si3N4) over Silox (SiO2, 5% Phos.)
Silox Thickness: 12kÅ ± 2kÅ
Nitride Thickness: 3.5kÅ ± 1.5kÅ

WORST CASE CURRENT DENSITY:
3.6 x 10^5A/cm^2
This device meets Glassivation Integrity Test Requirement per MIL-STD-883 Method 2021 and MIL-I-38535 Paragraph 30.5.5.4.

SUBSTRATE POTENTIAL (Powered Up): V-

TRANSISTOR COUNT: 63

PROCESS: Bipolar Dielectric Isolation

Metallization Mask Layout

HA-5127/883