Low Power High Speed Operational Amplifier

FEATURES

- 1mA Supply Current
- 50V/µs Slew Rate
- 11MHz Gain Bandwidth
- Unity Gain Stable
- 430ns Settling Time to 0.1%, 10V Step
- 6V/mV DC Gain, R_L = 2kΩ
- 1mV Maximum Input Offset Voltage
- 50nA Input Offset Current
- 500nA Input Bias Current
- ±12V Minimum Output Swing into 2kΩ
- Wide Supply Range ±2.5V to ±15V
- Drives All Capacitive Loads

APPLICATIONS

- Wideband Amplifiers
- Buffers
- Active Filters
- Data Acquisition Systems

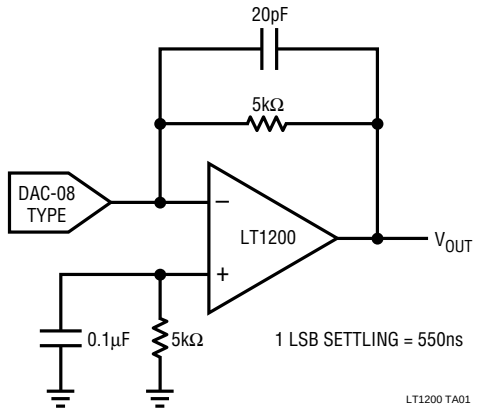
DESCRIPTION

The LT1200 is a low power high speed operational amplifier with excellent DC performance. The LT1200 features much lower supply current than devices with comparable bandwidth and slew rate. The circuit is a single gain stage with outstanding settling characteristics. The fast settling time makes the circuit an ideal choice for data acquisition systems. The output is capable of driving a 2kΩ load to ±12V with ±15V supplies and a 500Ω load to ±3V on ±5V supplies. The circuit is also capable of driving large capacitive loads which makes it useful in buffer or cable driver applications.

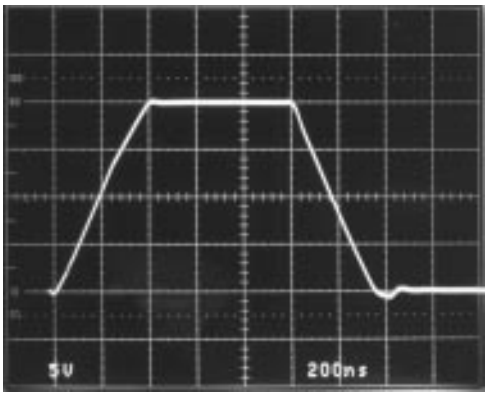
The LT1200 is a member of a family of fast, high performance amplifiers that employ Linear Technology Corporation's advanced bipolar complementary processing.

TYPICAL APPLICATION

DAC Current to Voltage Converter



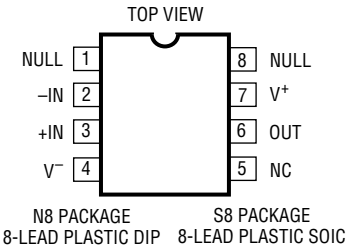
Inverter Pulse Response



ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 36V
Differential Input Voltage ..... ±6V
Input Voltage ..... $\pm V_S$
Output Short Circuit Duration (Note 1) ..... Indefinite
Operating Temperature Range
LT1200C..... 0°C to 70°C
Maximum Junction Temperature
Plastic Package ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec.)..... 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LT1200CN8 LT1200CS8

ELECTRICAL CHARACTERISTICS

V_S = ±15V, T_A = 25°C, V_{CM} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 2)		0.5	1.0	mV
I_{OS}	Input Offset Current			50	100	nA
I_B	Input Bias Current			0.5	1.0	µA
e_n	Input Noise Voltage	f = 10kHz		30		$nV/\sqrt{Hz}$
i_n	Input Noise Current	f = 10kHz		0.7		$pA/\sqrt{Hz}$
R_{IN}	Input Resistance	V_{CM} = ±12V	48	90		MΩ
	Input Resistance	Differential		500		kΩ
C_{IN}	Input Capacitance			2		pF
	Input Voltage Range$^+$		12	14		V
	Input Voltage Range$^-$			–13	–12	V
CMRR	Common Mode Rejection Ratio	V_{CM} = ±12V	80	100		dB
PSRR	Power Supply Rejection Ratio	V_S = ±5V to ±15V	80	90		dB
A_{VOL}	Large Signal Voltage Gain	V_{OUT} = ±10V, R_L = 5kΩ V_{OUT} = ±10V, R_L = 2kΩ	4 3	8 6		V/mV V/mV
V_{OUT}	Output Swing	R_L = 2kΩ	12.0	13.8		±V
I_{OUT}	Output Current	V_{OUT} = ±12V	6	12		mA
SR	Slew Rate	A_{VCL} = –2, (Note 3)	30	50		V/µs
	Full Power Bandwidth	10V Peak, (Note 4)		0.8		MHz
GBW	Gain Bandwidth	f = 0.1MHz		11		MHz
t_r, t_f	Rise Time, Fall Time	A_{VCL} = +1, 10% to 90%, 0.1V		18		ns
	Overshoot	A_{VCL} = +1, 0.1V		25		%
	Propagation Delay	50% V_{IN} to 50% V_{OUT}		18		ns
t_s	Settling Time	10V Step, 0.1%		430		ns
R_O	Output Resistance	A_{VCL} = +1, f = 0.1MHz		1.1		Ω
I_S	Supply Current			1	1.4	mA

ELECTRICAL CHARACTERISTICS $V_S = \pm5V$, $T_A = 25°C$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 2)		1.0	3.0	mV
I_{OS}	Input Offset Current			50	100	nA
I_B	Input Bias Current			0.5	1.0	µA
	Input Voltage Range$^+$		2.5	4		V
	Input Voltage Range$^-$			–3	–2.5	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm2.5V$	80	100		dB
A_{VOL}	Large Signal Voltage Gain	$V_{OUT} = \pm2.5V$, $R_L = 2k\Omega$ $V_{OUT} = \pm2.5V$, $R_L = 1k\Omega$	2.5 2.0	5 4		V/mV V/mV
V_{OUT}	Output Voltage	$R_L = 500\Omega$	3.0	4.0		±V
I_{OUT}	Output Current	$V_{OUT} = \pm3V$	6	12		mA
SR	Slew Rate	$A_{VCL} = –2$, (Note 3)	20	33		V/µs
	Full Power Bandwidth	3V Peak, (Note 4)		1.7		MHz
GBW	Gain Bandwidth	f = 0.1MHz		8.5		MHz
t_r, t_f	Rise Time, Fall Time	$A_{VCL} = +1$, 10%-90%, 0.1V		23		ns
	Overshoot	$A_{VCL} = +1$, 0.1V		20		%
	Propagation Delay	50% V_{IN} to 50% V_{OUT}		23		ns
t_s	Settling Time	–2.5V to 2.5V, 0.1%		300		ns
I_S	Supply Current			1	1.4	mA

ELECTRICAL CHARACTERISTICS $0°C \le T_A \le 70°C$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_S = \pm15V$, (Note 2) $V_S = \pm5V$, (Note 2)		0.5 1.0	2.0 3.5	mV mV
	Input V_{OS} Drift			11		µV/°C
I_{OS}	Input Offset Current	$V_S = \pm15V$ and $V_S = \pm5V$		50	150	nA
I_B	Input Bias Current	$V_S = \pm15V$ and $V_S = \pm5V$		0.5	1.2	µA
CMRR	Common Mode Rejection Ratio	$V_S = \pm15V$, $V_{CM} = \pm12V$; $V_S = \pm5V$, $V_{CM} = \pm2.5V$	80	100		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm5V$ to $\pm15V$	80	90		dB
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm15V$, $V_{OUT} = \pm10V$, $R_L = 5k\Omega$ $V_S = \pm15V$, $V_{OUT} = \pm10V$, $R_L = 2k\Omega$ $V_S = \pm5V$, $V_{OUT} = \pm2.5V$, $R_L = 2k\Omega$ $V_S = \pm5V$, $V_{OUT} = \pm2.5V$, $R_L = 1k\Omega$	3.5 2.5 2.0 1.6	8 6 5 4		V/mV V/mV V/mV V/mV
V_{OUT}	Output Swing	$V_S = \pm15V$, $R_L = 2k\Omega$ $V_S = \pm5V$, $R_L = 500\Omega$	12.0 3.0	13.8 4.0		±V ±V
I_{OUT}	Output Current	$V_S = \pm15V$, $V_{OUT} = \pm12V$ $V_S = \pm5V$, $V_{OUT} = \pm3V$	6 6	12 12		mA mA
SR	Slew Rate	$V_S = \pm15V$, $A_{VCL} = –2$, (Note 3) $V_S = \pm5V$, $A_{VCL} = –2$, (Note 3)	27 18	50 33		V/ms V/ms
I_S	Supply Current	$V_S = \pm15V$ and $V_S = \pm5V$		1	1.6	mA

Note 1: A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted indefinitely.

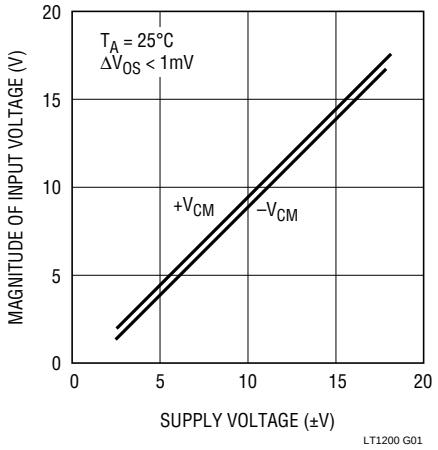
Note 2: Input offset voltage is tested with automated test equipment in <1 second.

Note 3: Slew rate is measured in a gain of –2 between ±10V on the output with ±6V on the input for ±15V supplies and ±2V on the output with ±1.75V on the input for ±5V supplies.

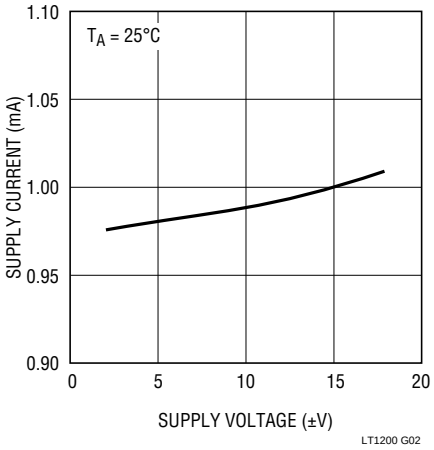
Note 4: Full power bandwidth is calculated from the slew rate measurement: FPBW = SR/2πVp.

TYPICAL PERFORMANCE CHARACTERISTICS

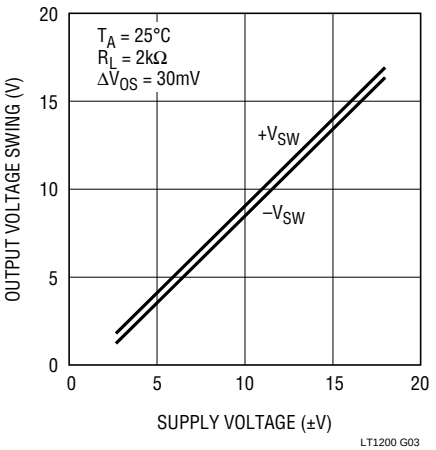
Input Common Mode Range vs Supply Voltage



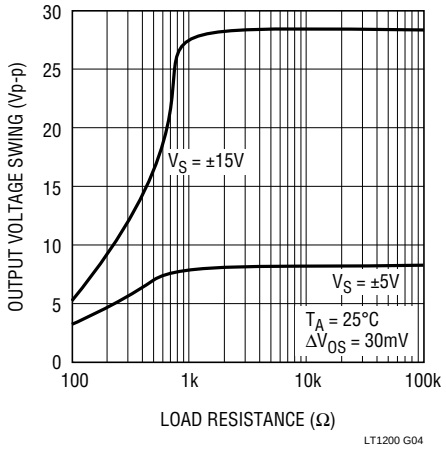
Supply Current vs Supply Voltage



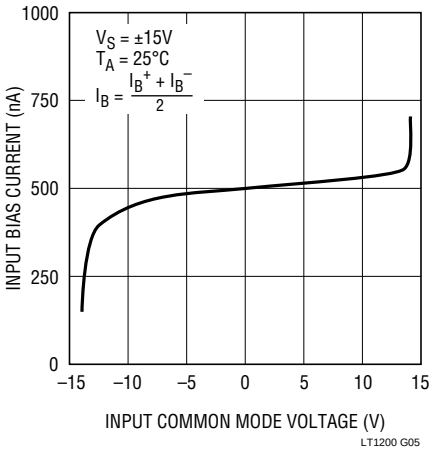
Output Voltage Swing vs Supply Voltage



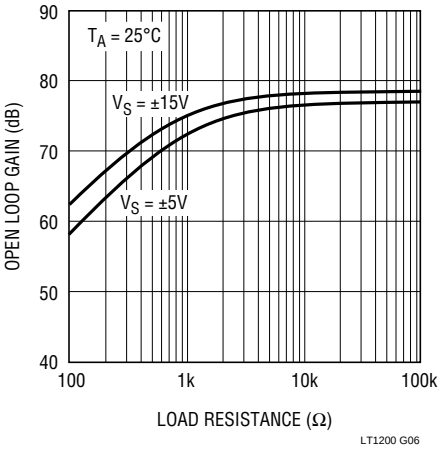
Output Voltage Swing vs Resistive Load



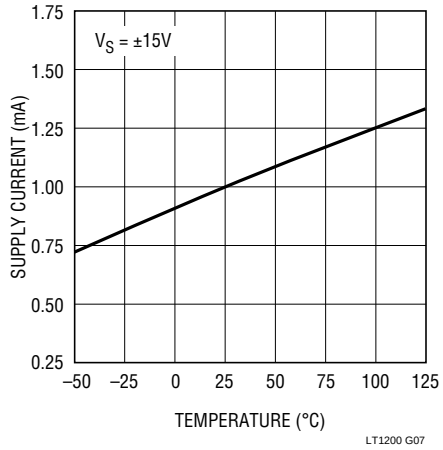
Input Bias Current vs Input Common Mode Voltage



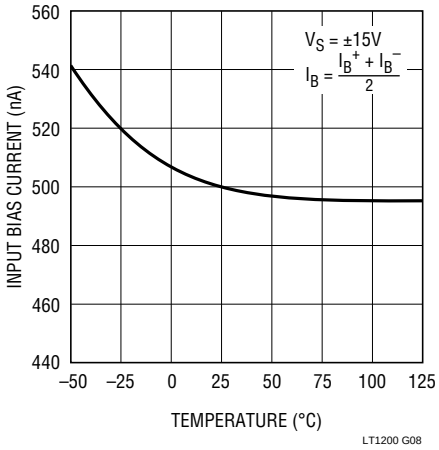
Open Loop Gain vs Resistive Load



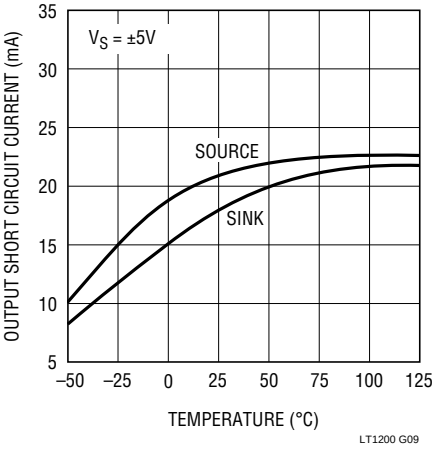
Supply Current vs Temperature



Input Bias Current vs Temperature

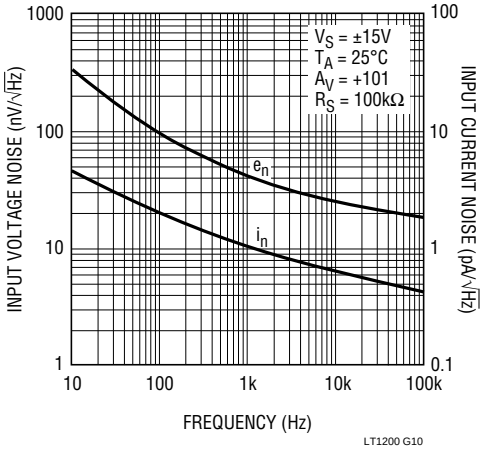


Output Short-Circuit Current vs Temperature

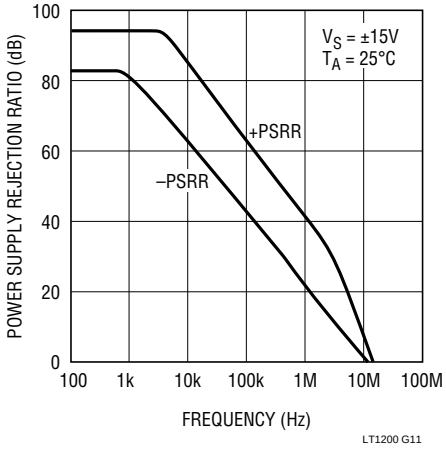


TYPICAL PERFORMANCE CHARACTERISTICS

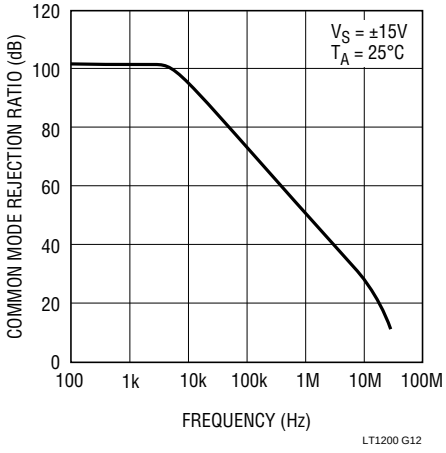
Input Noise Spectral Density



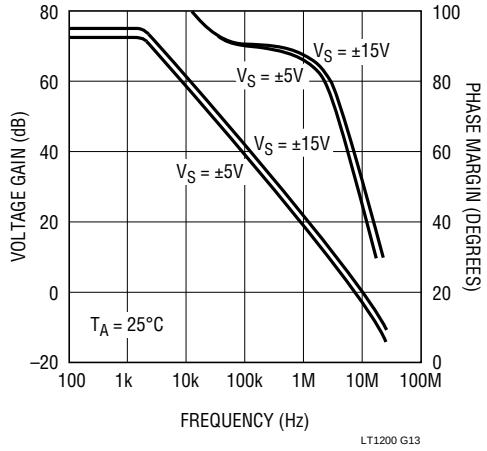
Power Supply Rejection Ratio vs Frequency



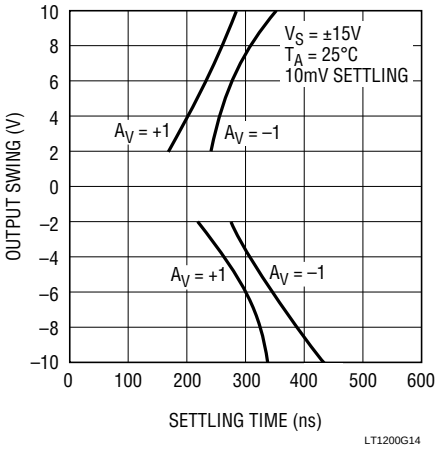
Common Mode Rejection Ratio vs Frequency



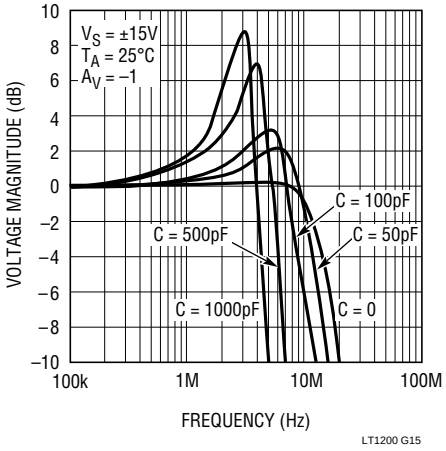
Voltage Gain and Phase vs Frequency



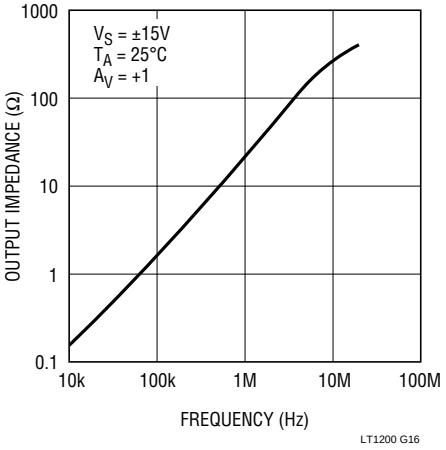
Output Swing vs Settling Time



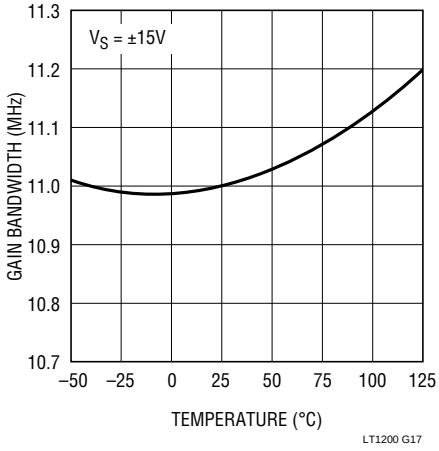
Frequency Response vs Capacitive Load



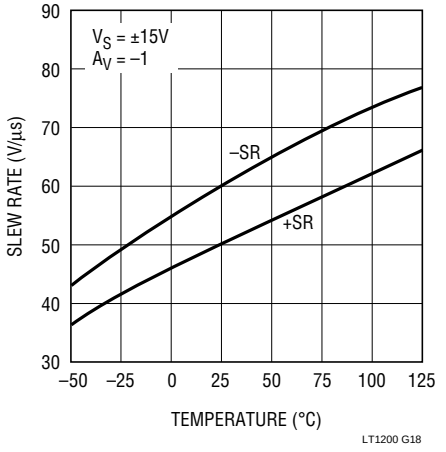
Closed Loop Output Impedance vs Frequency



Gain Bandwidth vs Temperature



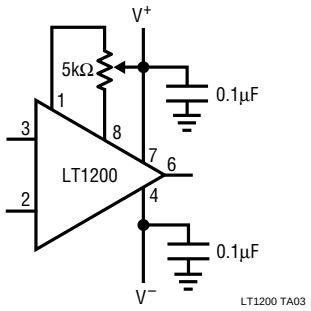
Slew Rate vs Temperature



APPLICATIONS INFORMATION

The LT1200 may be inserted directly into many applications, provided that the nulling circuitry is removed. The suggested nulling circuit for the LT1200 is shown below.

Offset Nulling



Layout and Passive Components

As with any high speed operational amplifier, care must be taken in board layout in order to obtain maximum performance. Key layout issues include: use of a ground plane, minimization of stray capacitance at the input pins, short lead lengths, RF-quality bypass capacitors located close to the device (typically 0.01μF to 0.1μF), and use of low ESR bypass capacitors for high drive current applications (typically 1μF to 10μF tantalum). Sockets should be avoided when maximum frequency performance is required, although low-profile sockets can provide reasonable performance up to 50MHz. For more details see Design Note 50. The parallel combination of the feedback resistor and gain setting resistor on the inverting input combine with the input capacitance to form a pole which can cause peaking. If feedback resistors greater than 5kΩ are used, a parallel capacitor of value:

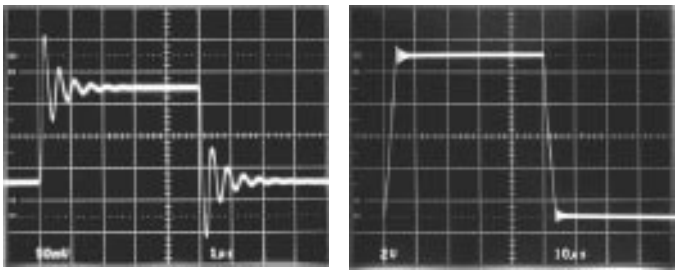
$$C_F \geq R_G \times \frac{C_{IN}}{R_F}$$

should be used to cancel the input pole and optimize dynamic performance. For unity gain applications where a large feedback resistor is used, C_F should be greater than or equal to C_{IN}.

Capacitive Loading

The LT1200 is stable with all capacitive loads. This is accomplished by sensing the load induced output pole and adding compensation at the amplifier gain node. As the capacitive load increases both the bandwidth and phase margin decrease so there will be peaking in the frequency domain and in the transient response. The photo of the small signal response with 1000pF load shows 50% peaking. The large signal response with a 10,000pF load shows the output slew rate being limited by the short-circuit current.

A_V = –1, C_L = 1000pF **A_V = +1, C_L = 10,000pF**



DAC Current to Voltage Converter

The wide bandwidth, high slew rate and fast settling time of the LT1200 make it well suited for current to voltage conversion after current output D/A converters. A typical application is shown on page one with a DAC-08 type converter with a full-scale output of 2mA. A compensation capacitor is used across the feedback resistor to null the pole at the inverting input caused by the DAC output capacitance. The combination of the LT1200 and DAC settles to 40mV in 550ns for a 10V to 0V step and 450ns for a 0V to 10V step.

Input Considerations

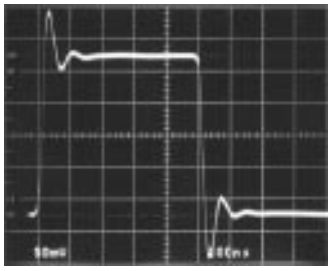
Resistors in series with the inputs are recommended for the LT1200 in applications where the differential input voltage exceeds ±6V continuously or on a transient basis. An example would be in noninverting configurations with high input slew rates or when driving heavy capacitive loads. The use of balanced source resistance at each input is recommended for applications where DC accuracy must be maximized.

APPLICATIONS INFORMATION

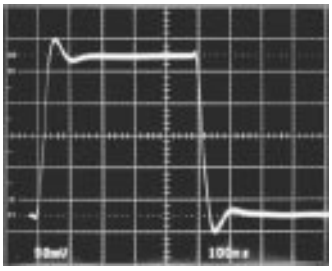
Transient Response

The LT1200 gain bandwidth is 11MHz when measured at 100kHz. The actual frequency response in unity gain is considerably higher than 11MHz due to peaking caused by a second pole beyond the unity gain crossover. This is reflected in the 45° phase margin and shows up as overshoot in the unity gain small signal transient response. Higher noise gain configurations exhibit less overshoot as seen in the inverting gain of one response.

Small Signal, A_V = +1



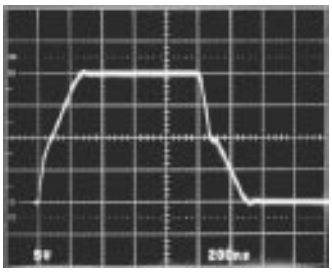
Small Signal, A_V = –1



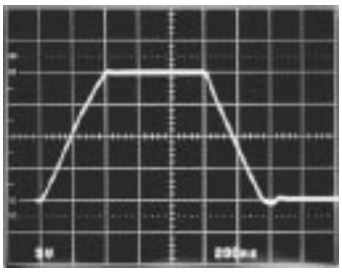
The large signal reponse in both inverting and noninverting gain shows symmetrical slewing characteristics. Normally the noninverting response has a much faster rising edge due to the rapid change in input common mode voltage which affects the tail current of the input differential pair. Slew enhancement circuitry has been added to the LT1200 so that the falling edge slew rate is enhanced which balances the noninverting slew rate.

The large signal, unity gain response shows the characteristic noninverting response of an op amp with an input slew rate much faster than that of the amplifier. In this case the input is slewing at greater than 1000V/µs.

Large Signal, A_V = +1



Large Signal, A_V = –1

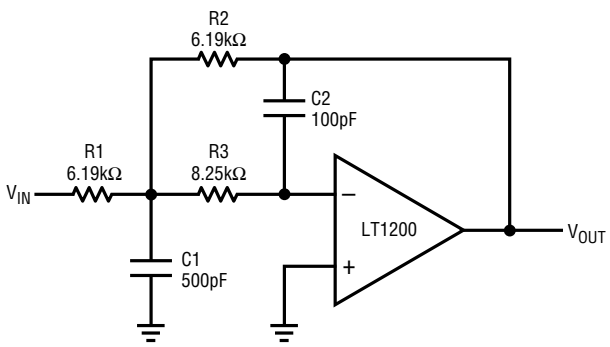


Low Voltage Operation

The LT1200 is functional at room temperature with only 3V of total supply voltage. Under this condition, however, the undistorted output swing is only $0.8V_{P-P}$. A more realistic condition is operation at ±2.5V supplies (or 5V and ground). Under these conditions at room temperature the typical input common mode range is +2.2V to –1.5V, and a 1MHz, $2.5V_{P-P}$ sine wave can be faithfully reproduced. With 5V total supply voltage the gain bandwidth is reduced to 6MHz and the slew rate is reduced to 20V/µs.

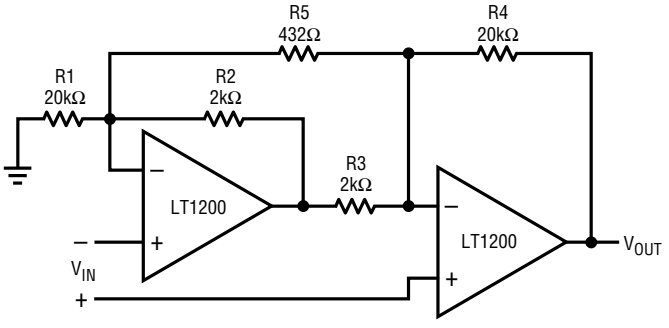
TYPICAL APPLICATIONS

100kHz, 2nd Order Butterworth Filter



LT1200 TA04

Two Op Amp Instrumentation Amplifier

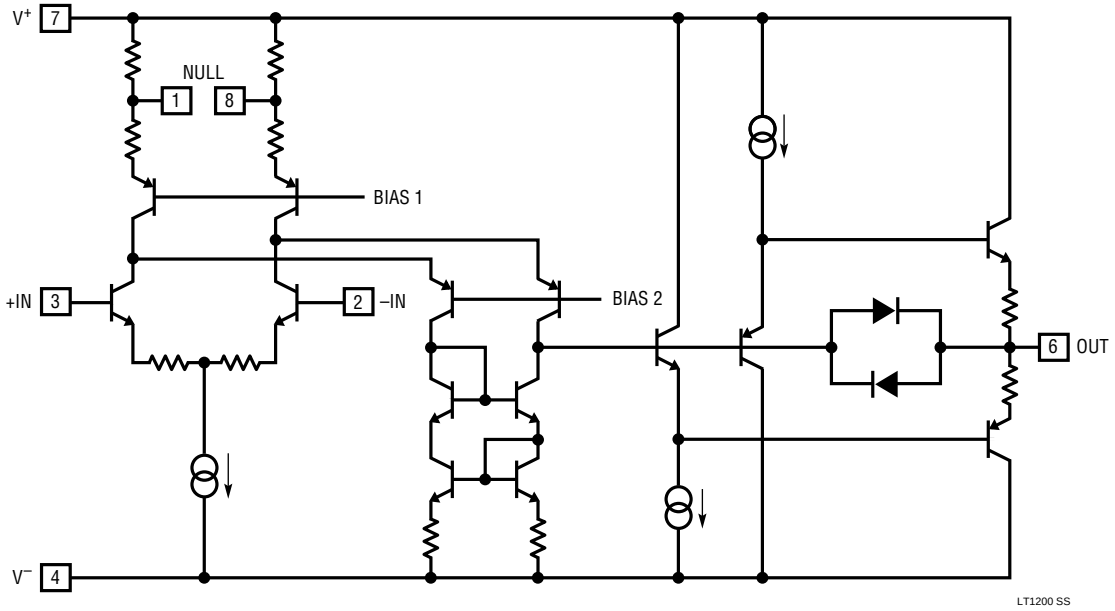


$$A_V = \frac{R4}{R3}\left[1 + \frac{1}{2}\left(\frac{R2}{R1} + \frac{R3}{R4}\right) + \frac{R2 + R3}{R5}\right] = 104$$

TRIM R5 FOR GAIN
TRIM R1 FOR COMMON MODE REJECTION
BW = 125kHz

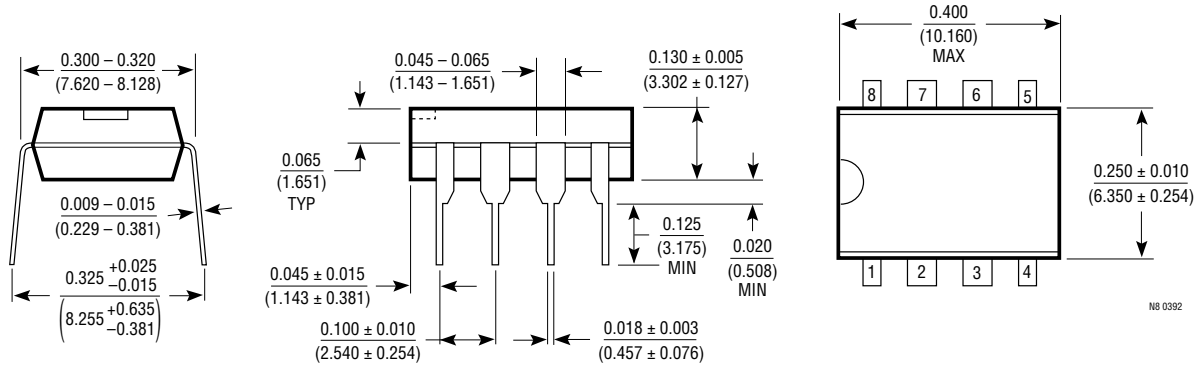
LT1200 TA05

SIMPLIFIED SCHEMATIC



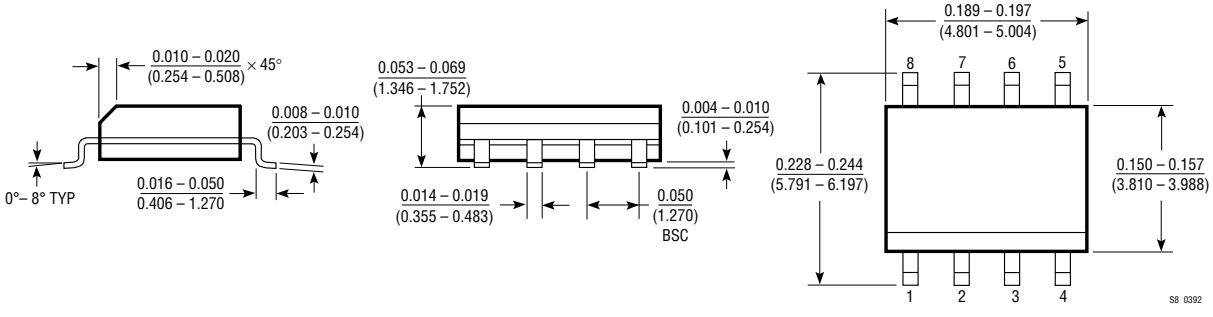
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

N8 Package
8-Lead Plastic DIP



$T_{J\,MAX}$	θ_{JA}
150°C	130°C/W

S8 Package
8-Lead Plastic SOIC



$T_{J\,MAX}$	θ_{JA}
150°C	220°C/W

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7487
(408) 432-1900 • FAX: (408) 434-0507 • TELEX: 499-3977
LT/GP 0492 10K REV 0