

Low-Power Cellular Upconverter-Driver

General Description

The MAX2307 is an integrated RF upconverter-driver optimized for the Japanese cellular frequency band. It can also be used for applications in the US cellular and ISM bands. Its low current consumption (15mA at -15dBm output) extends the average talk time.

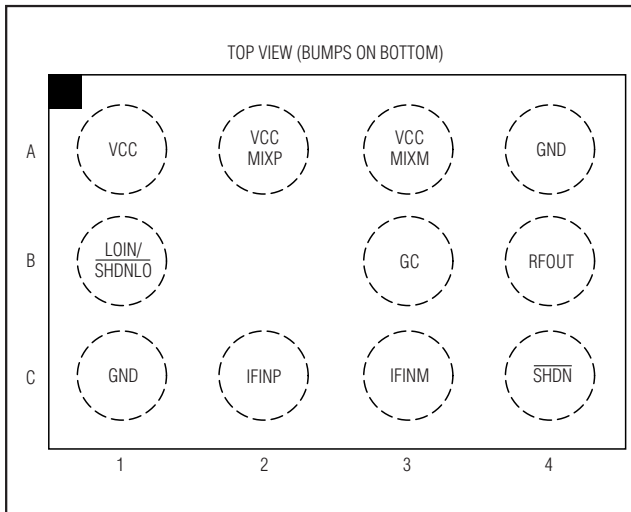
The image rejection is done using only two external inductors at the upconverter output because the image frequency in Japanese cellular phones is typically 330MHz away. This realizes the image rejection with no current consumption penalty and only two inexpensive off-chip components, saving cost and valuable board space.

The MAX2307 has a separate shutdown control for the LO buffer to minimize VCO pulling. It comes in an ultra-small 3x4 ultra-chip-scale package (UCSP).

Applications

Cellular Handsets
cdmaOne™ Handsets
ISM Band

Pin Configuration



cdmaOne is a trademark of CDMA Development Group.

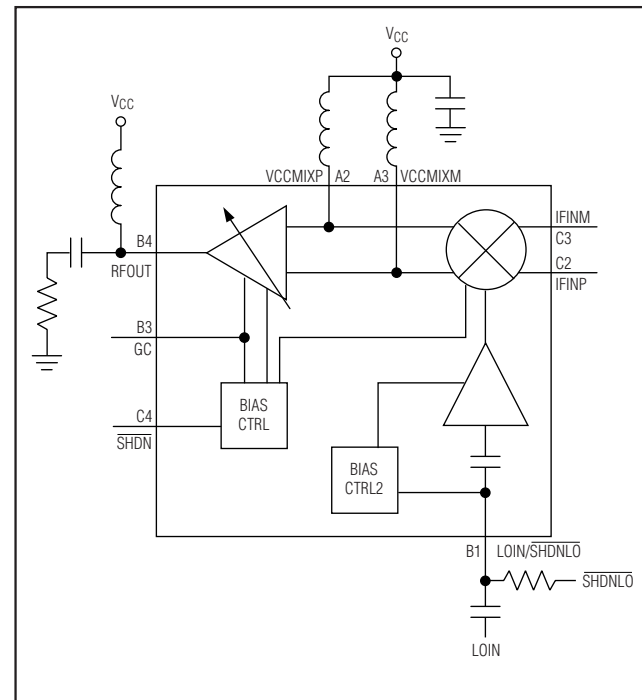
Features

- ◆ Ultra-Small Implementation Size
- ◆ Low Off-Chip Component Count
- ◆ 15mA at -15dBm P_{OUT}
- ◆ 34mA at +6.5dBm P_{OUT} and -53dBc ACPR
- ◆ <1μA Shutdown Mode
- ◆ Separate Shutdown for LO Buffer
- ◆ No External Logic Interface Circuitry Required

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX2307EBC	-40°C to +85°C	3x4 UCSP

Block Diagram



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ABSOLUTE MAXIMUM RATINGS

V_{CC} , RFOUT to GND	-0.3V to +5.5V	Operating Temperature Range	-40°C to +85°C
\overline{SHDN} to GND.....	-0.3V to ($V_{CC} + 0.3V$)	Junction Temperature	+150°C
RF, IF Input Power	0dBm	Storage Temperature Range	-65°C to +160°C
Continuous Power Dissipation ($T_A = +70^\circ\text{C}$)			
3x4 UCSP (derate 80mW/°C above +70°C)	628mW		

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

($V_{CC} = +2.8V$ to $+4.2V$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, no RF/IF signals applied, $V_{\overline{SHDN}} = V_{\overline{SHDNLO}} = +1.8V$. Typical values are at $V_{CC} = +3.0V$, $T_A = +25^\circ\text{C}$, unless otherwise noted).

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		2.8		4.2	V
Shutdown Supply Current	I_{CC}	$\overline{SHDN} = \overline{SHDNLO} = 0.6V$		0.1	20	μA
Standby Supply Current	I_{CC}	$\overline{SHDN} = 0.6V$, $\overline{SHDNLO} = 1.8V$		2.5	4	mA
Supply Current (Note 1)	I_{CC}	$V_{GC} = 2.2V$, $P_{OUT} = +6.5\text{dBm}$		33.5	42	mA
		$V_{GC} = 2.2V$, $P_{OUT} = +2\text{dBm}$		29.5	38	
		$V_{GC} = 0.5V$		14	20	
Supply Current with No RF Drive	I_{CC}	$V_{GC} = 2.2V$		28	36.5	mA
Gain Control Voltage	V_{GC}		0		3.0	V
\overline{SHDN} , \overline{SHDNLO} Logic High			1.8			V
\overline{SHDN} , \overline{SHDNLO} Logic Low			0		0.6	V
\overline{SHDN} , \overline{SHDNLO} Logic Current High					1	μA
\overline{SHDN} , \overline{SHDNLO} Logic Current Low			1			μA

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AC ELECTRICAL CHARACTERISTICS

(MAX2307 Evaluation Kit, $V_{CC} = +2.8V$ to $+4.2V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, $f_{RF} = 887MHz$ to $925MHz$, $f_{LO} = 722MHz$ to $760MHz$, $f_{IF} = 165MHz$, $P_{IFIN} = -20dBm$, $P_{LOIN} = -15dBm$, $V_{SHDN} = V_{SHDNLO} = +1.8V$, 50Ω system. Typical values are at $V_{CC} = 3.0V$, $V_{SHDN} = V_{SHDNLO} = 1.8V$, $f_{RF} = 906MHz$, $T_A = +25^{\circ}C$, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RF Frequency Range (Note 2)			887		925	MHz
Power Gain	G	$V_{GC} = 2.2V$, $V_{CC} = 3.0V$, $T_A = +25^{\circ}C$	21.5	24.5	27.5	dB
		$V_{GC} = 2.2V$, $V_{CC} = 2.8V$ to $4.2V$, $T_A = T_{MIN}$ to T_{MAX}	17	24.5	32.5	
Output Power	P_{OUT}	$V_{GC} = 2.2V$, $ACPR \leq -53dBc$, $ALT \leq -65dBc$	4.5	6.5		dBm
LO Input Power Level			-15	-12	-5	dBm
Gain Control Range		$V_{GC} = 0.5V$ to $2.2V$, $P_{IFIN} = -30dBm$	18	23		dB
Gain Control Slope (Note 3)		$V_{GC} = 0.5V$ to $2.2V$, $P_{IFIN} = -30dBm$		32	36	dB/V
Adjacent Channel Power Ratio	ACPR1	Offset = $\pm 885kHz$ in $30kHz$ BW			-53	dBc
Alternate Channel Power Ratio	ACPR2	Offset = $\pm 1.98MHz$ in $30kHz$ BW			-65	dBc
RX Band Noise Power (Note 4)	P_{NOISE}	$P_{OUT} = 6.5dBm$		-134	-131	dBm/Hz
		$P_{IFIN} = -50dBm$, $V_{GC} = 0.5V$		-147		
LO Leakage		P_{OUT} from $+6.5dBm$ to $-8dBm$		-43	-30	dBc
Image Leakage (Note 1)		P_{OUT} from $6.5dBm$ to $-8dBm$, $f_{RF} = 887MHz$ to $925MHz$, $f_{IMAGE} = 557MHz$ to $595MHz$		-40	-25	dBc

Note 1: Minimum and maximum limits are guaranteed by design and characterization.

Note 2: See *Typical Operating Characteristics* for operation outside this frequency range.

Note 3: Slope measured with $V_{GC} = +0.5V$ and $V_{GC} = +0.8V$.

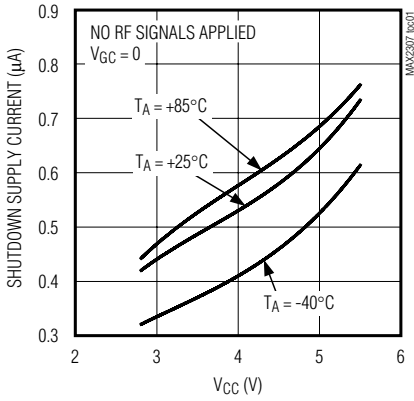
Note 4: $f_{RF} = 925MHz$, noise measured at $870MHz$.

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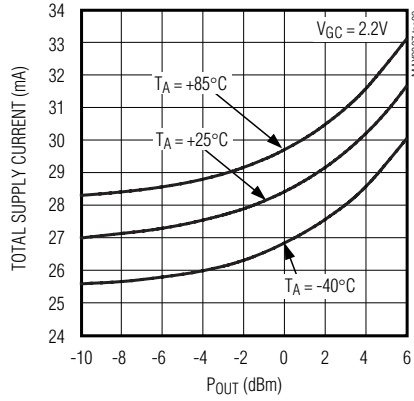
Typical Operating Characteristics

(MAX2307 Evaluation Kit, $V_{CC} = +2.8V$, $V_{GC} = 2.2V$, $V_{SHDN} = V_{SHDNLO} = V_{CC}$, $f_{RF} = 906MHz$, $f_{IF} = 165MHz$, $f_{LO} = 741MHz$, $T_A = +25^\circ C$, unless otherwise noted.)

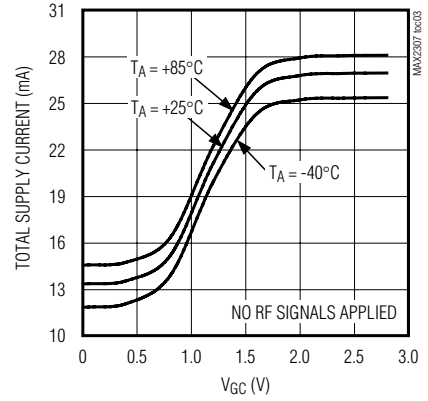
SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



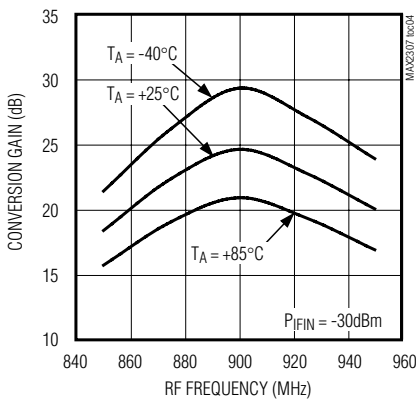
TOTAL SUPPLY CURRENT vs. OUTPUT POWER



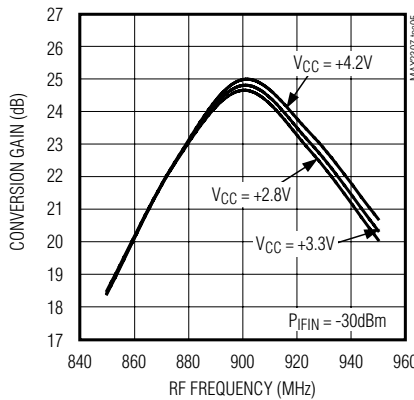
TOTAL SUPPLY CURRENT vs. GAIN CONTROL VOLTAGE



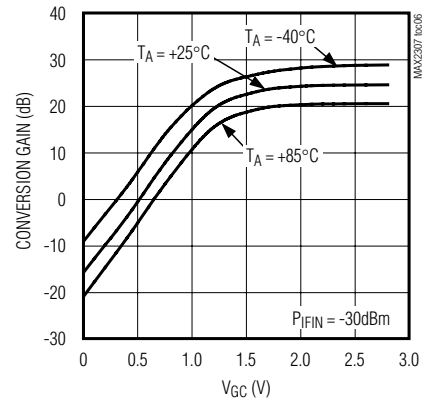
CONVERSION GAIN vs. RF FREQUENCY



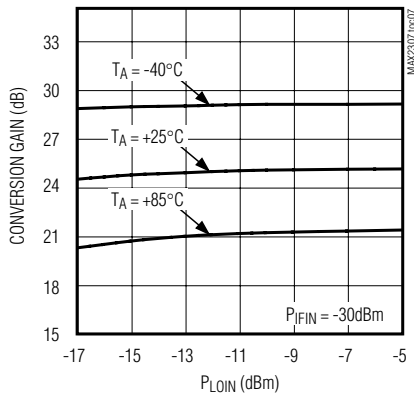
CONVERSION GAIN vs. RF FREQUENCY



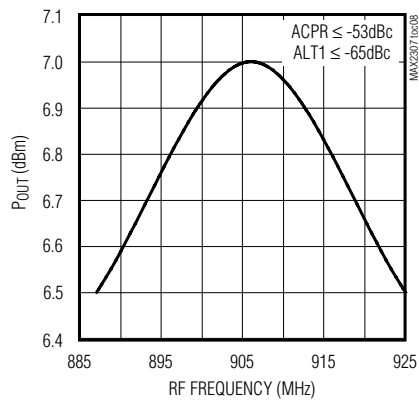
CONVERSION GAIN vs. GAIN CONTROL VOLTAGE



CONVERSION GAIN vs. LO INPUT POWER



OUTPUT POWER vs. RF FREQUENCY



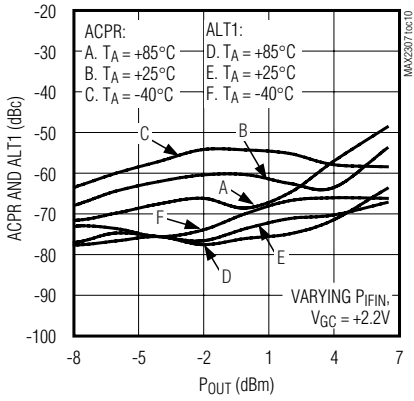
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MAX2307

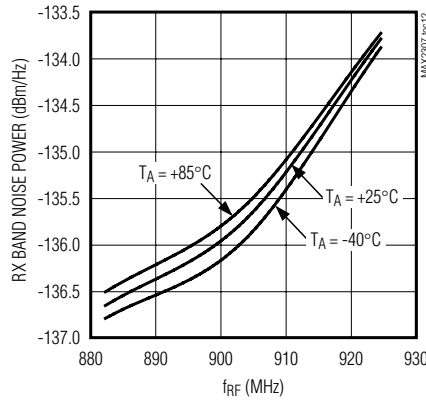
Typical Operating Characteristics (continued)

(MAX2307 Evaluation Kit, $V_{CC} = +2.8V$, $V_{GC} = 2.2V$, $V_{SHDN} = V_{SHDNLO} = V_{CC}$, $f_{RF} = 906MHz$, $f_{IF} = 165MHz$, $f_{LO} = 741MHz$, $T_A = +25^\circ C$, unless otherwise noted.)

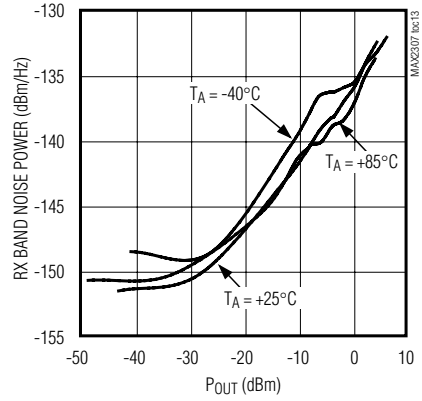
ACPR AND ALT1 vs. OUTPUT POWER



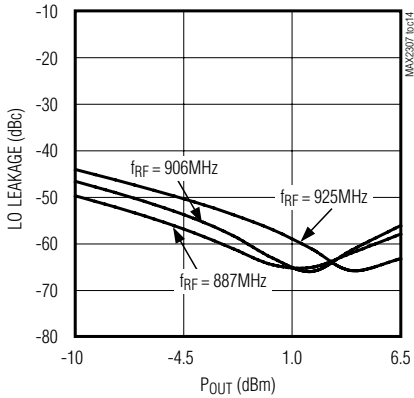
RX BAND NOISE POWER vs. RF FREQUENCY



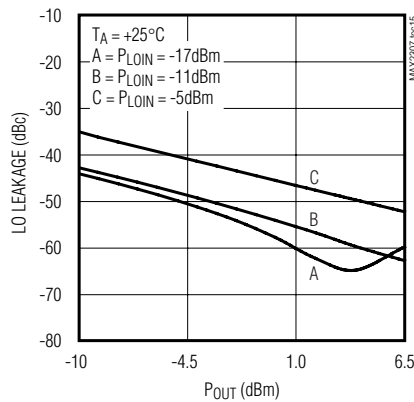
RX BAND NOISE POWER vs. OUTPUT POWER



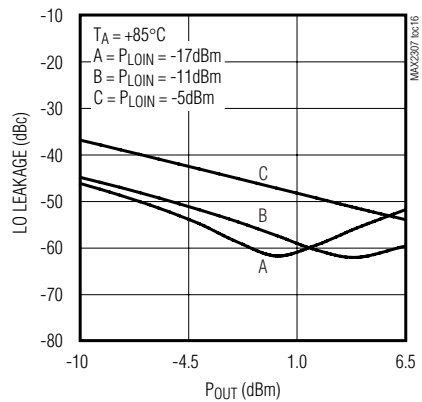
LO LEAKAGE vs. OUTPUT POWER



LO LEAKAGE vs. OUTPUT POWER



LO LEAKAGE vs. OUTPUT POWER



LO LEAKAGE vs. OUTPUT POWER

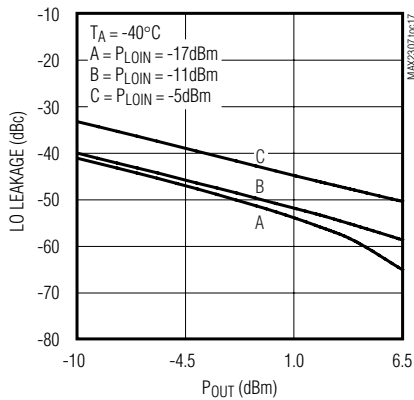
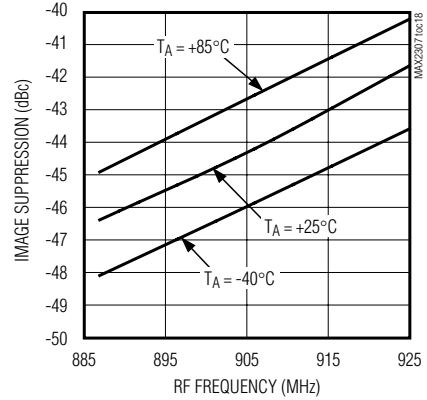


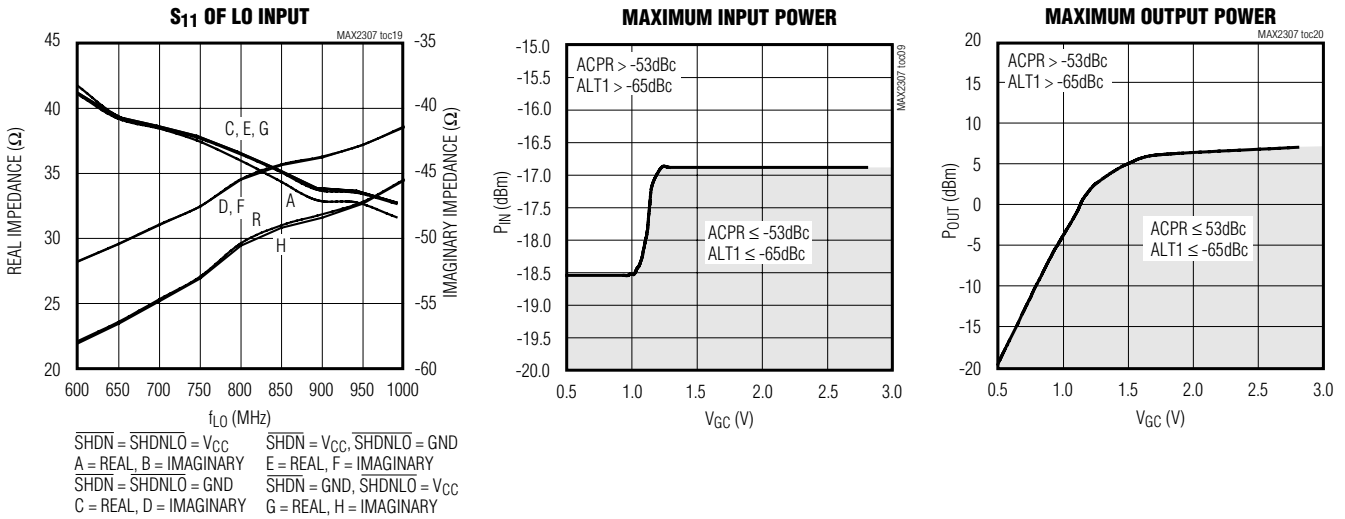
IMAGE LEAKAGE vs. RF FREQUENCY



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Typical Operating Characteristics (continued)

(MAX2307 Evaluation Kit, $V_{CC} = +2.8V$, $V_{GC} = 2.2V$, $V_{\overline{SHDN}} = V_{\overline{SHDNLO}} = V_{CC}$, $f_{RF} = 906MHz$, $f_{IF} = 165MHz$, $f_{LO} = 741MHz$, $T_A = +25^\circ C$, unless otherwise noted.)

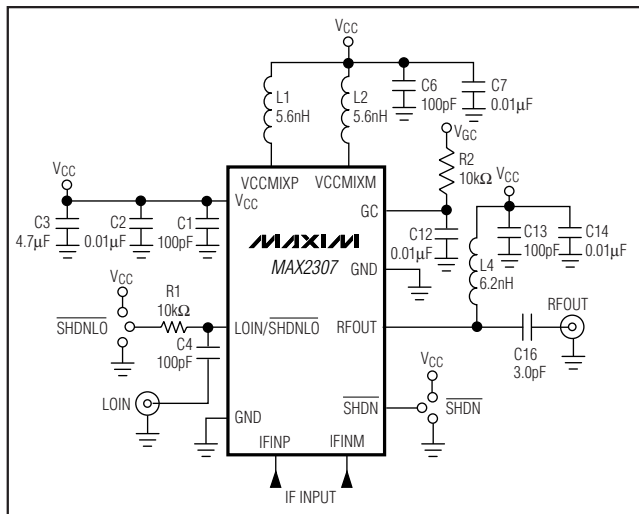


Pin Description

PIN	NAME	FUNCTION
A1	VCC	Supply Pin. Bypass with 100pF and 0.01 μ F capacitors as close to the pin as possible.
A2, A3	VCCMIXP, VCCMIXM	Mixer Supply Pins. Require pullup inductors, which are used as part of the image rejection filter network. Supply to inductors should be locally bypassed with 100pF and 0.01 μ F capacitors.
B1	LOIN/ \overline{SHDNLO}	LO Input and LO Buffer Shutdown. Apply both LO input signal and LO buffer shutdown control to this pin. The LO path requires a DC-blocking capacitor. A logic high on \overline{SHDNLO} turns on the LO buffer, and a logic low turns off the LO buffer, independently of \overline{SHDN} . The shutdown control requires a 10k Ω isolation resistor in order not to load the LO signal.
B3	GC	Gain Control Pin. Apply a voltage between 0 to 3V to vary the gain of the IC.
B4	RFOUT	PA Driver Output. Requires an inductor pullup and a DC-blocking capacitor. These components are also the matching elements.
A4, C1	GND	GND Connection. Solder directly to the PCB ground plane, with three ground vias around the corner of the UCSP, as close to bump as possible. It is imperative that GND sees a low inductance to the system ground plane. See the MAX2307 EV Kit as an example.
C2, C3	IFINP, IFINM	Upconverter IF Inputs. AC-couple IF signals to these pins.
C4	\overline{SHDN}	Shutdown Control. HIGH turns on the device except the LO buffer, LOW turns off the device except the LO buffer.

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Typical Operating Circuit



Applications Information

Local Oscillator LOIN/SHDNLO Input

The LO input is a single-ended broadband port. The LO signal is mixed with the input IF signal and the resulting upconverted output appears on the RFOUT pin. AC-couple the LO pin with a capacitor having less than 3Ω reactance at the LO frequency. This device also contains an internal LO buffer and supports an LO signal ranging from -15dBm to -5dBm.

$\overline{\text{SHDNLO}}$ turns the LO buffer on and off independent of the rest of the IC and shares the same pin as LOIN. To avoid loading of the LO, connect a $10k\Omega$ isolation resistor between the LOIN/SHDNLO pin and the $\overline{\text{SHDNLO}}$ logic output. The $\overline{\text{SHDNLO}}$ control can help reduce VCO pulling in gated-transmission mode by providing a means to keep the LO buffer on while the upconverter and driver turn on and off.

IF Input

The MAX2307 has a differential IF input port for interfacing to differential IF filters. AC-couple the IF pins with a capacitor. The typical IF input frequency is 165MHz, but device can operate from 130MHz to 230MHz. The differential impedance between the two IF inputs is approximately 400Ω in parallel with 0.5pF.

Mixer

The MAX2307 uses a double-balanced differential upconverting mixer. Two inductors connecting the mixer output pins (A2 and A3) to VCC in conjunction with an on-chip capacitor achieve image suppression. This method allows image rejection with no current consumption penalty, and permits much higher Q than

using on-chip inductors to ensure sufficient selectivity for image rejection. The Q of the off-chip tank inductor directly determines the image suppression level and usable bandwidth.

The MAX2307 also provides a continuous variable gain function, enabling at least 20dB of gain control using an external control voltage input.

PA Driver

The MAX2307 utilizes a class AB driver stage. Unlike class A or B, class AB action offers both good linearity and low current consumption. Current consumption of class AB is proportional to the output power at high drive levels.

RFOUT is an open-collector output that requires an external inductor to VCC for proper biasing. For optimum performance, implement an impedance-matching network. The configuration and values for the matching network depend on the transmit frequency, performance, and desired output impedance. For simultaneous optimum linearity and return loss, the real part of the load impedance should be about 100Ω . The device's internal 0.5pF shunt parasitic needs to be absorbed by the matching network. For matching network values for the Japanese cellular transmit band, see the MAX2307 EV kit data sheet.

Layout Issues

For best performance, pay close attention to power-supply issues, as well as to the layout of the RFOUT matching network. The EV kit can be used as a layout example. Ground connections and supply bypassing are the most important.

Power Supply and SHDN Bypassing

Bypass VCC with a 100pF capacitor in parallel with a 0.01µF RF capacitor. Use separate vias to the ground plane for each of the bypass capacitors and minimize trace length to reduce inductance. Use three separate vias to the ground plane for each ground pin.

Power-Supply Layout

To minimize coupling between different sections of the IC, the ideal power-supply layout is a star configuration with a large decoupling capacitor at a central VCC node. The VCC traces branch out from this central node, each going to a separate VCC node in the PC board. At the end of each trace is a bypass capacitor with low ESR at the RF frequency of operation. This arrangement provides local decoupling at each VCC pin. At high frequencies, any signal leaking out of one supply pin sees a relatively high impedance (formed by the VCC trace inductance) to the central VCC node, and an even higher impedance to any other supply pin, as

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well as a low impedance to ground through the bypass capacitor.

Impedance-Matching Network Layout

The RFOUT matching network is very sensitive to layout-related parasitics. To minimize parasitic inductance, keep all traces short and place components as close as possible to the chip. To minimize parasitic capacitance, minimize the area of the plane.

Chip Information

TRANSISTOR COUNT: 693

PROCESS TECHNOLOGY: Silicon Bipolar

Package Information

